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A Simple Commutation Method and a Cost-Effective Clamping Circuit for Three-to-Five-Phase Indirect-Matrix Converters

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Abstract: This article presents and analyzes a three-to-five-phase indirect matrix converter (IMC) structure for directly supplying a five-phase static $R-L$ load from a three-phase supply. The IMC topology offers a lower number of switches, a simple commutation procedure and a cost-effective clamping circuit in comparison to the direct matrix converter (DMC). A simple clamping circuit with one ultrafast diode and one small capacitor is proposed to protect the switches of the IMC from overvoltage. The issues of powering up the IMC with the simple clamping circuit is discussed in detail. The instructions for the safe start-up of the IMC with the proposed clamping circuit is introduced based on the simulated and the measured analyses. Moreover, a carrier-based pulse-width-modulation (CBPWM) method is also presented in order to control the switches of the IMC. The presented CBPWM method creates PWM pulses for both the inverter and the rectifier legs by using only one symmetric and triangular carrier signal. Finally, experimental and simulation testing with a five-phase R–L load demonstrate the viability and the efficiency of the introduced CBPWM algorithm for the suggested IMC.

Keywords: indirect-matrix converter; commutation technique; current-source rectifier; five-phase inverter; carrier-based PWM; space-vector-modulation

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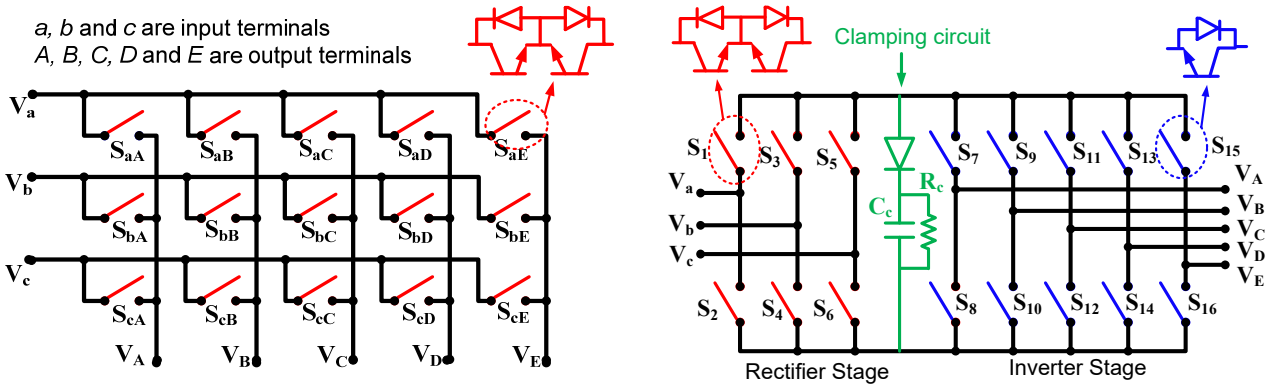
1. Introduction

Multi-phase drive systems are vital in high-reliability applications where a better fault-tolerant property is a must to ensure operation under exceptional circumstances [1,2]. The combination of the high-power operating requirement and the robustness requirements are widely represented in aerospace applications and electric vehicles [2–4]. Multi-phase drive systems also offer characteristics that make them competitive in a variety of different industries. The number of phases in electric machines can be increased to improve torque-density, reduce noise and vibrations levels, and develop multi-motor technologies [5–8].

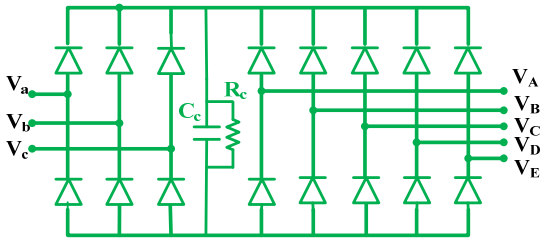
A multi-phase rectifier-inverter converter is generally used to energize a multi-phase motor drive. However, this converter entails a large reactive DC-link element, which is a specific scrawny point in a harsh environment [9]. This difficulty is eliminated using the matrix converter (MC) [10]. A direct AC-to-AC conversion of power without the need for DC-energy storage is possible with MCs. They have lately received a lot of attention as an alternative to the traditional rectifier inverter [11,12]. Many benefits can be obtained from MCs, including sinusoidal input- and output-current waveforms, high power density, unity-input-power factor and four-quadrant operation [13,14]. Furthermore, because of the nonexistence of the massive DC-link electrolytic capacitors for energy storage, MCs are very dependable and robust [15,16].

There are a number of other advantages to using MCs in a practical manner. First, thanks to the introduction of SiC and GaN technologies, this topology tends to solve the problem of thermal management, and it performs significantly better under high-temperature circumstances than traditional DC-link topologies [17,18]. Second, the switches in the MCs are exposed to lower voltage stress compared to the switches in traditional converters. Despite the increased number of IGBTs, the MCs' success rates are improved by the lesser stress on their switches. As a result, these converters (MCs) have a better level of reliability than traditional converters (DC-link rectifier inverters) [16–18]. Manufacturers such as Yaskawa, Siemens, ABB, and others have expressed their interest in this converter for the reasons stated above. Consequently, there is a lot of work being done to use this technology in more electric and quieter aircrafts.

Direct (DMC) and indirect (IMC) MCs are the two different forms of MCs. The three-to-five-phase DMC is a one-stage AC-to-AC direct converter with 15 bidirectional switches that directly link the three-phase input voltages to the five-phase output loads as shown in Figure 1a [17,18]. Nevertheless, this topology necessitates a large number of power switches, multi-step-commutation techniques, and complex overvoltage-protection circuits. The IMC structure is built using an AC-to-DC-to-AC power conversion with no massive intermediary capacitor. The IMC is divided into two stages, the rectifier stage and the inverter stage, as reported in Figure 1b [19]. The maximum value of the voltage-transfer ratio and the characteristics of the input/output are all the same between the DMC and the IMC topologies. The IMC architecture, on the other hand, allows for soft-switching commutation, which is not possible in the DMC topology. In addition, as compared to the DMC, the IMC requires a simpler clamping circuit, which is utilized to avoid the IMC's switches from breaking down due to overvoltage. Figure 1c shows the conventional clamping circuit for the three-to-five-phase MC, which consists of 16 ultrafast diodes, a clamping capacitor, and resistance. Moreover, the IMCs have the capability of reducing the number of power switches. The IMC has 22 IGBTs compared to 30 IGBTs in the case of the DMC, as described in Figure 1. In addition, the IMC has the capability of supplying the electricity to an imbalanced or nonlinear three-phase load. This is accomplished by placing an extra leg at the inverter stage. The voltage-transfer ratio in the case of the IMC can be increased by adding a *Z*-source network between the rectifier and the inverter stages [20,21]. In the IMC, the rectifier-stage switches are commutated at zero current, which minimizes the rectifier switching losses. Consequently, the rectifier stage achieves safer commutation and lower switching losses. The IMC has lately received a lot of attention, and several researchers have created numerous IMC topologies that are suited for certain applications. The authors of [22,23] focused on using zero-current commutation to enhance the structure of the rectifier stage in the IMC using reduced-power devices.



(**a**) (**b**)



(**c**)

Figure 1. (**a**) DMC, (**b**) IMC and (**c**) conventional clamping circuit.

Besides the advancement of MC topologies, pulse-width-modulation (PWM) techniques have lately attracted a lot of attention [24,25]. The space-vector-PWM (SVPWM) and carrier-based-PWM (CBPWM) techniques are two PWM schemes for IMCs. Some parts of the SVPWM technique are complicated [16,21,26–28]. In recent years, researchers have used the CBPWM technique to simplify the SVPWM [14,29–32]. The carrier signal used in the rectifier stage of the conventional CBPWM method [29–32] differs from that used in the inverter stage; the rectifier-stage carrier signal is a symmetrical triangular signal, whereas the inverter-stage carrier signal is an asymmetrical triangular signal with different slopes of the rising and falling edges. Furthermore, because of the fluctuation in the DC-link voltage, the slopes of the asymmetrical carrier signal differ at each sampling interval. To overcome the drawbacks of the conventional CBPWM method, the authors of [33] proposed an effective alternative method that is suitable for the three-to-five-phase IMC topology by generating the PWM signals for all of the switches in both the rectifier and five-phase-inverter stages using only one symmetrical triangular carrier signal.

The majority of the scientific focus on the MC is dedicated to enhancing modulation (SVM [34], CBPWM [33], direct torque control [35], etc.), control techniques (wind generation [36], distributed generation [37], loss reduction [38], common mode voltage reduction [39], sensorless control [40], etc.), waveform quality [41], stability analysis [42], and semisoft commutation [43], etc. However, there are just a few publications that look into MC hardware and the issues that come with it. The majority of them focus on novel switches with reverse-blocking capability (reverse-blocking IGBT) [44] and clamp circuits [45] as MC-protection circuits. Most of the protection circuits use the conventional clamping circuit shown in Figure 1c. In [46], a simplified IMC structure with just six diodes in a clamp circuit is suggested, which has the same functionality as its twelve-diode version. In [47], an open-circuit analysis for a three-phase-to-three-phase IMC with a simple clamping circuit was proposed. The clamping circuit in [47] consists of only one diode and one capacitor. This clamping circuit is used with the introduced three-to-five-phase IMC. However, if several key considerations are not followed when working with the IMC, then this simple clamping circuit may cause damage to the matrix's switches instead of protecting them. These key considerations are experimentally studied and discussed in this paper.

This paper introduces a three-to-five-phase indirect MC with a cost-effective and simple clamp circuit that consists of only one diode and one capacitor. A detailed discussion about the clamping circuit is introduced considering the issues concerned with charging the clamping capacitor and the start-up of the converter when the PWM of the rectifier is working. These issues are experimentally tested and analyzed. Moreover, a CBPWM based on space-vector modulation (SVM) is implemented. In this method, a zero-current commutation in the rectifier stage is maintained by using the CBPWM to minimize the switching losses. This is achieved by considering the synchronization between the rectifier and inverter stages, where the commutation in the rectifier stage occurs at the zero vectors of the inverter, i.e., at zero DC-link current. Hence, a lower switching loss is obtained. Finally, the simulated and the measured performances of the indirect MC with the CBPWM technique at different output frequencies are introduced and discussed.

2. Five-Phase Indirect-Matrix Converter

The proposed three-to-five-phase IMC's power-circuit architecture is seen in Figure 1b. It comprises a rectifier stage and a five-phase inverter stage. Six bidirectional switches are used in the rectifier stage, whereas the inverter stage uses only ten unidirectional switches. The purpose of the rectifier stage is to build sinusoidal input currents while also keeping the DC-link voltage positive. The five-phase inverter stage produces five-phase output voltages with adjustable magnitude and frequency. The familiar theory of the indirect SVM is firstly introduced to describe the suggested IMC topology's working principles.

2.1. Indirect Space Vector Modulation

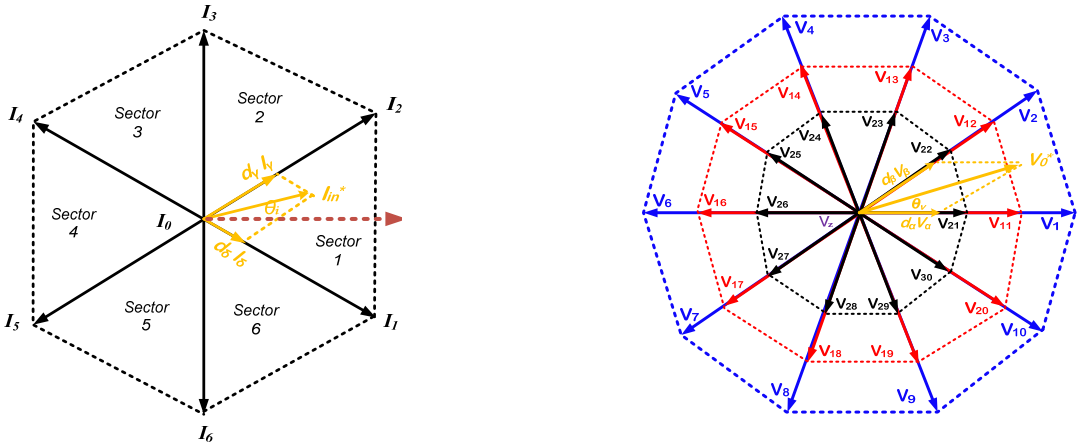
The indirect SVM approach is a popular method to control the IMC. In this approach, there are two stages (the rectifier stage and the inverter stage). The required input current, available input voltages, and required output voltages are used to compute the controlling pulses for the switches of the rectifier stage and the inverter stage.

2.1.1. Current-Source Rectifier

The rectifier stage comprises 6 bidirectional switches as seen in Figure 1b. Because of the lack of bidirectional switches on the market, the bidirectional switches in the rectifier stage are made up of two unidirectional common-emitter switches. The input voltage to the rectifier stage can be described by Equation (1). In Equation (1), i represents the input-phase number, e.g., a, b and c. In Equation (1), f_i and V_{im} represent the frequency and the peak of the phase input voltage, respectively. In Equation (1), ∂ is 0, 1 and 2.

$$v_i = V_{im} \cos\left(2\pi * f_i * t - \partial * \frac{2\pi}{3}\right) \quad (1)$$

There are only nine switching states allowed for these switches in order to prevent a virtual DC-connection open circuit. These switching states are six non-zero (active) vectors ($I_1 - I_6$) and three zero vectors ($I_7 - I_9$) as represented by the hexagon in Figure 2a. For both the zero and active vectors, the duty cycles are determined using the yellow-colored vectors in Figure 2a, as shown in Equations (2)–(4) [34].



(**a**) (**b**)

Figure 2. (**a**) The rectifier's hexagon and (**b**) the inverter's decagon.

$$d_\delta = m_i \sin\left(\frac{\pi}{6} - \theta_i\right) \quad (2)$$

$$d_\gamma = m_i \sin\left(\frac{\pi}{6} + \theta_i\right) \quad (3)$$

$$d_{0c} = 1 - d_\gamma - d_\delta \tag{4}$$

where m_i is the input-current-modulation index with a value between 0 and 1. In addition, θ_i indicates the measured angle starting from the positive X-axis to the rectifier's input reference-current vector ($2\pi \times f_i \times t$).

The zero-vectors are ignored during the rectifier-stage modulation with the aim of obtaining the greatest DC-link voltage. As a result, the switching sequence simply comprises the two active vectors, I_γ and I_δ, whose duty cycles are d_x and d_y, respectively, and can be defined by Equations (5) and (6) [16]. The average DC-link voltage in the first sector can be calculated from Equation (7). The switching states and the duty cycles for the other sectors may be determined using the same method as reported in Table 1.

$$\begin{gathered} d_x = \frac{d_\delta}{d_\delta + d_\gamma} = \\ \frac{m_i[\sin\left(\frac{\pi}{6}\right)\cos(\theta_i) - \cos\left(\frac{\pi}{6}\right)\sin(\theta_i)]}{m_i[\sin\left(\frac{\pi}{6}\right)\cos(\theta_i) - \cos\left(\frac{\pi}{6}\right)\sin(\theta_i) + \cos\left(\frac{\pi}{6}\right)\sin(\theta_i) + \sin\left(\frac{\pi}{6}\right)\cos(\theta_i)]} \\ = \frac{-\cos\left(\theta_i - \frac{2\pi}{3}\right)}{\cos(\theta_i)} = -\frac{v_b}{v_a} \end{gathered} \tag{5}$$

$$\begin{gathered} d_y = \frac{d_\gamma}{d_\delta + d_\gamma} = \\ \frac{m_i[\sin\left(\frac{\pi}{6}\right)\cos(\theta_i) + \cos\left(\frac{\pi}{6}\right)\sin(\theta_i)]}{m_i[\sin\left(\frac{\pi}{6}\right)\cos(\theta_i) - \cos\left(\frac{\pi}{6}\right)\sin(\theta_i) + \cos\left(\frac{\pi}{6}\right)\sin(\theta_i) + \sin\left(\frac{\pi}{6}\right)\cos(\theta_i)]} \\ = \frac{-\cos\left(\theta_i + \frac{2\pi}{3}\right)}{\cos(\theta_i)} = -\frac{v_c}{v_a} \end{gathered} \tag{6}$$

$$V_{DC} = d_x v_{ab} + d_y v_{ac} = \frac{-v_a(v_a - v_b)}{v_a} + \frac{-v_c(v_a - v_c)}{v_a} = \frac{v_a^2 + v_b^2 + v_c^2}{v_a} = \frac{3V_{im}^2}{2v_a} \tag{7}$$

Table 1. The switching states, the duty cycles, and the DC-link voltage for the rectifier in all sectors.

Sector Number	ON Switch	The Duty Cycles and Modulated Switches				DC-Link Voltage
		d_x		d_y		
1	S_1	S_4	$-\frac{v_b}{v_a}$	S_6	$-\frac{v_c}{v_a}$	$\frac{3V_{im}^2}{2v_a}$
2	S_6	S_3	$-\frac{v_b}{v_c}$	S_1	$-\frac{v_a}{v_c}$	$-\frac{3V_{im}^2}{2v_c}$
3	S_3	S_6	$-\frac{v_c}{v_b}$	S_2	$-\frac{v_a}{v_b}$	$\frac{3V_{im}^2}{2v_b}$
4	S_2	S_5	$-\frac{v_c}{v_a}$	S_3	$-\frac{v_b}{v_a}$	$-\frac{3V_{im}^2}{2v_a}$
5	S_5	S_2	$-\frac{v_a}{v_c}$	S_4	$-\frac{v_b}{v_c}$	$\frac{3V_{im}^2}{2v_c}$
6	S_4	S_1	$-\frac{v_a}{v_b}$	S_5	$-\frac{v_c}{v_b}$	$-\frac{3V_{im}^2}{2v_b}$

2.1.2. Five-Phase Voltage-Source Inverter

The switches of the inverter stage have 32 allowed switching states in order to prevent the short circuit of the virtual DC link and the open circuit of the load terminals. There are 30 active vectors ($V_1 - V_{30}$) in these states and 2 zero vectors (V_0) as shown in the decagon in Figure 2b. There are three groups for the active vectors: small vectors ($0.2472\,V_{DC}$), medium vectors ($0.4\,V_{DC}$) and large vectors ($0.6472\,V_{DC}$) [48]. As shown in Equation (8) and Figure 2b, the reference output voltage (V_o^*) is obtained using the adjacent vectors (V_α , V_β and V_z). The duty cycles of these adjacent vectors are calculated using the yellow-colored vectors in Figure 2b as in Equations (9)–(11). In Equations (9) and (10), θ_v indicates the measured angle starting from the first vector in the associated sector to the reference-output-voltage vector, and m_v is the output-voltage-modulation index for the inverter [48].

$$V_O^* = d_\alpha V_\alpha + d_\beta V_\beta + d_z V_z \tag{8}$$

$$d_\alpha = m_v \ \sin\left(\frac{\pi}{5} - \theta_v\right) \tag{9}$$

$$d_\beta = m_v \ \sin(\theta_v) \tag{10}$$

$$d_z = 1 - d_\alpha - d_\beta \tag{11}$$

In this paper, large and medium vectors are only considered in order to obtain the reference output voltage so as to reduce the amount of switching occurrences. The large- and medium-voltage-vector duty cycles are determined based on their length relative to each other. This is clarified in Equations (12)–(15).

$$d_{\alpha l} = d_\alpha \frac{V_l}{V_l + V_m} = 0.618 d_\alpha \tag{12}$$

$$d_{\alpha m} = d_\alpha \frac{V_m}{V_l + V_m} = 0.382 d_\alpha \tag{13}$$

$$d_{\beta l} = d_\beta \frac{V_l}{V_l + V_m} = 0.618 d_\beta \tag{14}$$

$$d_{\beta m} = d_\beta \frac{V_m}{V_l + V_m} = 0.382 d_\beta \tag{15}$$

Notice that the times of the medium and the large vector are 38.2% and 61.8% of the overall active time, respectively. Accordingly, the value of the reference-output-voltage vector is limited to $0.5257\,V_{DC}$ [34]. For further minimization of switching, the switching sequence is arranged as in Equation (16) [49,50]. Table 2 describes the switching vectors that minimize switching losses in various sectors. The switching state V_{11} (10000) in Table 2 indicates that the inverter switches S_7, S_{10}, S_{12}, S_{14} and S_{16} are turned on, while switches S_8, S_9, S_{11}, S_{13} and S_{15} are turned off. Figure 3 depicts the switching pattern for the upper switches of the five-phase VSI in the first sector. It should be noticed that only one of the upper switches' states is changed between two adjacent switching states.

$$\begin{gathered} \frac{d_{z1}}{2}, \frac{d_{\alpha m}}{2}, \frac{d_{\beta l}}{2}, \frac{d_{\alpha l}}{2}, \frac{d_{\beta m}}{2}, \frac{d_{z2}}{1}, \frac{d_{\beta m}}{2}, \frac{d_{\alpha l}}{2}, \frac{d_{\beta l}}{2}, \frac{d_{\alpha m}}{2}, \frac{d_{z1}}{2} \\ d_{z1} = \ d_{z2} = \frac{d_z}{2} \end{gathered} \tag{16}$$

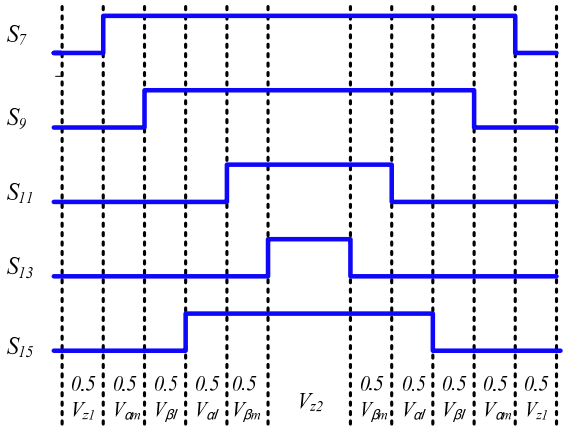


Figure 3. Switching sequence for a five-phase voltage-source inverter (VSI) in the first sector.

Table 2. Inverter's switching vectors, which minimize switching losses in all sectors.

Sector No.	$V_{\alpha m}$	$V_{\alpha l}$	$V_{\beta m}$	$V_{\beta l}$	V_{z1}	V_{z2}
1	V_{11} (10000)	V_1 (11001)	V_{12} (11101)	V_2 (11000)		
2	V_{13} (01000)	V_2 (11000)	V_3 (11100)	V_{12} (11101)		
3	V_{13} (01000)	V_4 (01100)	V_3 (11100)	V_{14} (11110)		
4	V_{15} (00100)	V_4 (01100)	V_5 (01110)	V_{14} (11110)		
5	V_{15} (00100)	V_6 (00110)	V_5 (01110)	V_{16} (01111)	V_{31} (00000)	V_{32} (11111)
6	V_{17} (00010)	V_6 (00110)	V_7 (00111)	V_{16} (01111)		
7	V_{17} (00010)	V_8 (00011)	V_7 (00111)	V_{18} (10111)		
8	V_{19} (00001)	V_8 (00011)	V_9 (10011)	V_{18} (10111)		
9	V_{19} (00001)	V_{10} (10001)	V_9 (10011)	V_{20} (11011)		
10	V_{11} (10000)	V_{10} (10001)	V_1 (11001)	V_{20} (11011)		

2.2. Carrier-Based Pulse Width Modulation

The previously introduced indirect-SVM study demonstrates that the SVM for the five-phase indirect MC may be implemented following a complicated procedure. In the rectifier and the inverter stages, the selection of the operative vectors is carried out independently. Various and complex equations are employed to compute the duty ratios of the effective vectors in the rectifier and in the inverter stages. The rectifier and inverter stages' switching states are then synchronized to produce balanced output voltages and to ensure a zero-current commutation in the rectifier stage. The CBPWM technique was created to solve these issues by making it simple to produce gating pulses for the rectifier and the inverter. PWM signals are generated in the CBPWM technique when the modulation signals are compared to a carrier signal with a high frequency ($1/T_s$). Accordingly, the CBPWM method begins with identifying the carrier signal and the modulation signals. For both the rectifier and inverter stages in this study, just one symmetrical and triangular carrier signal is employed to produce PWM signals.

As illustrated in Figure 4 (a), the carrier signal ($v_{carr.}(t)$) is defined as follows:

$$v_{carr.} = V_{im}\left(\frac{4}{T_s}t - 1\right), \quad t = 0{:}\frac{T_s}{2} \tag{17}$$

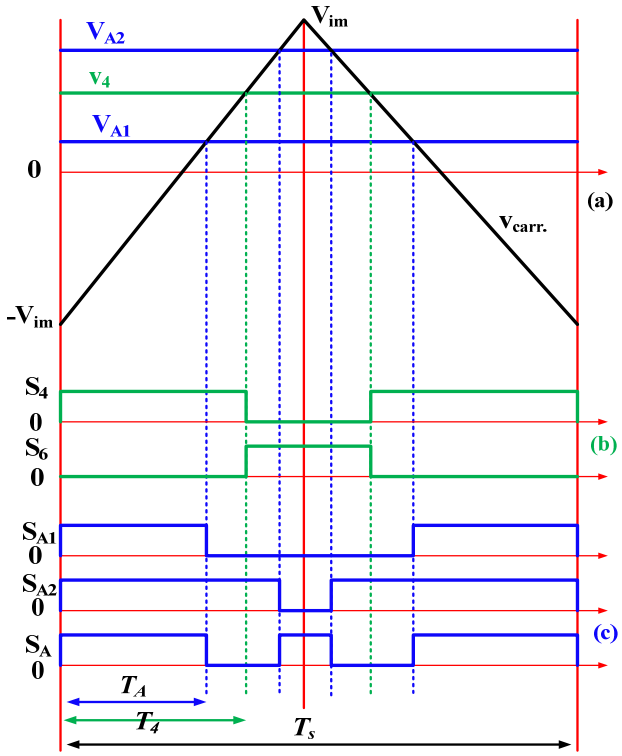


Figure 4. (a) Carrier and modulation signals, (b) the duty cycle of rectifier and (c) inverter in sector 1 using CBPWM.

2.2.1. Current-Source Rectifier

For the rectifier and when the vector of the reference input current is located in the first sector, the switching pattern and the timing of the modulated switches can be described as shown in Figure 4 (b). The duration of the gate pulse of the switch S_4 (T_4) is defined by Equation (18). The modulated signal of the rectifier switch S_4 (V_4) is given by Equation (19). The operating pulse of switch S_4 is obtained by comparing the modulated signal in Equation (19) with the carrier signal as seen in Figure 4 (b). The operating pulse of switch S_6 is the complement of the pulse of switch S_4, and switch S_1 is constantly on in the first sector. Switches S_2, S_3 and S_5 are constantly off in the first sector. The switching states and the duty cycles for other sectors may be determined using the same method as reported in Table 1.

$$T_4 = d_x \frac{T_s}{2} \tag{18}$$

$$V_4 = V_{im}(2d_x - 1) \tag{19}$$

2.2.2. Five-Phase Inverter

For the inverter, two modulation signals are provided in order to obtain the required output voltage despite the DC-link-voltage volatility. These signals are generated from duty ratios d_x and d_y, respectively. These duty ratios are dependent on the DC-link voltage as given by Equations (20) and (21). For example, two modulation signals V_{A1} and V_{A2} are required to create the gate signal for the top switch of phase A. Figure 4 (a) depicts the waveforms of V_{A1} and V_{A2}, as well as the carrier signal ($v_{carr.}(t)$). Then, two pulses S_{A1} and S_{A2} are achieved by individually comparing the two modulation signals V_{A1} and V_{A2} with the carrier signal ($v_{carr.}(t)$). Finally, the logic-XNOR function is used to determine the gate signal for switch S_A (S_7 in Figure 1b), as illustrated in Figure 4 (c) and Equation (23).

This is also clearly depicted in the block diagram illustrated in Figure 5. It can be clearly noticed from Figure 4 that when commutation occurs in the rectifier stage, the inverter stage works on the zero vectors to ensure the rectifier's zero-DC-link-current commutation. As a result, during commutation, all currents flowing through the switches of the rectifier are zero. The rectifier stage's switching loss is reduced, and a complicated multi-step-commutation procedure is avoided.

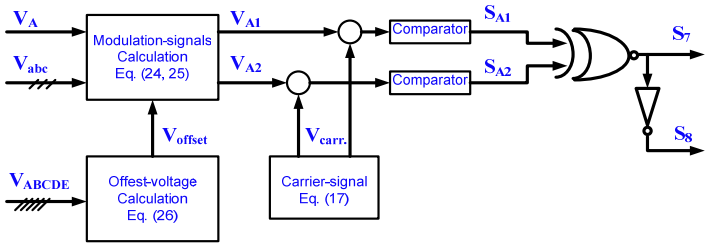


Figure 5. The CBPWM block diagram for the inverter stage in the IMC.

$$V_{A1} = V_{im}(-2d_y \frac{v_A + v_{offset}}{V_{DC}} + d_x) \tag{20}$$

$$V_{A2} = V_{im}(2d_x \frac{v_A + v_{offset}}{V_{DC}} - d_y) \tag{21}$$

$$v_{offset} = -\frac{1}{2}(v_A + v_D) \tag{22}$$

$$S_A = S_{A1} \odot S_{A2} \tag{23}$$

For a generic formulation for the other phases, the modulation signals for switch S_M can be written as in Equations (24) and (25). In Equations (24)–(27), M represents the output phase number A, B, C, D and E, and v_{max} and v_{min} indicate the maximum and minimum values of the output phase voltages, respectively.

$$V_{M1} = V_{im}(-2d_y \frac{v_M + v_{offset}}{V_{DC}} + d_x) \tag{24}$$

$$V_{M2} = V_{im}(2d_x \frac{v_M + v_{offset}}{V_{DC}} - d_y) \tag{25}$$

$$v_{offset} = -\frac{1}{2}(v_{max} + v_{min}) \tag{26}$$

$$S_M = S_{M1} \odot S_{M2} \tag{27}$$

3. Clamping Circuit and Input Filter

This section introduces the input filter and the simple clamping circuit that are used with the three-to-five-phase indirect MC. The start-up issues and difficulties associated with the proposed clamping circuit are investigated in this section. The experimental validation for these issues is also presented in this section. The guidelines for the safe start-up of the proposed IMC with the simple clamping circuit is introduced.

3.1. Analysis of Clamping Circuit

The lack of the DC connection, which is common in other voltage-source-inverter topologies, is one of the most appealing features of the MC design when used in aviation applications. As a result, with an MC, no electrolytic capacitors are needed. Therefore, the

removal of the load's energy in some situations, such as an over-current situation, a failure in the commutation process, and/or during start-up of the operation of the MC, might cause overvoltage at the converter's input because the matrix converter does not have an energy-storage facility. A diode bridge with ultrafast diodes linked to each input and output side of the MC, as well as a capacitor, is definitely the most commonly employed protection approach [51]. However, this two-bridge clamping circuit can be easily replaced by the simple clamping circuit shown in Figure 1b. It consists of only one diode and one capacitor.

The capacitor must store all of the inductive load energy without causing harmful overvoltages; therefore, it must be properly sized. The capacitor size is determined using the maximum stored load energy (W_{load}) in motor inductance (L) and the maximum accessible clamp voltage, and may be computed as follows:

$$W_{load} = \frac{1}{2}L(i_A^2 + i_B^2 + i_C^2 + i_D^2 + i_E^2) \tag{28}$$

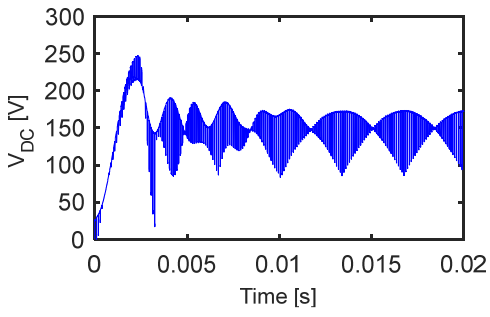
The change in the clamp-capacitor stored energy from its starting voltage to its final voltage may be utilized to compute the capacitor size, as illustrated in Equation (29). In Equation (29), C_c represents the capacitance of the clamping capacitor, V_{MAX} represents the maximum voltage allowable for MC switches and V_{MIN} represents the initial voltage of the capacitor.

$$W_{load} = \frac{1}{2}C_c(V_{MAX}^2 + V_{MIN}^2) \tag{29}$$

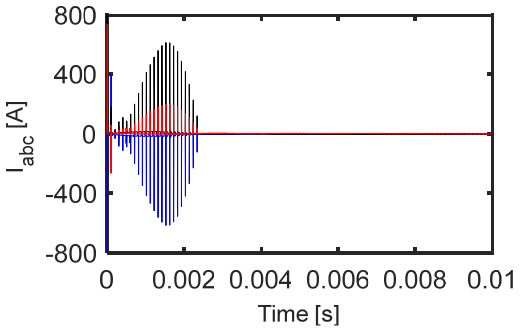
For high-power multi-phase drives, e.g., with 17.3 A (peak current), 0.05 H inductance, and 1200 V as the maximum allowable voltage for switches [2], the clamping circuit is chosen as 110 μF as a safety. When supplying these high-power drive systems with the proposed three-to-five-phase indirect MC (given in Figure 1b) with the proposed clamped circuit with a capacitor of 110 μF, there are some issues related to powering up the MC, e.g., due to inrush current and start-up with the operation of the PWM of the rectifier. To clarify these issues and determine their impact, simulation and experimental results have already been generated for the proposed indirect MC.

Figure 6 displays the simulation results for testing of the clamping circuit at start-up with the operation of the PWM of the rectifier. It can be noticed from Figure 6b that there is an extremely high supply current while charging the capacitor up to about 600 A, which causes current protection to work and a sudden trip of the circuit breaker occurs, and as a result an extremely high voltage occurs that causes the breakdown of matrix switches. Hence, the rectifier PWM must be stopped during the start-up of the MC.

Figure 7 describes the simulation results for the testing of the clamping circuit at start-up without operation of the PWM of the rectifier, and with the capacitor being charged using any line voltage, e.g., V_{ab}. It can be noticed from Figure 7c that the maximum input current during capacitor charging is about 15 A. However, there is a high pulse current at time zero. This is because the start-up is not at zero voltage, as shown in Figure 7a.



(**a**)



(**b**)

Figure 6. Simulation testing of the clamping circuit at start-up with operation of the PWM of the rectifier (**a**) DC-link voltage and (**b**) input current for MC.

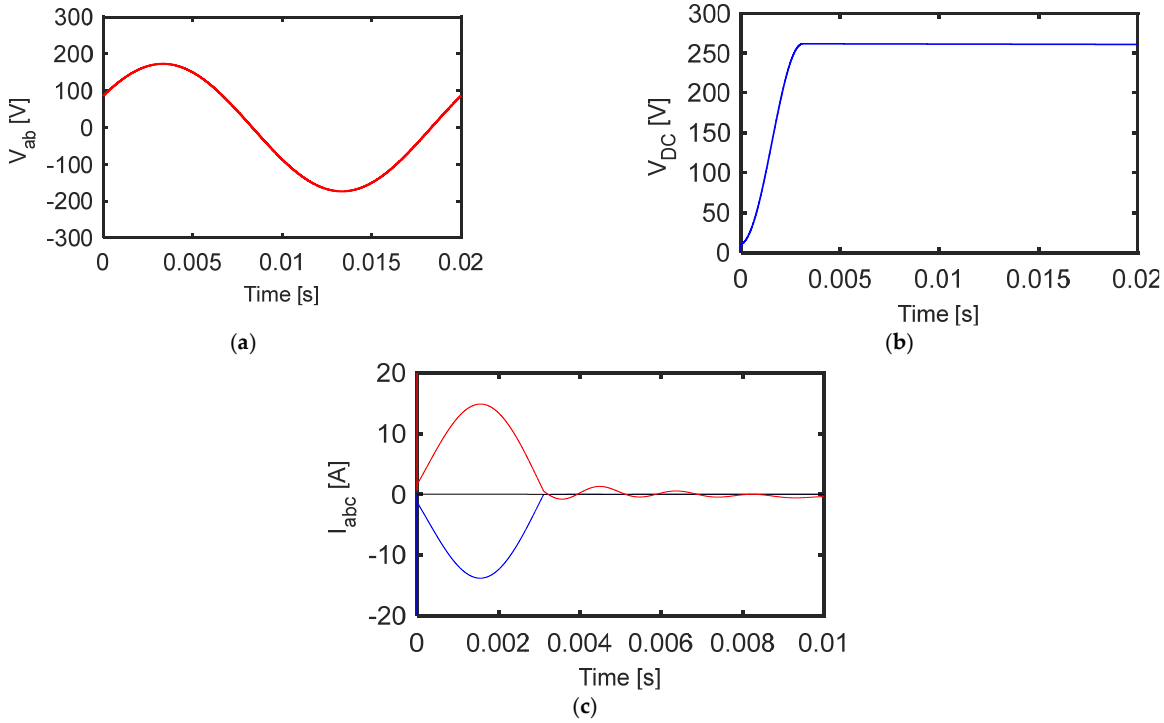
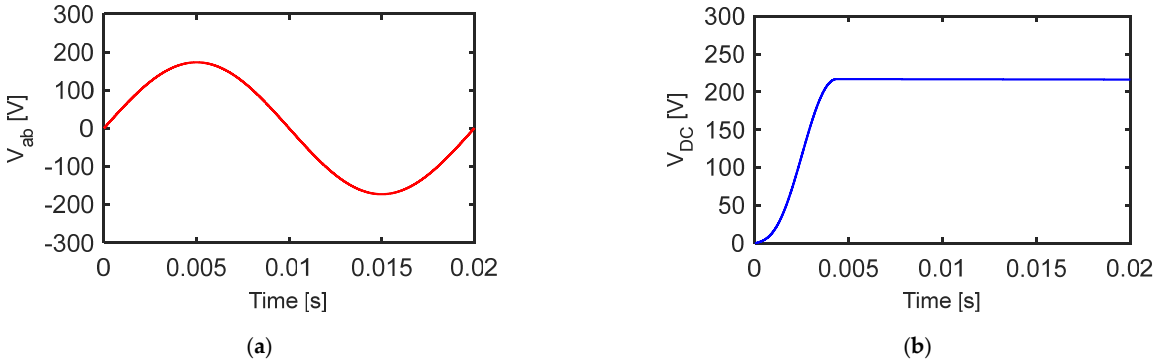
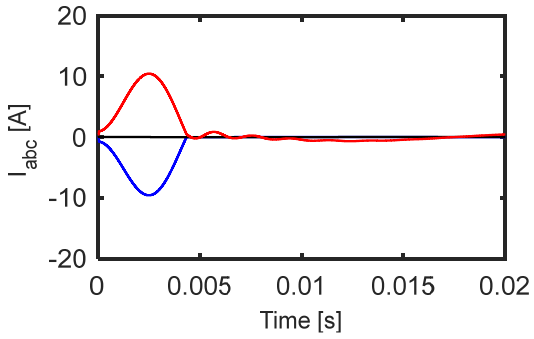


Figure 7. Simulation testing of the clamping circuit at start-up without operating the PWM of the rectifier and charging using line voltage V_{ab} (**a**) Line-input voltage V_{ab}, (**b**) DC-link voltage and (**c**) input current for MC.

Figure 8 shows the simulation results for the testing of the clamping circuit at start-up without operating the PWM of the rectifier and with the capacitor being charged using any line voltage at the instant of zero crossing. The maximum supply current in this case is about 10 A.

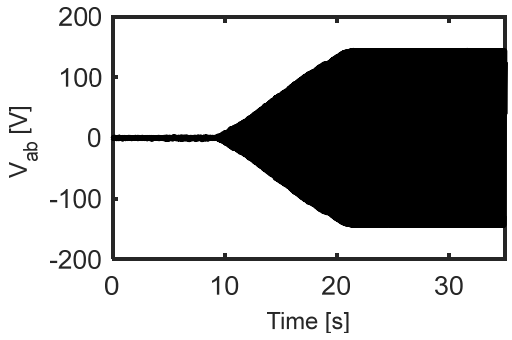




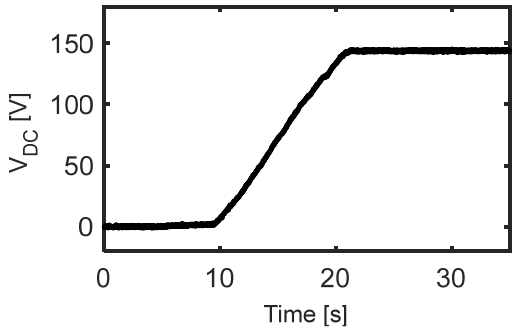
(**c**)

Figure 8. Simulation testing of the clamping circuit at start-up without operating the PWM of the rectifier and charging using line voltage V_{ab} at zero crossing (**a**) Line-input voltage V_{ab}, (**b**) DC-link voltage and (**c**) input current for MC.

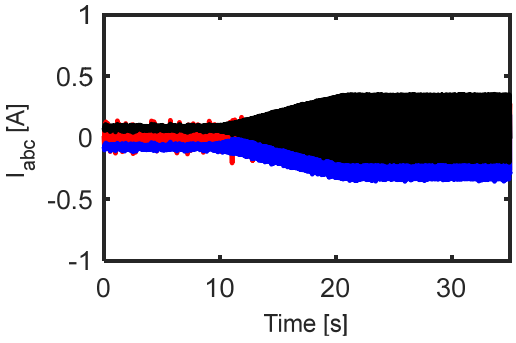
Figure 9 shows the experimental results of testing the clamping circuit at start-up without operating the PWM of the rectifier and charging using the ramp-line voltage V_{ab}. Figure 10 describes the experimental results of testing the clamping circuit at start-up without operating the PWM of the rectifier and charging using the step-input-line voltage V_{ab}. Hence, it is concluded from these figures that the start-up of the proposed MC should consider the following conditions: (1) the PWM of the rectifier stage should be held during the start-up until the capacitor charging finishes and (2) the capacitor charging should be done using any line voltage and this input-line voltage must be smoothly increased from zero up to the operating value.



(**a**)



(**b**)



(**c**)

Figure 9. Experimental testing of the clamping circuit at start-up without operating the PWM of the rectifier and charging using ramp-line voltage V_{ab} (**a**) Line-input voltage V_{ab}, (**b**) DC-link voltage and (**c**) input current for MC.

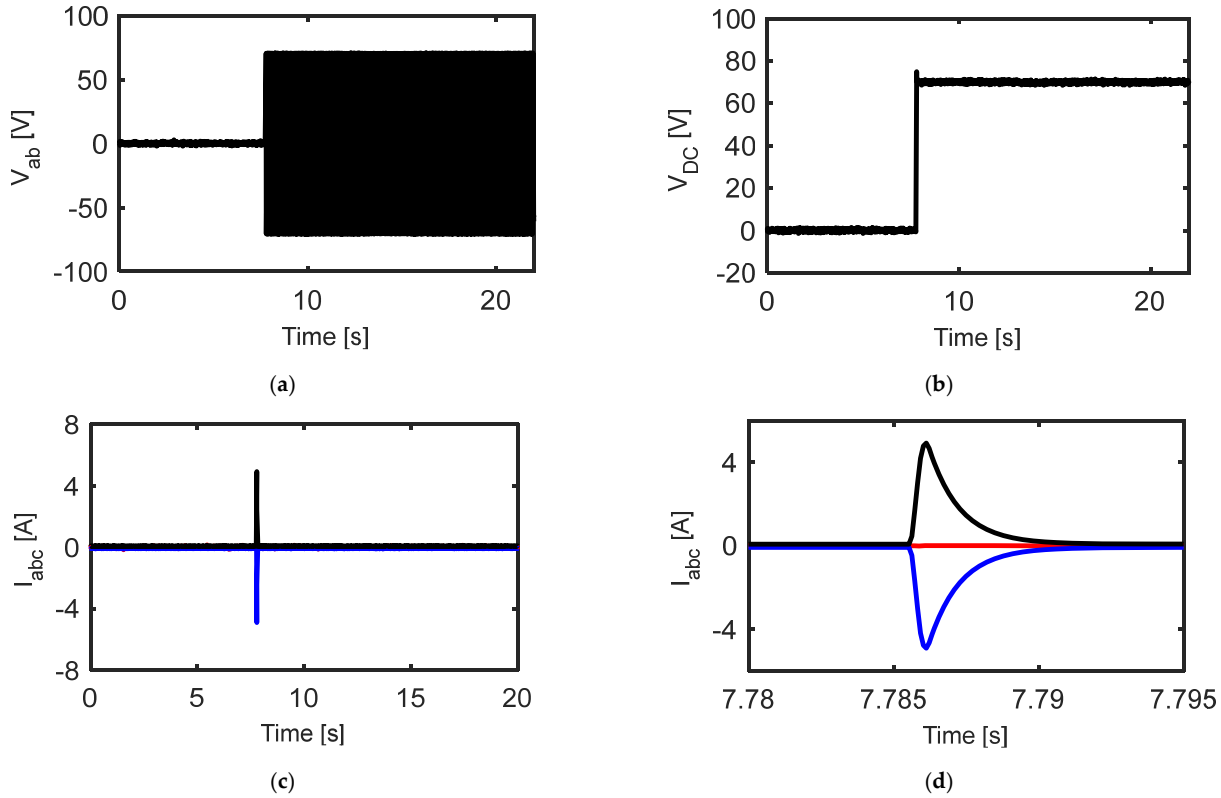


Figure 10. Experimental testing of the clamping circuit at start-up without operating the PWM of the rectifier and charging using step-input-line voltage V_{ab} (**a**) Line-input voltage V_{ab}, (**b**) DC-link voltage, (**c**) input current for MC and (**d**) zoom-in view of the input current at start-up.

3.2. Low-Pass Input Filter

The inductive impact of the power grid should be decreased since MC functions as a current-source-inverter on the input side and a voltage-source-inverter on the output side. A low-pass input filter is used to remove the high-frequency ripple from the waveform of the input current to the IMC. Figure 11 shows the input-filter structure [51]. In Figure 11, R_f, C_f and L_f represent damping resistance, filter capacitance and filter inductance, respectively.

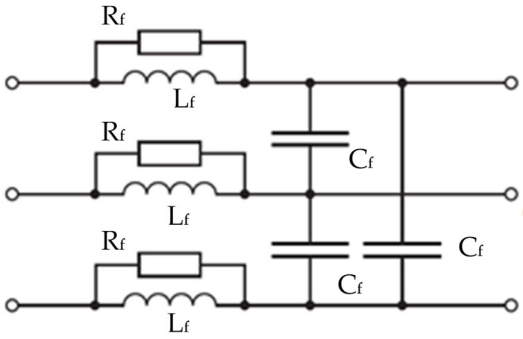


Figure 11. Low-pass input filter.

4. Results and Discussion

This section introduces and analyzes the performance of the indirect MC for both the experimental and simulation results. The three-to-five-phase indirect MC is supplied from a three-phase AC supply of 50 Hz and 100 V peak value. The five-phase output terminals of the indirect MC are connected to a static five-phase *R*–*L* load (R = 82 Ω and L = 10 mH). An LC input filter is connected between the supply and the input terminals of the indirect MC. The input-filter parameters are the following: L_f = 3 mH, R_f = 50 Ω and C_f =10 μF. The clamping circuit consists of a 110 μF capacitor and one ultrafast diode MUR860. The CBPWM is applied in order to control the indirect MC with minimal switching losses in the rectifier stage. The switching frequency is 10 kHz. The sampling times at the simulation and experimental measurements are 1 μs and 100 μs, respectively. The voltage-transfer ratio is chosen as 0.78.

Figure 12 shows the test bench used in the experimental measurements. The MC is controlled to give different output frequencies, e.g., 100 Hz, 50 Hz and 25 Hz. Figures 13 and 14 show the simulation and the experimental results for the MC at 50 Hz of output frequency, respectively. The simulation and experimental results of the DC-link voltage are shown in Figures 13a and 15b, respectively. The input voltage to the MC during the experimental measurements is shown in Figure 15a. There is a great agreement between the measured and the simulated results. Figures 16 and 17 show the simulation and the experimental results for the MC at 100 Hz of output frequency, respectively. Figures 18 and 19 display the simulation and the experimental results for the MC at 25 Hz of output frequency, respectively.

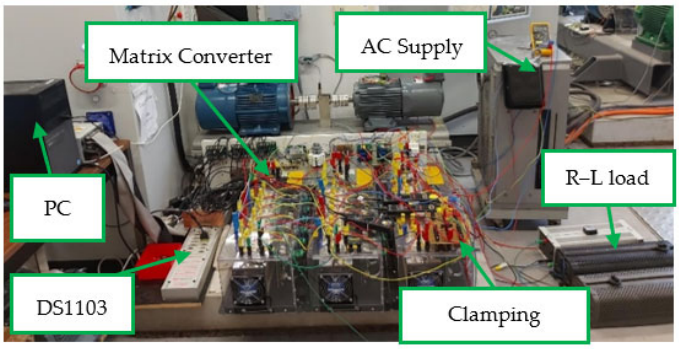
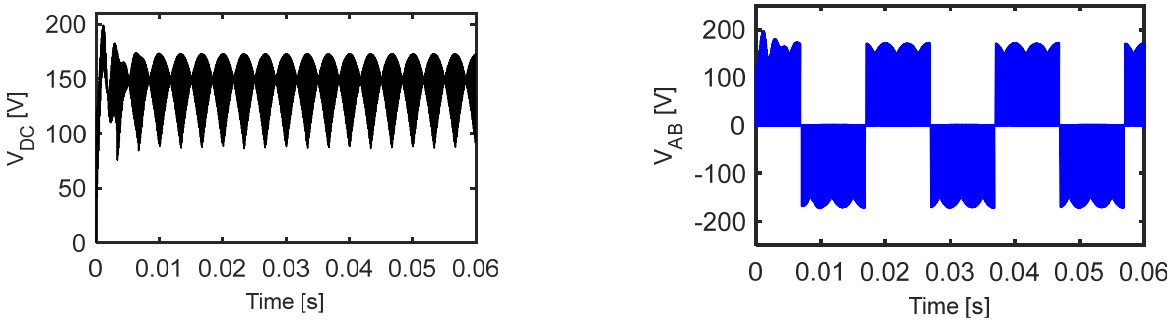
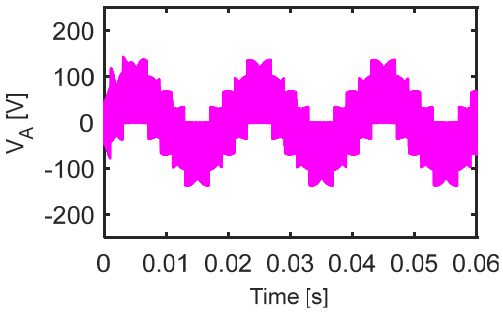
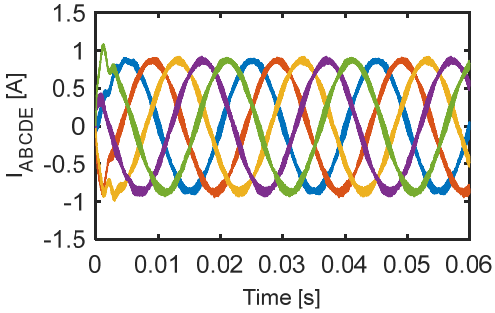


Figure 12. The test bench.



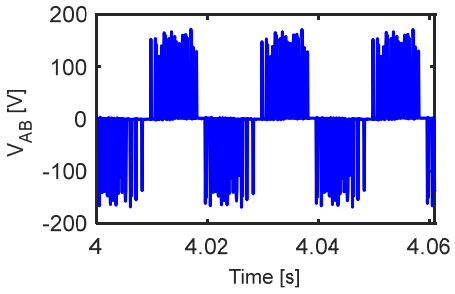


(**c**)

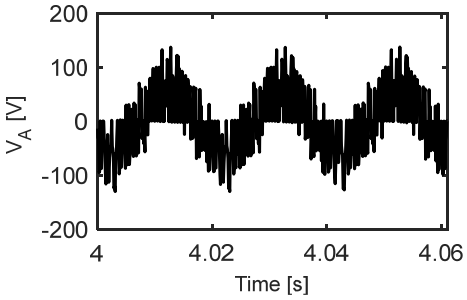


(**d**)

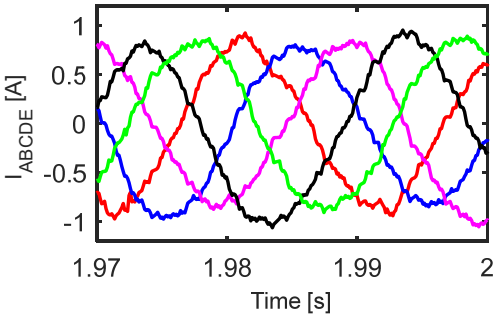
Figure 13. Simulation results at 50 Hz output frequency (**a**) voltage of the DC link, (**b**) output line voltage, (**c**) output phase voltage and (**d**) output phase currents.



(**a**)

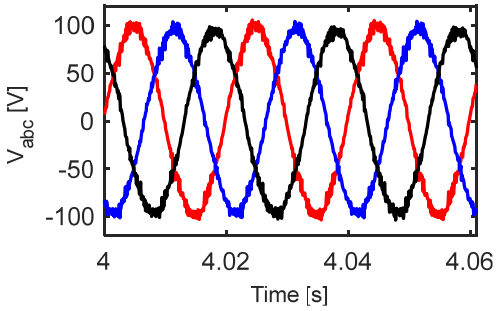


(**b**)

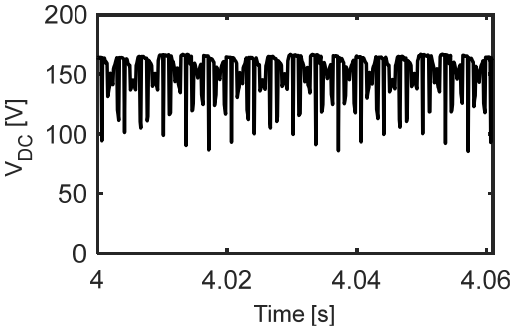


(**c**)

Figure 14. Experimental results at 50 Hz output frequency (**a**) output line voltage, (**b**) output phase voltage and (**c**) output phase currents.



(**a**)



(**b**)

Figure 15. Experimental results (**a**) phase input voltages and (**b**) the voltage of DC link.

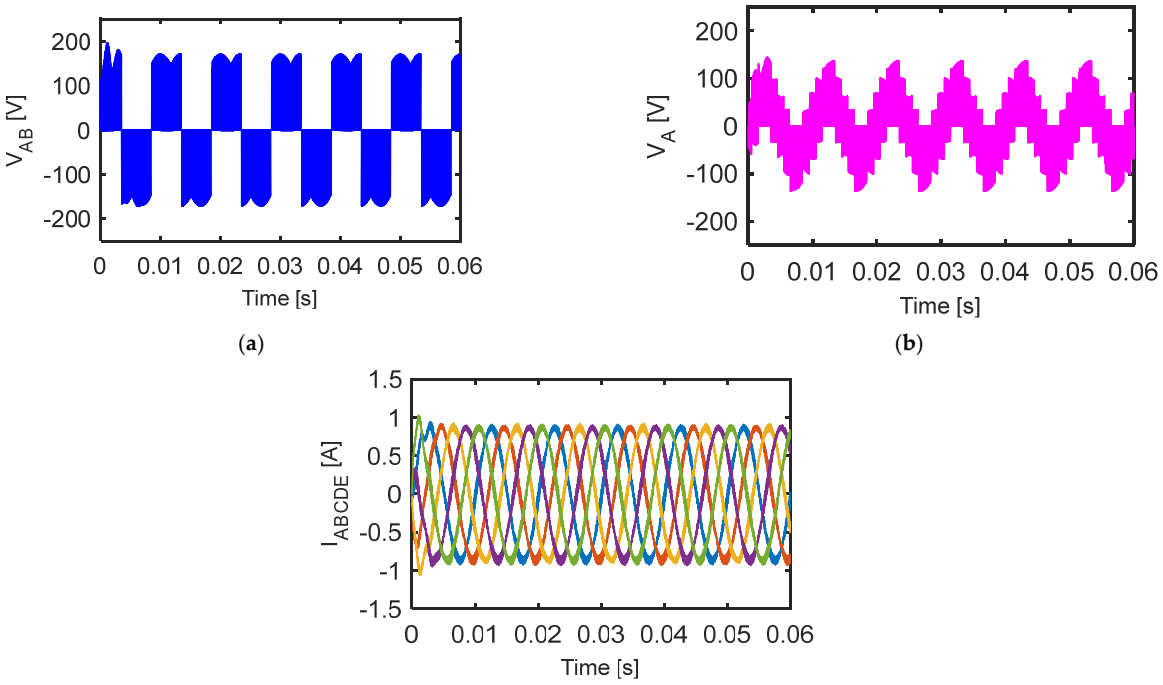


Figure 16. Simulation results at 100 Hz output frequency (**a**) output line voltage, (**b**) output phase voltage and (**c**) output phase currents.

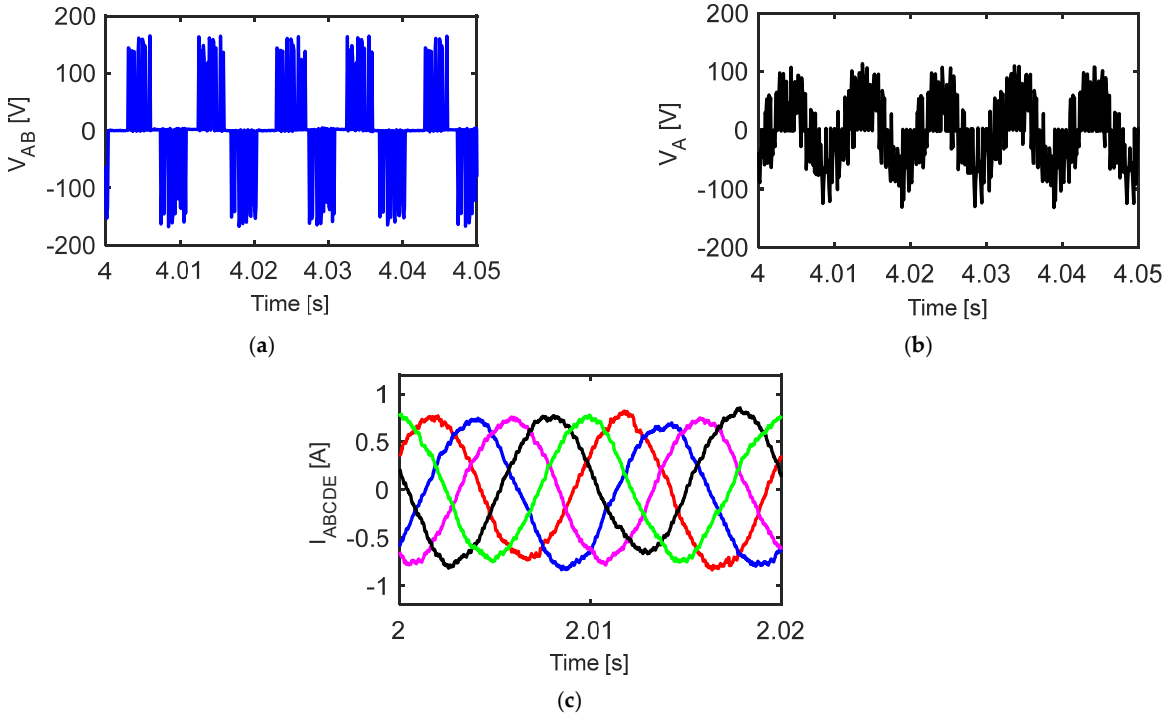


Figure 17. Experimental results at 100 Hz output frequency (**a**) output line voltage, (**b**) output phase voltage and (**c**) output phase currents.

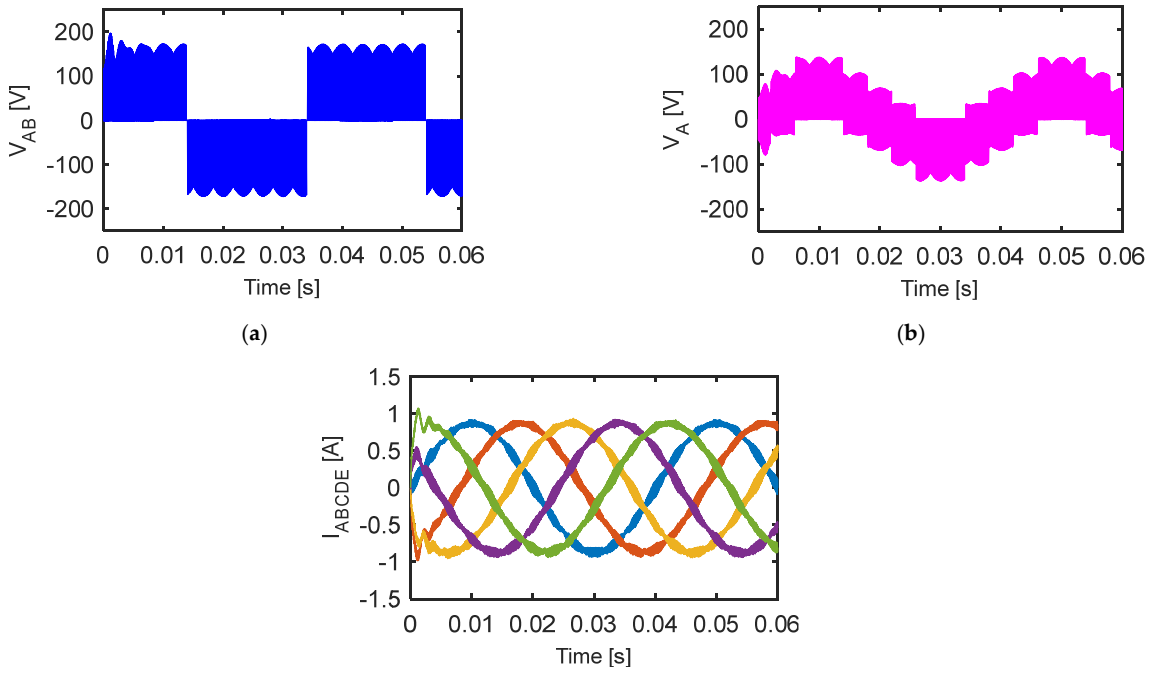


Figure 18. Simulation results at 25 Hz output frequency (**a**) output line voltage, (**b**) output phase voltage and (**c**) output phase currents.

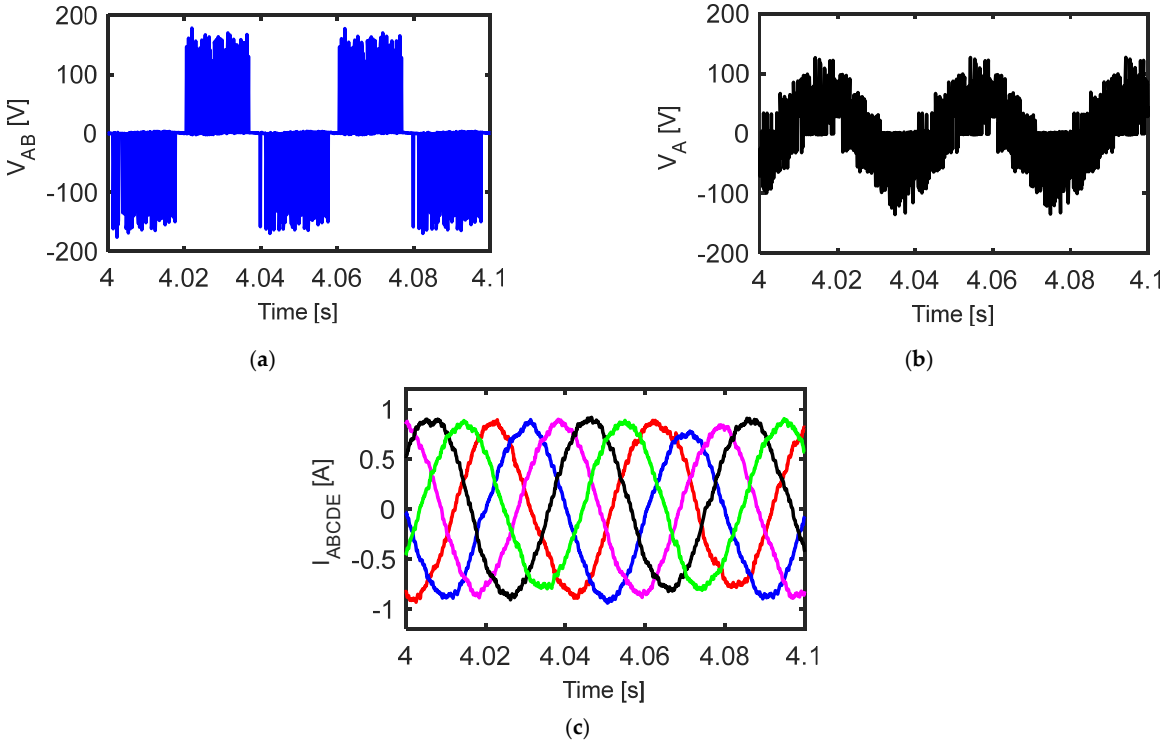


Figure 19. Experimental results at 25 Hz output frequency (**a**) output line voltage, (**b**) output phase voltage and (**c**) output phase currents.

5. Conclusions

In this article, a three-to-five-phase indirect-matrix converter (IMC) with a simple clamp circuit was presented. The suggested converter has the same properties as the three-to-five direct-matrix converter (DMC), despite the fact that the number of semiconductors (IGBTs) was decreased and the commutation procedure was simplified. The IMC has 22 IGBTs compared to 30 IGBTs in the case of the DMC. In addition, a simple clamping circuit with one ultrafast diode and one capacitor was used to protect the switches from overvoltage. A detailed discussion of the issues related to powering up the MC was introduced. Experimental and simulation tests, which had already been performed in order to show these issues and their solutions, was suggested. Moreover, a CBPWM technique appropriate for the introduced three-to-five-phase IMC structure was introduced. The introduced CBPWM technique generates the required PWM pulses for both the rectifier- and inverter-stage controllers using just one symmetrical and triangular carrier signal. Finally, experimental testing with a five-phase static *R–L* load demonstrated the viability of the implemented CBPWM algorithm for the suggested indirect MC.

Author Contributions: Conceptualization, K.B.T.; methodology, K.B.T.; software, K.B.T.; validation, K.B.T.; investigation, K.B.T.; writing—original draft preparation, K.B.T.; writing—review and editing, M.N.I., P.S.; visualization, M.N.I., P.S.; supervision, M.N.I., P.S. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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