A 6-bit 56-GSa/s DAC in 55 nm SiGe BiCMOS

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***Abstract*— We present a 6-bit 56-GSa/s digital-to-analog converter (DAC), implemented in 55 nm SiGe BiCMOS. It consumes 2.36 W of which 0.77 W is utilized in the DAC core. Experiments show an analog 3-dB bandwidth exceeding 28 GHz and an effective number of bits (ENOB) of 3.9. We demonstrate transmission of 112 Gb/s four-level pulse-amplitude modulation (PAM-4) and 168 Gb/s PAM-8 over a channel consisting of an electrical probe and 20 cm RF cables. With pre-equalization compensating the channel loss, we achieve a 0.59 Vpp signal swing.**

Keywords—DAC, BiCMOS, PAM-4, PAM-8

I. Introduction

Next-generation fiber-optic data-center links require higher and higher serial line rates to cope with increasing bandwidth demands. Traditional non-return-to-zero (NRZ) on-off-keying (OOK) has been replaced by multi-level signaling such as four-level pulse-amplitude modulation (PAM-4), doubling the bit rate for a given bandwidth. Nonetheless, PAM-4 modulation schemes are more susceptible to noise, distortion and intersymbol interference, such that equalization is indispensable for signal integrity. Furthermore, optical links employing directly-modulated vertical-cavity surface-emitting lasers (VCSELs) add distortion due to their nonlinearity. As such, high-speed transmitter architectures are migrating towards a combination of digital signal processor (DSP) and digital-to-analog converter (DAC) such that equalization and predistortion can be easily configured and adapted. Existing >50 GSa/s DACs [1]–[7] are often implemented in CMOS, which allows tight co-integration with DSP and other digital signal processing blocks. However, these CMOS DACs are often limited in terms of output swing, in part due to their low supply voltage, and because they often require significant equalization to overcome the bandwidth limitations in the chip itself. On the other hand, implementation in InP [8] allow high-speed transistors and high voltages but prohibit co-integration with digital logic. Finally, SiGe BiCMOS-based DACs [9], [10] provide a middle ground. The availability of CMOS devices enable integration with digital logic, while the high-speed heterojunction bipolar transistors (HBTs) allow high bandwidths. Furthermore, the increased supply voltage ensures larger output swings can be reached.

This paper presents a 6-bit 56-GSa/s DAC in 55 nm SiGe BiCMOS. A maximal output swing of 1 Vpp is realized with an analog 3-dB bandwidth exceeding the Nyquist frequency. The presented DAC architecture yields a piecewise-linear input-to-output transfer, enabling pre-compensation of non-linearities in electro-optical modulators [11].

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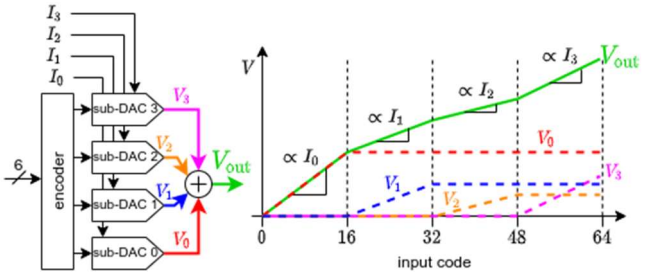


Fig. 1. Piecewise-linear input-output relation obtained by summing four sub-DAC outputs.

II. Design

The piecewise-linear response is obtained by summing the outputs of four sub-DACs, as shown in Fig. 1. Each sub-DAC can generate an output between 0 and 16 times the least significant bit (LSB) step, the size of which is controlled by the corresponding reference current I_k, with $k = 0, 1, 2, 3$. An encoder generates the appropriate input data for each sub-DAC from the binary-coded 6-bit input data. As illustrated in Fig. 1, the reference currents I_k control the LSB step in the corresponding region of the input range. Setting $I_0 = I_1 = I_2 = I_3$ results in conventional linear DAC operation.

The current-steering sub-DACs employ high-speed HBT differential pairs, directing the tail current to either collector. Due to the HBT's large area, however, it is infeasible to have many LSB unit cells. Moreover, the HBT bias current would be much below its optimal point, significantly reducing the switching speed. Instead, binary current scaling is achieved using an R-2R ladder, allowing the use of few unit cells with optimal HBT sizing and biasing, at the cost of a reduced power efficiency. Moreover, because the R-2R ladder is linear, it can be shared between the sub-DACs, summing the currents going into the ladder.

In order to reduce the switching frequency of the unit cells, a 2:1 interleaved architecture is employed, where current multiplexers are placed between two sets of half-rate current steering unit cells and the subsequent R-2R ladder. This approach has the main advantage that a significantly increased settling time is allowed in the unit cells [12], and that the preceding logic runs at a reduced frequency.

The resulting top-level architecture is shown in Fig. 2. All signals are fully differential. Two sets of three input stages [13] convert either 28 GBd PAM-4 or 56 Gb/s NRZ input data to parallel 28 Gb/s streams. This binary coded data then passes through an encoder, driving a 6x4 matrix of current steering unit cells, where each column corresponds to a different sub-

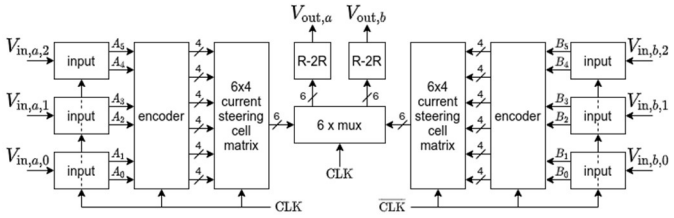


Fig. 2. Top-level block diagram. All signals are fully differential.

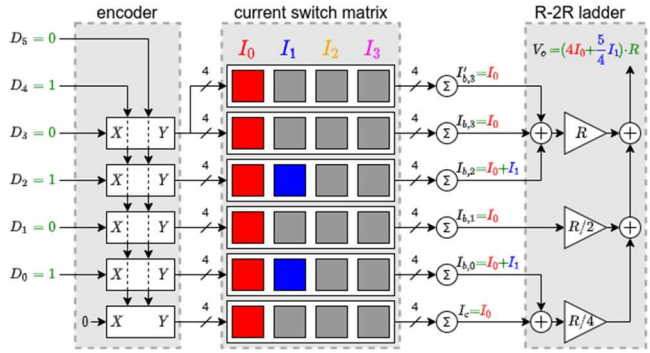


Fig. 3. Block diagram of encoder, current switch matrix and R-2R ladder.

DAC. After multiplexing, the currents are scaled and converted to differential output voltages in R-2R stages.

Each input stage includes an emitter follower input buffer, continuous-time linear equalization (CTLE) and three variable level shifters and slicers and subsequent decoders for extracting the most-significant bit (MSB) and LSB components of the half-rate PAM-4 input signal. Full-rate NRZ OOK is also supported, where the input data is demultiplexed, resulting in two half-rate data streams.

Fig. 3 illustrates the workings of the encoder, 6x4 current steering matrix and R-2R ladder. For clarity, the current mux was omitted, and the response to a binary input 010101 is annotated. The encoder consists of five identical blocks, each having 4 outputs Y_0, Y_1, Y_2, Y_3 controlled by input X and the two most significant input bits D_5 and D_4 as follows:

$$Y_k = \begin{cases} 0, & k > 2 \cdot D_5 + D_4 \\ X, & k = 2 \cdot D_5 + D_4 \\ 1, & k < 2 \cdot D_5 + D_4 \end{cases},$$

where $k = 0, 1, 2, 3$. It is easily verified that this block can be implemented using few logic gates, important due to the high operating frequency. Remark that four of the encoder blocks have their input X driven by the four least significant bits D_3, D_2, D_1, D_0 as inputs, whereas the fifth block has its input $X = 0$. The outputs of each of the five encoder blocks drive a row of current switch unit cells. The total output current of each row is then appropriately scaled in the R-2R ladder. To limit the number of nodes in the R-2R ladder, the encoder block corresponding to D_3 drives two rows of current switches, the total output current of which gets scaled by R. The cells of column k steer a reference current I_k. Thus, the cells of this column generate a combined output voltage between 0 and $4\,I_k R$. From the encoder logic, it follows that the total output is generated by filling the columns from left to right. Thus, the piecewise-linear input-to-output transfer from Fig. 1 is

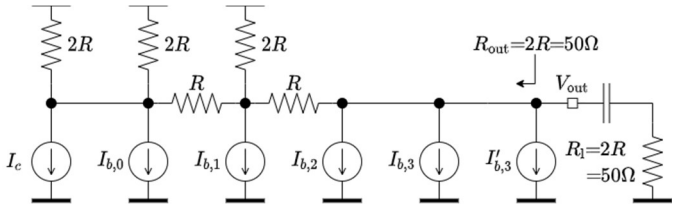


Fig. 4. R-2R ladder for binary current scaling, driving an AC-coupled 50 Ω load.

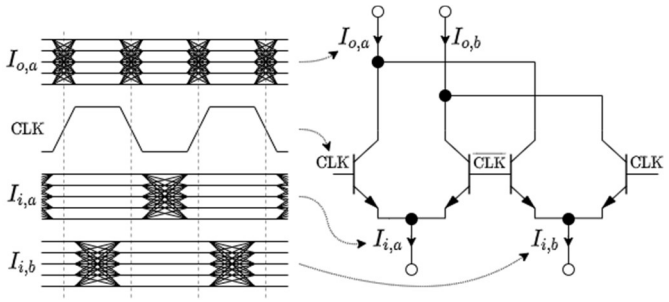


Fig. 5. Current mux circuit with timing of signals annotated.

obtained. The reference currents are controlled via SPI; with $\sum I_k = 5$ mA, the differential output voltage swing is 1 Vpp.

Fig. 4 shows the employed R-2R ladder, with $2R = 50\ \Omega$, resulting in a 50 Ω output impedance. The signal currents I_c, $I_{b,0}$, $I_{b,1}$, $I_{b,2}$, $I_{b,3}$, and $I'_{b,3}$ are the summed outputs of the unit cells of the corresponding row. With a 50 Ω load, they appear at the output voltage with weights $R/4$, $R/4$, $R/2$, R, R, R, respectively. The unit cells corresponding to $I_{b,3}$ and $I'_{b,3}$ are driven by the same input, effectively yielding a weight $2R$. Due to layout parasitics, the signal currents incur different propagation delays to the output. By retiming these signals using appropriately delayed clocks, this effect is largely counteracted. Remark that this ladder is present at both the positive output and the negative output.

The schematic of the current mux is shown in Fig. 5. Driven by a differential clock signal, HBTs are used to steer currents. When the clock is high (low), input currents $I_{i,a}$ and $I_{i,b}$ are directed to outputs $I_{o,a}$ and $I_{o,b}$ ($I_{o,b}$ and $I_{o,a}$), respectively. The timing of the clock relative to the input data is such that output $I_{o,a}$ receives valid data from both inputs, as annotated in Fig. 5. The mux can be disabled by applying a constant high (or low) differential clock input, resulting in dual half-rate DAC functionality. Remark that the current mux acts as a cascode device and, as such, allows high bandwidth summing of the four current switch row outputs. Finally, note that this circuit is duplicated for multiplexing both the positive and negative components of the differential input currents.

III. Experimental Results

The DAC was fabricated in a 55 nm SiGe BiCMOS process and measures 2.0 mm x 1.9 mm. An annotated die photograph is provided in Fig. 6. The full chip consumes 2.36 W from a single 2.5 V supply, with the DAC core (containing current steering matrices, current mux, R-2R ladders and local retiming and clock buffers) consuming 0.77 W, input stages 0.90 W, encoders 0.46 W, and global clock distribution 0.23 W, as illustrated in Fig. 6.

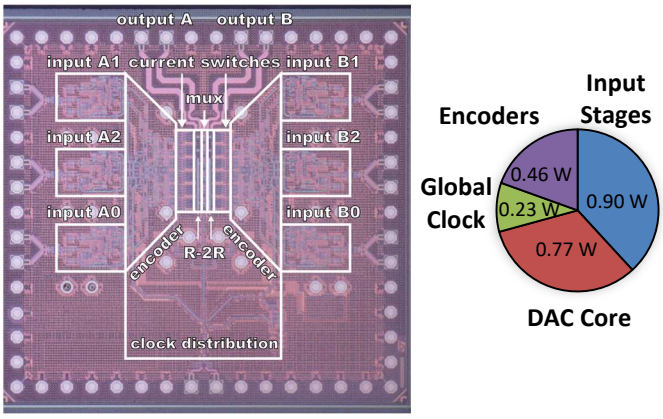


Fig. 6. Annotated die micrograph of the DAC (left) and breakdown of the power consumption, totaling 2.36 W (right).

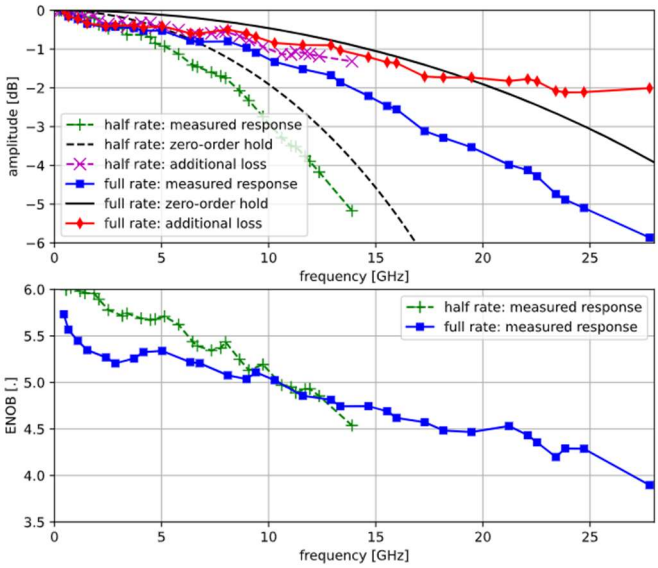
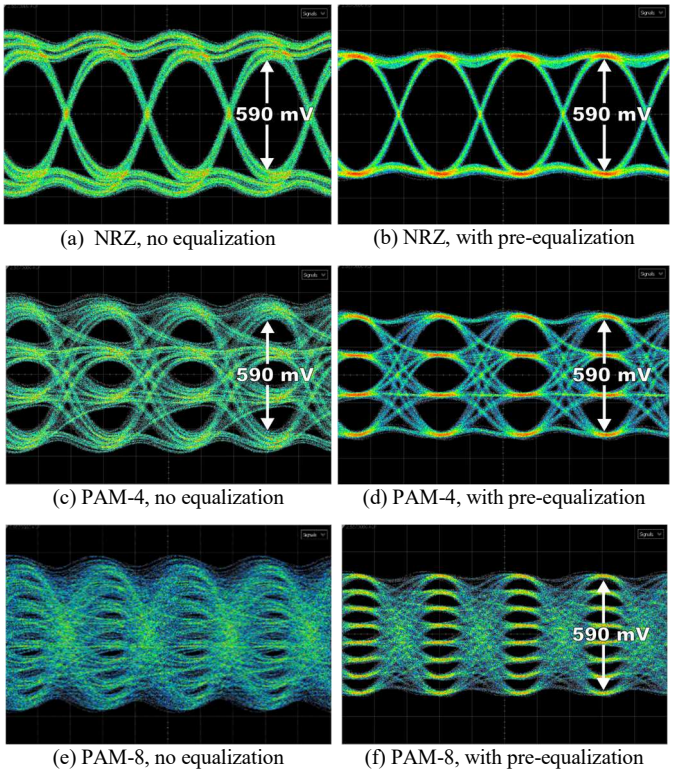


Fig. 7. DAC amplitude response and ENOB versus frequency.

The DAC input data were provided by six AC-coupled PAM-4 signals, generated by a Xilinx FPGA at its maximum rate of 28 GBd, while a bench top clock generator supplied the 28 GHz clock signal. The DAC differential output "A" was probed using a 125 um GSSG probe which incurs a loss of 0.8 dB at 28 GHz. Finally, a pair of 20 cm RF cables and DC blocks connect the probe to the remote heads of a sampling oscilloscope. The loss of the RF cables and DC blocks connecting the probe to the remote heads was measured separately, reaching 1.1 dB at 28 GHz. The DAC reference currents were set to 1.25 mA unless specified otherwise.

Sine waves of various frequencies were generated by the DAC, in both half-rate and full-rate modes. The differential output signal was recorded using a sampling scope at 16 samples per symbol. No averaging was used. After conversion to the frequency domain, the loss of the probe, RF cables and DC blocks was de-embedded. From the resulting spectrum, capped to the Nyquist frequency, the power of the fundamental tone and the effective number of bits (ENOB) were calculated. The resulting frequency response and ENOB are plotted in Fig. 7. The signals undergo zero-order hold pulse shaping

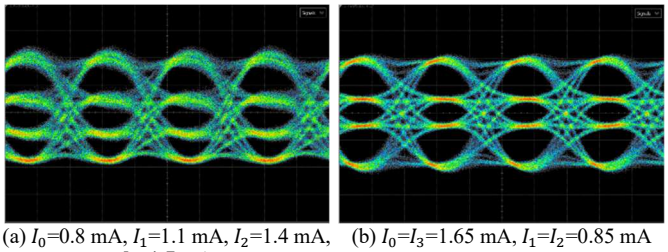


(a) NRZ, no equalization (b) NRZ, with pre-equalization

(c) PAM-4, no equalization (d) PAM-4, with pre-equalization

(e) PAM-8, no equalization (f) PAM-8, with pre-equalization

Fig. 8. Captured 56 GSa/s eye diagrams using NRZ, PAM-4, and PAM-8, both with and without pre-equalization.



(a) I_0=0.8 mA, I_1=1.1 mA, I_2=1.4 mA, I_3=1.7 mA (b) I_0=I_3=1.65 mA, I_1=I_2=0.85 mA

Fig. 9. Captured 56 GSa/s eye diagrams with pre-equalization and non-linear DAC transfer characteristic.

inherent from the DAC operation. Additional loss is incurred due to the finite transition times in the mux and bandwidth limitations of the output network. In the full-rate mode, the loss at 28 GHz reaches 5.9 dB; compared to the zero-order hold response, only an additional 2 dB of loss is incurred: the analog 3 dB bandwidth exceeds the Nyquist frequency. The ENOB reaches a minimum of 3.9 at 28 GHz.

For 56 GBd data transmission measurements, a PRBS9 sequence was mapped to NRZ, PAM-4, or PAM-8. The output was recorded using a sampling oscilloscope. Data was transmitted both with and without pre-equalizing by applying—in software—a 7-tap symbol-spaced feed-forward equalizer (FFE) to the DAC input codes. The resulting eye diagrams are shown in Fig. 8. Note that the loss incurred due to the probe, RF cables and DC blocks, reaching 1.9 dB at 28 GHz, is not de-embedded, and no oscilloscope equalization was employed. Fig. 9 demonstrates the piecewise-linear DAC characteristic applied to equalized 56 GBd PAM-4 signals,

TABLE I.

COMPARISON WITH STATE OF THE ART

		This work		[9]	[10]		[8]	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Technology		55 nm SiGe BiCMOS		130 nm SiGe BiCMOS	55 nm SiGe BiCMOS		0.5 um InP	65 nm CMOS	14 nm FinFET	14 nm FinFET	40 nm CMOS	7 nm FinFET	10 nm FinFET	7 nm FinFET
Sample rate	GSa/s	56		56	100		75	56	64	56	100	56	112	58
Max output swing	V	1		6.7	1		1	0.6	1	-	0.56	1.2	1	1.2
Total (core) power draw	W	2.36 (0.77)		5.2	15		3.4 (0.5)	0.75	0.17	0.286 (0.230)	0.62 (0.205)	0.18 (0.092)	0.423 (0.307)	0.206
Resolution	bit	6		6	6		6	6	-	8	7	7	7	7
Modulation		PAM-4	PAM-8	-	PAM-4	16-QAM[a]	PAM-4	NRZ	PAM-4	PAM-4	NRZ	PAM-4	PAM-4	Duo-PAM4
Bit rate	Gb/s	112	168	-	200	128[a]	150	56	128	112	100	112	224	116
Equalized signal swing	Vpp	0.59	0.59	-	-	-	1[b]	0.4	0.4	0.4	0.073	0.36	0.29	1.23[c]

[a.] Two DACs were used for in-phase and quadrature signal generation.

[b.] No equalization employed.

[c.] Equalized signal swing obtained using de-embedding, the extent to which is not specified.

with Fig. 9 (a) yielding an asymmetrical expansion by setting the reference currents I_0=0.8 mA, I_1=1.1 mA, I_2=1.4 mA, I_3=1.7 mA, whereas Fig. 9 (b) demonstrates symmetrical expansion by setting I_0=I_3=1.65 mA, I_1=I_2=0.85 mA.

Table I compares the presented DAC with the state of the art. In this work, a significant portion of the total power is consumed by the high-speed input stages, a feature that is not included in [1]–[7]. For [3]–[6] we calculate the DAC core power consumption by subtracting the FFE, serializer, and phase-locked loop (PLL) power draw from the total. The presented DAC draws significantly less power than BiCMOS DACs [9] and [10], but has a smaller swing than [9] and lower sample rate than [10]. Our DAC has a core power consumption similar to that of InP DAC [8], but can be co-integrated with DSP. Our work provides an equalized output voltage swing between 1.5x and 8x that of CMOS entries [1]–[6], albeit at a higher power draw. The following must be considered when comparing the equalized signal swings: de-embedding is used in [7], the extent to which is not specified. Packaged DACs [5], [6] incurred loss from the package and PCB trace which [5] partially compensated using oscilloscope equalization whereas [6] employed package loss de-embedding. Due to their higher symbol rate, [4], [6] are more affected by equipment bandwidth limitations. Our results, as well as [1]–[4], [9] were obtained using probes. No oscilloscope equalization or de-embedding was employed in our data transmission experiments.

IV. CONCLUSIONS

We have presented a 6-bit 56-GSa/s DAC implemented in 55 nm SiGe BiCMOS. It consumes 2.36 W from a single 2.5 V supply, of which 0.77 W goes to the DAC core. Experimental results show an ENOB of 3.9, and an analog 3-dB bandwidth exceeding the Nyquist frequency. We demonstrated transmission of 112 Gb/s PAM-4 and 168 Gb/s PAM-8 over a channel consisting of an electrical probe and 20 cm RF cables. With pre-equalization compensating the channel loss, we achieve a 0.59 Vpp signal swing.

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