An IR-UWB IEEE 802.15.4z Compatible Coherent Asynchronous Polar Transmitter in 28-nm CMOS

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***Abstract*— A low-power IEEE 802.15.4z high-rate PHY (HRP) compatible coherent transmitter is described. The proposed transmitter uses a digital polar architecture with fixed amplitude steps in the power amplifier and asynchronous time-discrete pulse shaping. The pulse-shaping unit consists of a finite-impulse response (FIR) filter using current-starved inverter-based delay taps that can be calibrated on-chip. An injection-locked ring oscillator (ILRO)-based frequency synthesis enables wideband operation from 3- to 10-GHz frequency bands. The ILRO also allows for duty-cycled coherent mode operation with 2–4-ns phase locking time and binary phase modulation is applied directly on the oscillator. The on-chip digital front end enables duty cycling (DC) of analog front-end modules with a granularity of 2 ns. Implemented in 28-nm CMOS process, this chip is measured to consume 4.9-mW power in nominal mode with IEEE 802.15.4z high pulse repetition frequency (HPRF) compatible data rate of 6.81 Mb/s compliant with major spectrum mask regulations for channels 5 and 9. With DC of the oscillator enabled in the energy-efficient mode, a power consumption of 430 μW is achieved for packets compatible with legacy pulse-position-modulated IEEE 802.15.4a standard with a data rate of 27.2 Mb/s.**

***Index Terms*— Digital transmitter, IEEE 802154a, IEEE 802154z, impulse radio, localization, polar transmitter, transversal filter, ultra-wideband (UWB).**

I. Introduction

ULTRA-WIDEBAND impulse radios have seen resurgence in popularity due to increased demand for applications requiring spatial awareness, such as secure access, indoor localization, asset tracking, augmented reality (AR)/virtual reality (VR), and gaming. Impulse-radio ultra-wideband (IR-UWB) employing time-of-flight-based ranging is a promising solution for accurate localization [1].

The recently released IR-UWB IEEE 802.15.4z standard mandates coherent mode operation for high-rate PHY (HRP) and enhances the secure ranging operation with a dedicated scrambled timestamp sequence (STS) field in the packet [2]. The use of coherent transceiver improves the link budget of the IR-UWB radio at the cost of additional power dissipation as low-power non-coherent architectures cannot be employed [9]. Furthermore, other low-power IR-UWB transmitter architectures presented in the literature cannot support the coherent modulation requirements of 802.15.4z standard [10], [11]. The IEEE 802.15.4z standard also proposes two new high pulse repetition frequency (HPRF) modes of 124.8 and 249.6 MHz with higher pulse density compared to the legacy standard. The IEEE 802.15.4a/z standards specify channels from 3.5 to 10 GHz (Fig. 1). Transmission in these frequency channels is subject to regional spectral masks regulations [3].

Conventional IR-UWB transmitters use a baseband pulse-shaping filter whose output is upconverted to RF with an IQ mixer and transmitted using a linear power amplifier (PA), as shown in Fig. 2(a). The power dissipation in such transmitters to meet the spectrum mask requirements is high [4], [5]. This limits battery lifetime and, consequently, the applications

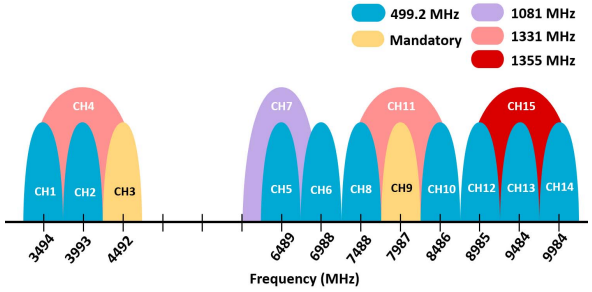

Fig. 1. Channels defined in 802.15.4z standard with bandwidths of 500, 1100, and 1310 MHz.

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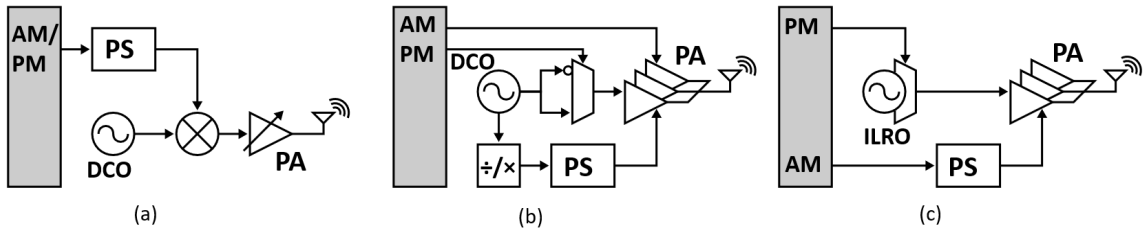

Fig. 2. (a) IQ-upconversion transmitter. (b) Polar transmitter using the LO clock for synchronization. (c) Proposed asynchronous transmitter architecture.

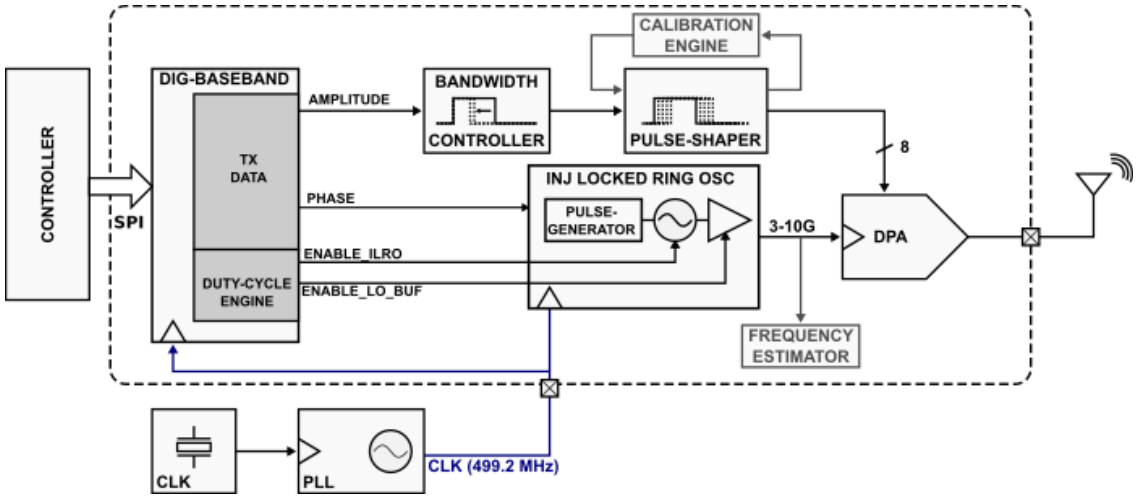

Fig. 3. High-level architecture of the asynchronous polar UWB transmitter IC consisting of a memory-based digital baseband, DC engine, ILRO, pulse shaper, and DPA.

in which IR-UWB can be applied. An alternative solution is to perform the pulse shaping in digital domain and use a polar transmitter by performing a Cartesian to polar transformation. A polar transmitter can employ a non-linear PA leading to high efficiency. However, the Cartesian to polar transformation results in bandwidth expansion, which can result in a clock rate of digital PA (DPA) that is 4–10 times higher than the chip rate resulting in large power dissipation for the overall system. An alternate polar architecture has been proposed in the past where the RF carrier frequency is used as the clock for discretizing the envelope [7]. This is shown in Fig. 2(b) where the digitally controlled oscillator (DCO) output frequency is used as the digital up-sampling clock. The drawback of this approach is that the pulse shape highly depends on the center frequency of the channel.

In this work, we propose an asynchronous polar transmitter employing a pulse shaper that consists of a finite-impulse response (FIR) filter employing current-starved inverter-based delay taps resulting in good power performance tradeoff [see Fig. 2(c)]. The use of an injection-locked ring oscillator (ILRO) for RF carrier generation allows duty cycling (DC) of the DCO and further reduction in power dissipation. The proposed transmitter is compatible with IEEE 802.15.4z standard supporting coherent operation with the lowest power dissipation in the literature known to us. The output spectrum is also compliant with most of regional spectral mask regulations applicable for specific UWB channels.

This article is organized as follows. Section II describes the high-level architecture of the transmitter chip, including an overview of the features of the on-chip digital baseband (DBB). Section III examines the choice of pulse shape and the associated tradeoffs for a power-efficient implementation. Section IV details the key building blocks of the chip. The silicon measurements are discussed in Section V and conclusions provided in Section VI.

II. Asynchronous Polar Transmitter Architecture

The architecture of the proposed asynchronous polar transmitter integrated circuit (IC) is shown in Fig. 3. An on-chip DBB generates phase and amplitude signals clocked at 499.2 MHz feeding the analog transmitter chain. The analog transmit chain consists of a bandwidth controller, which tunes the pulsewidth of the incoming pulse (nominally 2 ns). This is followed by a pulse shaper, which feeds an 8-bit one-hot signal to the DPA. An injection-locked ring oscillator generates the RF carrier and locks to an externally generated 499.2-MHz base clock frequency. The chip includes knobs to support software-based calibration of the ring oscillator frequency as well as the delay taps used in the pulse-shaper block. The chip can be controlled and observed by an external microcontroller over SPI interface.

A. Digital Baseband (DBB)

The DBB consists of a playback memory unit that can store complete IEEE 802.15.4z/4a compatible packets in a compressed format in an on-chip memory. During a packet

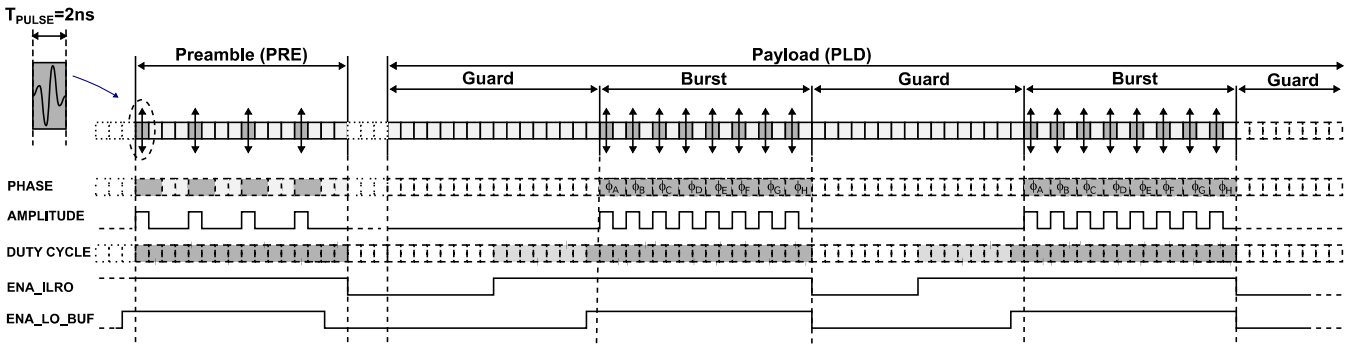

Fig. 4. Timing diagram of preamble and payload parts of 802.15.4z packet with PRF of 124.8 MHz. The DBB outputs phase and amplitude signals along with the enable signals for ILRO and LO buffer on a 2-ns timing grid to control the analog front end.

transmission, the DBB outputs a 2-bit code at 499.2 MHz representing amplitude and phase of the chips needed for binary phase shift keying (BPSK) coded signals. Fig. 4 shows the phase and amplitude signals for a preamble and payload for IEEE 802.15.4z HPRF mode with a 124.8-MHz pulse repetition frequency (PRF). In this mode, each payload bursts consists of alternate chips with a zero and non-zero amplitude. It should also be noted that as shown in Section III, the RF pulse at the output of the transmitter during the payload burst must be longer than 2 ns to meet the spectrum requirements. This is achieved in the analog front end in pulse-shaper block. For correct operation, the phase must not change, while a pulse is being transmitted. Therefore, the phase bit set during a chip with non-zero amplitude is held constant in the subsequent chip if this subsequent chip has a zero amplitude (Fig. 4).

Along with the amplitude and phase data bits, the DBB also outputs synchronized enable signals for the ILRO, buffers, and PA, which can each be independently controlled with a resolution of 2 ns. This allows DC of each analog block to optimize the overall power dissipation. An example of this shown in Fig. 4, where the ring oscillator is enabled with ENA_ILRO signal eight clock cycles (16 ns) before the beginning of the burst to allow the frequency to settle, while the buffer is enabled just one clock cycle before the burst.

B. Analog Front End

This transmitter IC supports 500 MHz as well as higher bandwidth channels specified in IEEE 802.15.4z HRP. The support for channels wider than nominal 500-MHz bandwidth is enabled by bandwidth-controller block shown in Fig. 5. The incoming 2-ns square pulse is shrunk to 1 ns or less and a rectangular output pulse is fed to the pulse-shaper block. Higher transmitter bandwidth in the transmitter can enable improved ranging performance [10].

The pulse-shaper block consists of an FIR filter with eight delay taps. A bus of eight output signals from the pulse shaper is fed to the DPA. The sum of this bus represents the envelope of the output RF signal. The ILRO block generates the RF carrier by locking the phase of a digitally controlled ring oscillator (DCRO) to a reference 499.2-MHz clock. This reference clock is supplied externally with an on-chip clock buffer.

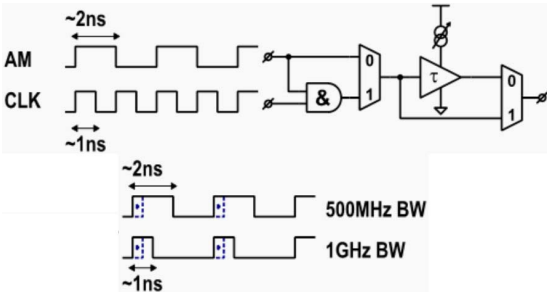

Fig. 5. Conceptual diagram of the bandwidth-controller block.

This pulse-shaper output signals are mixed with the RF carrier in the switched-capacitor-based DPA block. The switched-capacitor implementation allows for summation of pulse-shaper output bus in charge domain to create the desired envelope of the output RF signal to the antenna.

C. On-Chip Pulse-Shaper Calibration

To avoid the possibility of incorrect harmonic locking of the ILRO, the open-loop frequency of DCRO must theoretically be within 25% of the reference clock frequency to the target carrier frequency [13], [14]. Moreover, for the reference spurs due to injection locking to be lower than −40 dBc, the open-loop DCO frequency must be within 5 MHz of the target frequency [15]. Therefore, an on-chip frequency-estimation circuit is employed to calibrate the DCRO frequency.

The pulse shaper, which consists of several delay taps, suffers from variations in process, temperature, or other environmental conditions. An on-chip calibration technique is proposed for the delay chain in the pulse-shaper block to calibrate the delays to be within the desired range (detailed in Section IV-B).

III. Pulse Shape Analysis

The shape of the pulse in an IR-UWB radio is crucial for ranging as well as for the frequency spectrum of the output to meet the regulatory masks. It can be noted that channels 5 and 9, centered at 6489.6 and 7987.2 MHz can be used in many regions worldwide. However, the regulatory masks pose strict requirements of approximately −29-dBc suppression of any sidelobes close to the main lobe. The use

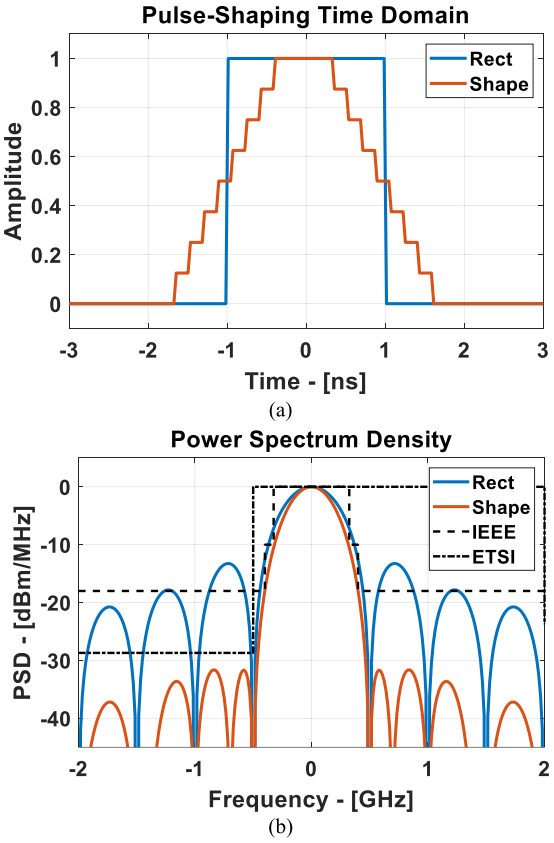

Fig. 6. (a) Triangular and rectangular pulse shapes in time domain. (b) Normalized close-in frequency spectrum of the corresponding pulse shapes centered with respect to channel 5 (6489.6 MHz) plotted with a normalized ETSI spectrum mask.

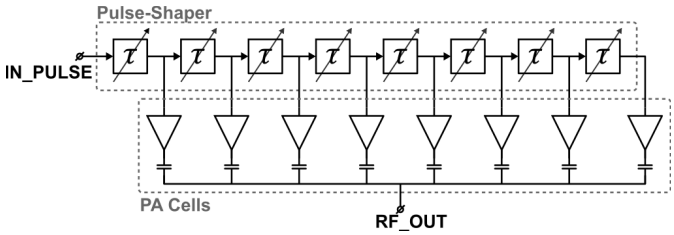

Fig. 7. Conceptual block diagram of the pulse shaping using tunable analog delay cells and switched capacitor PA cells for summation of the delay cell outputs.

of an analog delay line in the FIR filter-based pulse-shaping block allows a power-efficient design while keeping the circuit complexity low.

A. Pulse Shape

The rectangular pulse shape from the DBB does not have good spectral properties as the sidelobes violate most of the regulatory masks (Fig. 6). A study of pulse shapes with certain constraints has been discussed in [16]. These include triangular, trapezoidal, and other window-shaped pulses. In this analysis, we narrow down the search space to a trapezoidal pulse shape as it allows an energy-efficient design while meeting the regulatory masks for most regions. An major advantage of using trapezoidal pulses is that the desired pulse shape can be generated by a simple summation of outputs of

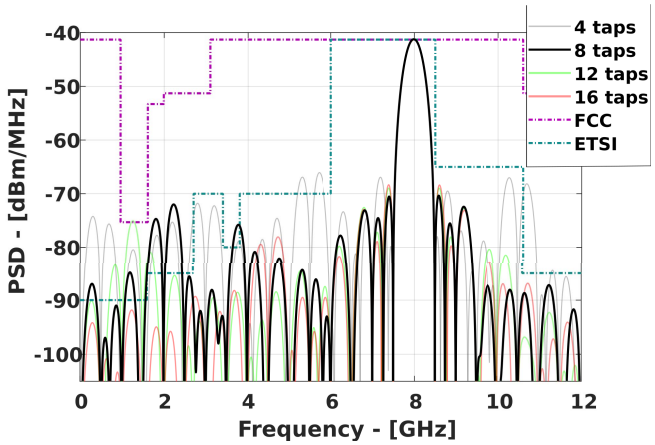

Fig. 8. Frequency spectrum of the pulse with a different number of taps in pulse-shaper delay line.

all the delay taps. The circuit implementation consists of delay taps and switched-capacitor PA cells that summate the output of the filter in charge domain to create the pulse (Fig. 7).

B. Pulse Quantization

A higher number of delay taps result in lower quantization noise and cleaner frequency spectrum at the expense of higher power dissipation.

Fig. 8 shows the simulated output spectrum as a function of number of delay taps. Although 16 taps result in cleaner spectrum far out from the main lobe, eight taps are sufficient to meet most of the regional spectrum mask regulations for channel 9. The sidelobes at frequencies lower than 4 GHz can easily be filtered by the antenna without requiring additional components, as discussed in Section V.

In this design, we use eight delay taps each connected to a PA cell that is a good tradeoff between spectral purity and design complexity. Each delay tap shifts the incoming pulse by an equal amount of time.

C. Sensitivity to Variation

A potential drawback to the proposed approach using asynchronous pulse-shaping approach is the variation in analog delay cells causing the pulse shape and consequently the output to degrade. Fig. 9 shows a plot with sensitivity analysis with 10% random normal variation in the delay of cells in the pulse-shaper block. It should be noted that the close-in sidelobes are not degraded significantly by mismatch. The variation in far-out sidelobes can be intuitively understood as the delay cells changes have a direct impact on the frequency of the aliases of the spectrum far from the center frequency. The 10% variation simulated in the delay taps implies that there is sufficient margin in the proposed design with eight delay taps to meet the regulatory spectrum mask requirements.

IV. Transmitter Circuit Design

A. Injection Locked Ring Oscillator

Fig. 10 shows the ILRO featuring a pseudo differential DCRO with a frequency operation range of 3–10 GHz.

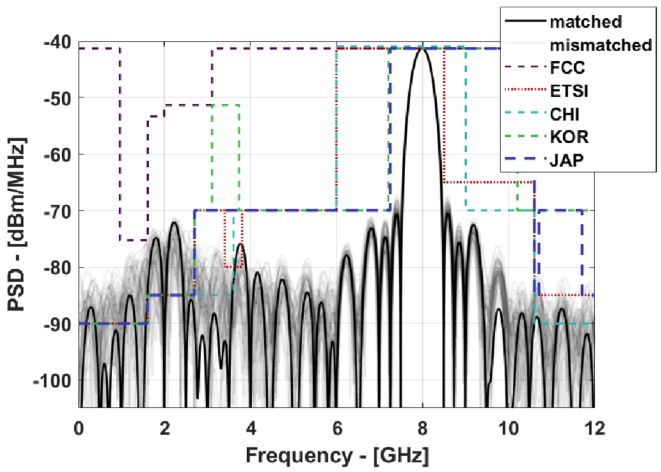

Fig. 9. Output spectrum variations due to random mismatch with standard deviation of 10% between the eight delay cells.

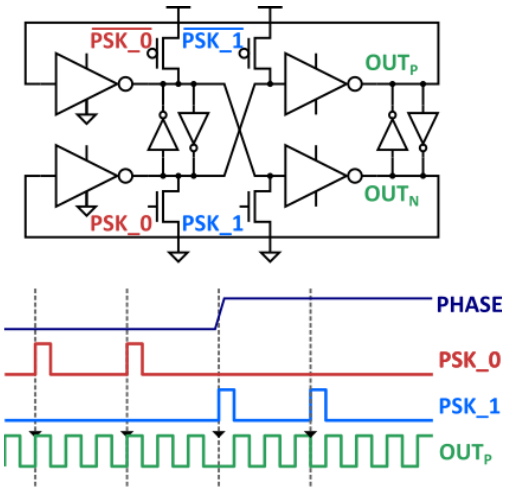

Fig. 10. ILRO circuit with BPSK implemented by reversing the polarity of injection.

The low quality factor of a DCRO allows for fast startup. The DCRO consists of four current-starved inverters and its frequency is tuned by the means of a digitally controlled current digital-to-analog converter (DAC). Before injection locking, the free-running frequency of the DCRO is checked to be calibrated to within 5 MHz of the target frequency using the frequency estimation. If the DCRO is not within this range, a calibration is performed with a software-controlled frequency-locked loop (FLL) using an on-chip frequency-estimation unit. This frequency-estimation unit consists of a counter that measures the number of LO edges in a pre-defined measurement period. The FLL enabled when first using the chip and it is subsequently only needed in case of large frequency drift due to, for instance, temperature drift. A single-frequency estimation takes <1 μs and is a power-efficient way to indicate when frequency drifts greater than the desired limits and an FLL-based calibration is needed.

In the injection-locking mode, the phase of RF carrier in the DCRO is periodically realigned with a clean reference clock edge to suppress the long-term noise from the DCRO as the noise of the DCRO is effectively high-pass-filtered [17], [18]. This feedforward phase-locking technique allows instantaneous phase locking with frequency locked to the intended integer multiple of 499.2-MHz reference clock. The instantaneous phase injection property is exploited for BPSK modulation by direct injection of opposite polarity to the injection nodes of the ILRO, as shown in Fig. 10 [19]. The instantaneous phase locking also enables DC of the ILRO while maintaining coherent mode operation. In this transmitter IC, an option to duty cycle the ILRO and other analog blocks with granularity of a single chip period (2 ns) is implemented. The ILRO and the LO buffer can be enabled/disabled with independent scheduling to optimize power dissipation for any packet configuration. Phase lock of the ILRO can be achieved within 16 ns, including the frequency settling time of the DCRO. Therefore, the ILRO is enabled eight clock cycles before the pulse or burst (Fig. 4).

B. Pulse-Shaping Circuits

The implementation of asynchronous pulse shaper and its interface with the PA is detailed in Fig. 11. The width of the rectangular amplitude pulse is tuned in the bandwidth controller and fed into a seven-tap delay-line-based pulse shaper. Unlike the prior-art synchronous polar techniques [6]–[9], this approach does not rely on the timing grid of the RF carrier. The delay elements of the pulse shaper are implemented using current-starved buffers whose unit delay τ is programmable by a 4-bit bias current control. This approach lends itself to a compact physical layout of the pulse shaper and PA where the pulse-shaper units can fit close to the PA cells.

An on-chip calibration is scheduled when the transmitter is inactive to account for voltage or temperature variations in the pulse shaper. In this calibration mode, the output of the delay line is fed back to its input converting through a multiplexer converting it into a ring oscillator. A frequency measurement unit is used to measure and calibrate the unit delay τ by optimizing the pulse-shaper current bias setting. The ability to calibrate the delay taps enables optimization of pulse shape for spectral purity independent of the LO frequency and enables the transmitter to operate in high-bandwidth modes (>1 GHz).

C. Power Amplifier

The eight output signals of the pulse shaper are used to enable respective switched-capacitor PA cells (Fig. 11). Each of these cells consists of four unit cells configurable with 2 bits of output power control to meet the power spectral density (PSD) requirement of -41.3 dBm/MHz for different PRFs.

The use of switched-capacitor class-D PA unit cells allows for summation of the pulse-shaper outputs in charge domain. However, this structure has a disadvantage in an impulse radio that the common-mode voltage at the output of this PA cell also follows the output pulses, resulting in larger than permitted frequency content at low frequencies close to dc. Adding a tristate mode to the class-D PA cell when no pulse is being transmitted and pre-biasing the output node to the desired common-mode level using a high-bandwidth amplifier

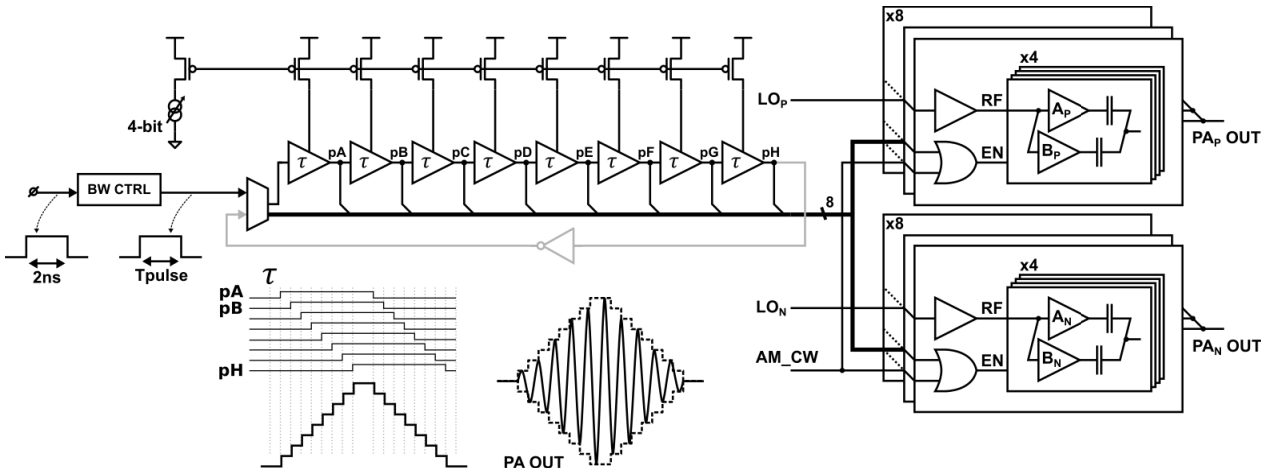

Fig. 11. Pulse-shaping chain includes a bandwidth control block that is used to tune the pulsewidth followed by eight-step pulse-shaping block feeding dual-capacitively coupled PA cells with 2-bit power control.

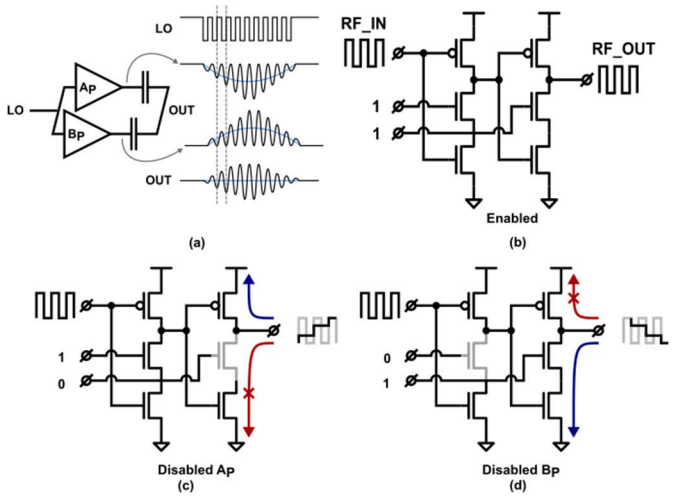

Fig. 12. (a) Balanced dual capacitively coupled PA cell. (b) Dynamic PA unit cell when enabled. (c) Built-in pull-up logic when disabled for A type unit cell. (d) Built-in pull-down logic when disabled for B type unit cell.

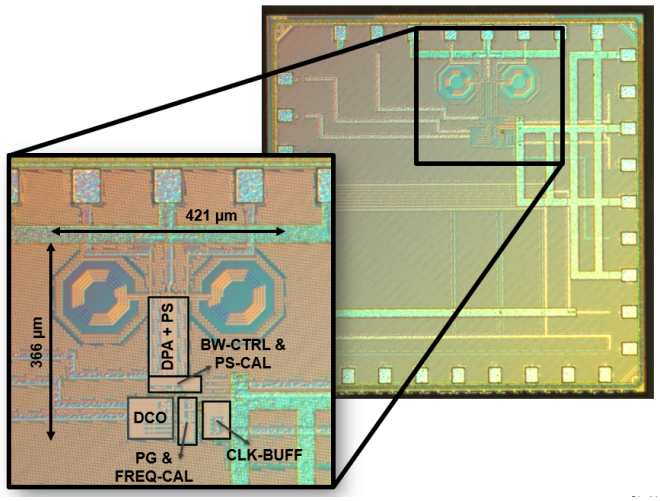

Fig. 13. Chip micrograph of the UWB transmitter IC with an active area of AFE of 0.11 mm^2.

was proposed by de Streel *et al.* [7]. An alternate approach proposed in [9] is to use a dual-capacitively coupled PA where two PAs cells with tri-state mode are coupled together. When the PA is not transmitting a pulse, the outputs of the two PAs are pulled toward supply and ground with respective switches. The combined output common mode of the overall PA remains close to mid-rail independent of the modulation. This approach is shown to improve the spectrum at low frequencies (close to dc). However, this circuit requires large transistor switches to set the common mode, which must be turned on and off periodically.

In this work, we propose a different approach of implementing the dual-capacitively coupled PA architecture with each PA cell consisting of two units A_P and B_P with opposite common-mode polarity when disabled (Fig. 12). This results in the output of PA cell being centered around mid-rail similar to [9] without need for large switches to set the common mode of the PA cell. A unit-capacitor size of 160 fF is used in this PA design, which results in small charge/discharge time relative to a pulse duration.

V. Measurement Results

The chip is implemented in 28-nm CMOS with an active analog front-end area of 0.154 mm^2 (Fig. 13) and measured with a supply voltage of 0.9 V. The chip is tested in two different modes: 1) a nominal mode that is compatible with 802.15.4z packets without DC of the ILRO and 2) an efficient mode where the ILRO is duty-cycled while still being compatible with the 802.15.4a standard.

Fig. 14 shows the time-domain plots of 802.15.4z preamble and payload in nominal mode. The 802.15.4z payload shown here has a PRF of 124.8 MHz. The individual pulses are of approximately 4-ns duration for both preamble and payload pulses. In this mode during payload, a chip with zero amplitude between active chips allows the pulses to return-to-zero during phase transition.

We demonstrate an efficient mode operation with DC of DCRO while maintaining coherence. Fig. 15 shows the demodulated amplitude and phase for part of preamble of 802.15.4a with. In this mode, the pulses in the preamble

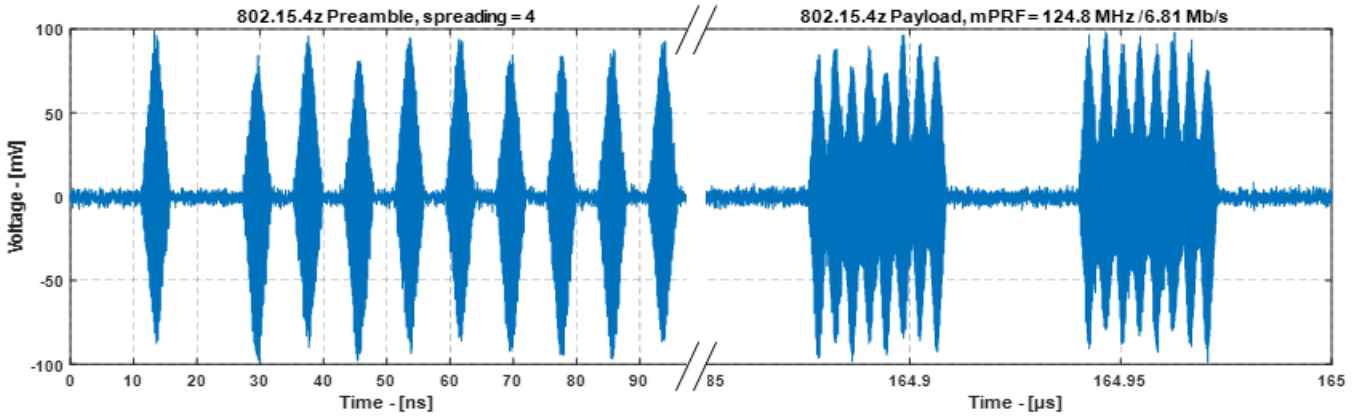

Fig. 14. Time-domain waveforms showing the pulses in 802.15.4z preamble and payload mode. It should be noted that the time divisions in the plots for preamble are smaller than payload section.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work		[4] Decawave DW3000	[5] Decawave DW1000	[6] Liu, RFIC'18	[7] de Streel, JSSC'17	[9] Mercier, JSSC'09
	Nominal mode	Efficient mode					
Process (nm)	28		40	90	22	28 (FDSOI)	90
Supply (V)	0.9		N.A.	N.A.	0.7	1.2/0.55/ ±1.8	1
Die area (mm ^{2})	0.154		N.A.	N.A.	0.085	0.095	0.07
LO freq. (GHz)	3 – 10		6.5, 8	3.5 – 6.5	6.5 – 8	3.5 – 4.5	2.1 – 5.7
BPSK Modulation	Yes					NO	
IEEE standard	802.15.4z / 4a	802.15.4a	802.15.4z	802.15.4a	802.15.4a	802.15.4a	802.15.4a
DCO Duty cycling	No	Yes	No	No	N.A.	N.A.	N.A.
UWB indoor regulations	FCC/ETSI/ KCC/JPY/CHI	FCC/ETSI	FCC/ETSI/ KCC/JPY/CHI	FCC / ETSI	FCC	FCC	FCC
Sidelobe PSD (dBr) @500MHz offset	-28*, -32**	-19	-28†	-30 ~ -33†	-11~-13†	-20 ~ - 22†	-20 ~ -22 †
Mod. BW (GHz)	0.5, 1		0.5, 1	0.5, 1	0.5	0.5	0.5
Data rate (Mb/s)	6.81	0.11, 0.85, 1.7, 6.81, 27.24	0.85, 6.81	0.11, 0.85, 6.81	0.11	0.11, 0.85, 1.7, 6.81, 27.24	15.6
LO RMS jitter (ps)	0.34 ††		N.A.	N.A.	9	N.A.	N.A.
CW TX P_{OUT}(dBm)	-2.5*, -0.7**		N.A.	N.A.	-1	N.A.	2.5
Active power (µW)	4900 ††	435 ††	83800	168300	300	380 (SoC: 650)	4360
E_{VDD}/bit (pJ/bit) @Datarate	720 @6.8 Mb/s	16 @27.2 Mb/s	12305 @6.8Mb/s	24700 @6.8Mb/s	2700 @0.11Mb/s	14 (24 SoC) @27.2Mb/s	280 @15.6 Mb/s
Avg E_{OUT}/pulse (pJ) $^{\#}$	1.12*, 1.7**		N.A.	N.A.	1.58	0.62	1.12
E_{VDD}/pulse (pJ/pulse) @PRF	39.5 @124.8 MHz	27 @15.6 MHz	197 @62.4 MHz	395 @62.4MHz	170 @15.6 MHz	24 @15.6 MHz	280 @15.6 MHz
TX Efficiency $^{\#\#}$	4.3%	6.2%			0.9%	2.5%	0.4%

* Channel 9, ** Channel 5, † Estimated from the figures in documentation, †† Reference clock (499.2MHz) from external source,
$^{\#}$ Approximated based on bandwidth of 500 MHz, $^{\#\#}$ Tx Efficiency=(E_{OUT}/pulse)/(E_{VDD}/pulse)

symbol are spread by 128 ns and the ILRO is enabled only 16 ns before the pulse, which is sufficient for frequency settling and injection locking of the phase. LO buffer and PA are enabled only 2 ns before the pulse is transmitted to further optimize the power dissipation. The demodulated phase plot shows correctly demodulated BPSK code. This underlines the benefit of injection locking for DC of the DCRO for use in a coherent receiver.

The on-chip calibration of pulse shape is done by converting the delay line into a ring oscillator and measuring its frequency. The resulting delay as measured with on-chip digital circuitry is shown in Fig. 16(a) as a function of 4-bit control.

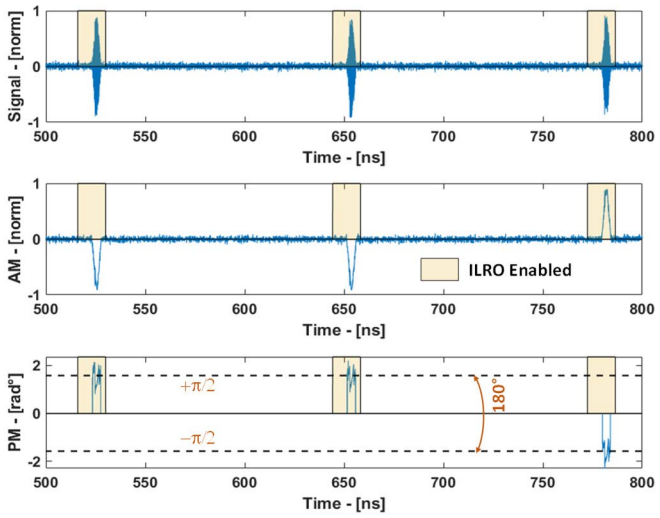

Fig. 15. Demodulated amplitude and phase with DC of the ILRO enabled 16 ns before the beginning of the pulse with BPSK with injection.

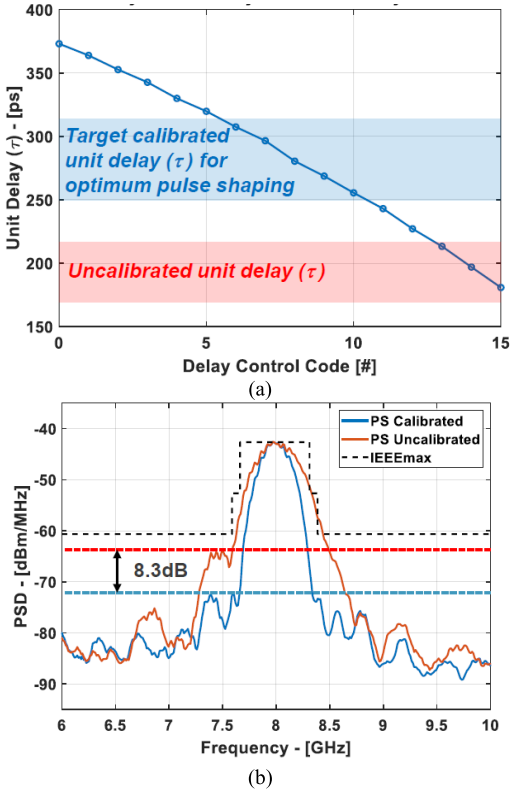

Fig. 16. (a) Measured unit delay of delay taps in the pulse shaper as a function of 4-bit code. (b) Result of calibration.

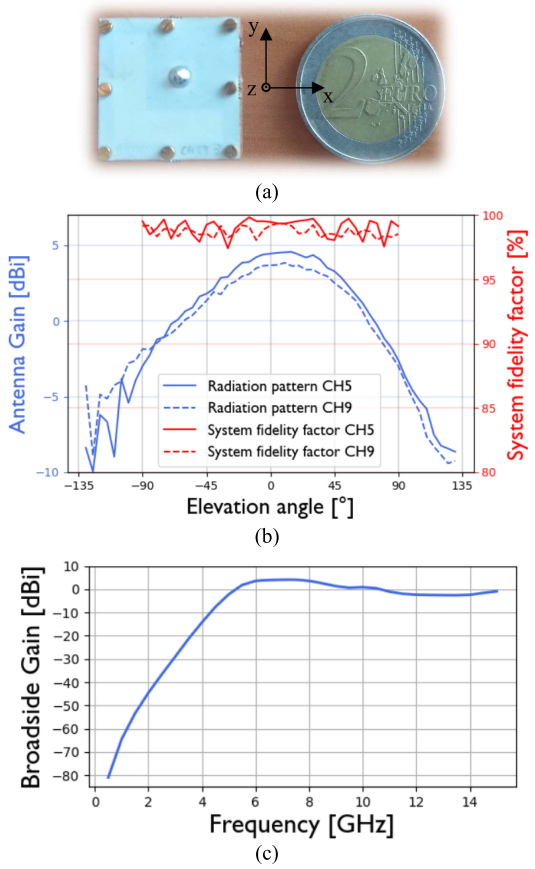

Fig. 17. (a) Dual-band quarter-mode cavity-backed AFSIW antenna. (b) Measured radiation pattern and SFF for channels 5 and 9 in the *XZ* plane. (c) Antenna gain as a function of frequency.

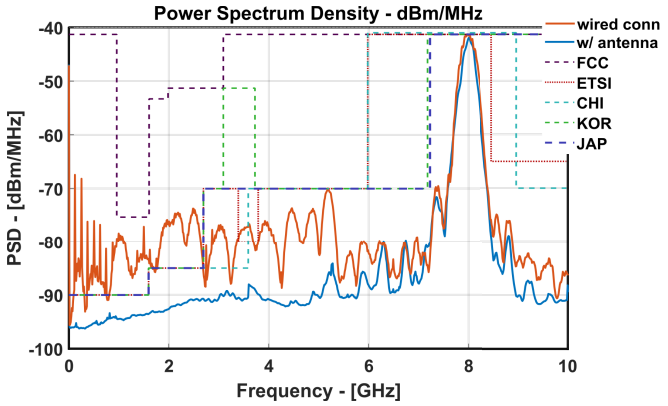

Fig. 18. Measured output spectrum of the transmitter set to channel 9 with wired connection and with antenna.

Fig. 16(b) shows the resulting spectrum with calibrated and un-calibrated settings of the pulse shape. The delay line can be calibrated as discussed in Section IV-C and allows the first sidelobe close to the main lobe to be lowered by 8.3 dB. The on-chip calibration proposed in this work does not need measurement of the spectrum to calibrate the pulse shape.

Channels 1, 5, 9, and 14 are 500-MHz bandwidth with pulse-shaper calibration, as shown in Fig. 16. The bandwidth controller and pulse-shaper blocks are set in high-bandwidth mode for measurement of channels 4, 7, and 11. The frequency spectrum measurements show compliance with FCC mask, except for some artifacts measured between 1 and 2 GHz, which can easily be filtered by an antenna or an off-chip filter.

To exploit the compactness and power efficiency of the IR-UWB transmitter, a quarter-mode cavity-backed slot antenna is implemented in air-filled substrate-integrated-waveguide (AFSIW) technology [Fig. 17(a)]. The AFSIW technology allows a very high radiation efficiency over a wide bandwidth while remaining compatible with standard printed

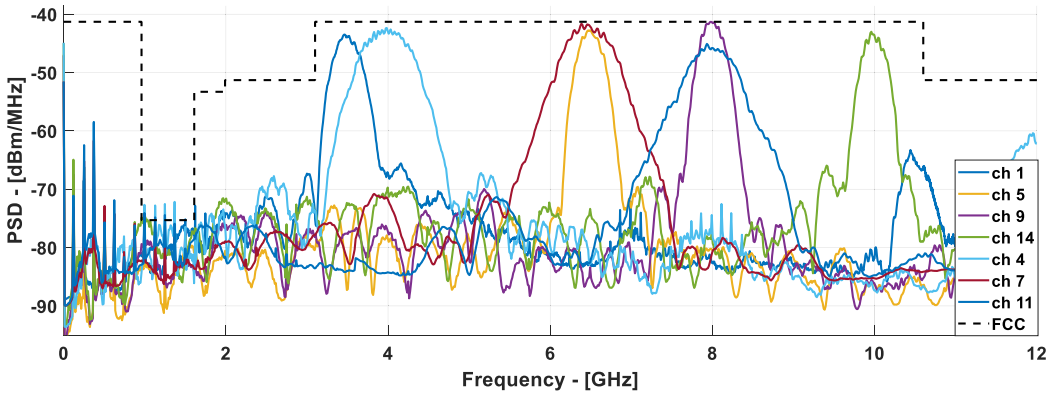

Fig. 19. Measured output spectrum for selected 500-MHz channels—channels 1, 5, 9 and 14—and high-bandwidth channels—channels 4, 7, and 11—along with FCC regulatory mask. The measurements are done with a spectrum analyzer setup as specified by FCC regulations.

circuit board (PCB) technology [20]. Quarter-mode miniaturization is then leveraged to reduce the footprint by a factor four [21]. The proposed antenna covers both channels 5 and 9 with a radiation efficiency over 90% in each channel, within a footprint of 18 mm $\times$ 18 mm. Moreover, through rigorous optimization in the frequency domain and on a system level, a large half-power beamwidth (HPBW) in both channels is obtained in which pulse distortion is minimized by maximizing the system fidelity factor (SFF) [22]. Fig. 17(b) shows the measured radiation pattern at the center frequency of both channels, along with the measured SFF. An HPBW of 110° is obtained in both channels, with a peak gain of 4.8 dBi in channel 5 and 3.9 dBi in channel 9. An SFF larger than 95 % is achieved indicating minimal pulse distortion. Finally, Fig. 17(c) shows the broadside gain of the antenna as a function of frequency, demonstrating stable antenna gain within channels 5 and 9, and a 20-dB attenuation at frequencies below 4 GHz filtering the transmitter output spectrum at low frequencies.

UWB transmission in channel 9, centered at 7.9872 GHz, is allowed by most spectrum regulations worldwide. The EIRP generally permitted for this channel is -41.3 dBm/MHz. The transmitter described in this article can transmit a continuous wave (CW) tone at a peak output power of -2.5 dBm (and -0.7 dBm) at the UWB channel 9 (and channel 5). When transmitting over a 500-MHz-wide channel, this peak output power translates to a PSD of -29.3 dBm/MHz. The HPRF mode of 124.8 MHz specified in 802.15.4z standard is four times lower than the chip rate of 499.2 MHz. The maximum PSD supported by this chip in 124.8-MHz PRF mode is -33.8 and -35.6 dBm/MHz for channels 5 and 9, respectively. The PA output power can be tuned in steps of $\sim$3 dB to meet the spectrum regulations. In addition, the PRFs of 62.4, 15.6, and 3.9 MHz are also supported by the transmitter with maximum PSD proportionally lower with respect to the 124.8-MHz PRF mode.

The measured spectrum of the transmitter IC for channel 9 centered at 8 GHz is shown in Fig. 18 with wired and wireless connection. The measured spectrum with wired connection shows some of the artifacts violating some regulatory masks below 4 GHz. However, as discussed earlier, these are filtered

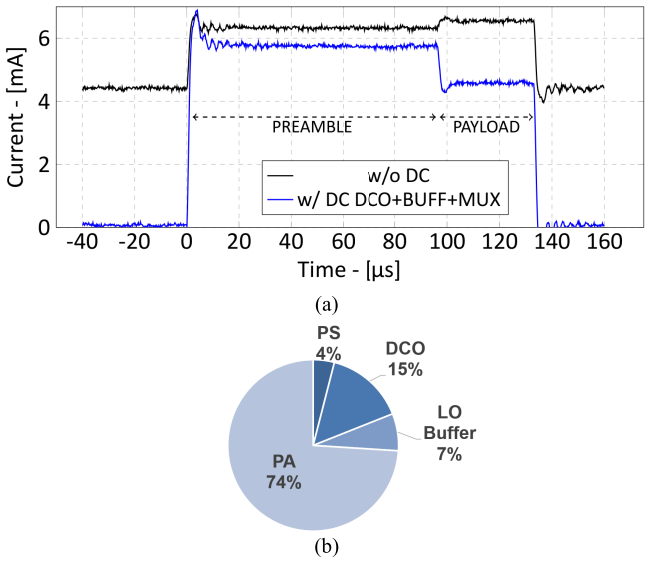

Fig. 20. (a) Current consumed during packet transmission with and without DC. (b) Power distribution in various blocks of the transmitter with duty-cycle disabled.

by the antenna without need for other external components and the measurement with antenna is compliant with all major regulatory masks. Fig. 19 shows the overlayed measured results for selected UWB channels between 3 and 10 GHz as specified in [2]. This shows compliance with FCC mask for all the channels except for the clock spurs of the 125-MHz on-chip digital clock. These low-frequency artifacts can be filtered by an off-chip filter or by the antenna. Fig. 20 shows the power dissipation breakdown of the transmitter. In the nominal mode, the majority of the power is consumed by the PA. The performance of this work in nominal and efficient transmitter mode is summarized and compared with the state of the art in Table I.

VI. Conclusion

This article presents an asynchronous polar transmitter compatible with IEEE 802.15.4z standard supporting coherent channels 5 and 9. The IC fabricated in TSMC 28-nm CMOS technology occupies an active area of 0.154 mm^2. With asyn-

chronous pulse-shaping and fine-grained DC, this chip demonstrates the lowest power 802.15.4z compatible transmitter and with minimal power overhead compared to previously reported 802.15.4a transmitters.

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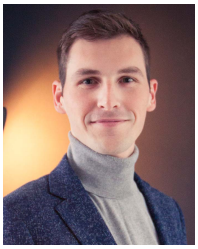

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