

A 4-to-1 240 Gb/s PAM-4 MUX with a 7-tap Mixed-Signal FFE in 55nm BiCMOS

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Next generation high-speed wireline and optical communications will target single lane data rates over 200Gb/s. For this, the generation and transmission of >100Gbaud PAM-4 is a key step. Recent transmitters in advanced CMOS and FinFET nodes [1,2] provide extensive transmit-side FFE capabilities at respectively 64 and 56Gbaud. Speed limitations in these technologies will make the transition to >100Gbaud a challenge. Alternatively, InP-based multiplexers like [3] manage to reach >100Gbaud easily. They also offer the possibility to create high-swing output drivers, necessary to efficiently drive optical modulators. However, InP solutions lack the ability to introduce more complex equalization of the signal. BiCMOS based transmitters like in [4], enable the integration of more complex circuits with respect to InP technologies, are capable to deliver high signal swings required for optical drivers and promise increased bandwidth compared to CMOS/FinFET. This paper presents a 120Gbaud PAM-4 TX incorporating a 7-tap FFE in a 55nm BiCMOS technology. The advantage of the presented FFE architecture is the efficient use of both digital and analog delay structures to obtain >100Gbaud operation with a large amount of filter taps in a compact configuration.

The TX architecture incorporating a 4:1 PAM-4 MUX and 7-tap FFE is shown in Fig 1. It accepts four input signals, processed by input decoders to obtain the MSB and LSB components. After retiming using two 90 degree out of phase quarter-rate clocks (CLK/2 and CLK/2 90°), the 4 MSB and 4 LSB signals are separately multiplexed and filtered using a 7-tap FFE (MUX-FFE) resulting in 2 independent 7-tap FFEs, one for the MSB and one for the LSB. The two quarter-rate clocks are derived from an externally supplied half-rate clock (CLK) which is divided on-chip. Using phase interpolators (PI), the phases of both quarter-rate clocks can be fine-tuned. The filtered MSB and LSB signals are combined in the output stage to obtain a full-rate PAM-4 signal. An output driver amplifies the PAM-4 signal to drive a 100Ω differential load. The four PAM-4 levels are created by scaling the overall gain in the separate FFEs.

Fig.2 provides the block diagram of the input decoder. It can operate in a quarter-rate PAM-4 mode or a half-rate NRZ mode. An emitter follower (EF) input buffer is followed by a CTLE, providing tunable peaking around 16GHz in PAM-4 mode and 28GHz in NRZ mode. Decoding the PAM-4 signal is done via 3 variable level shifters (LS) and slicers (S_1 , S_2 and S_3) to convert the PAM-4 signal into 3 bit streams D_{up} , D_{mid} and D_{low} . The sliced signals are decoded further with optional gray decoding to extract the MSB and LSB component. In the NRZ mode, only the middle slicer (S_2) is used and the half-rate signal is demultiplexed to obtain two quarter-rate bit streams D_{mid} and $D_{mid,180}$. All decoding is performed using quarter-rate logic. To monitor the performance of the input decoders, an additional subsampler is added, operating at 1/128th -rate.

Fig. 3 provides the core 7-tap MUX-FFE architecture alongside the important analog and digital circuits. The filter architecture resembles the structure of a travelling wave FIR filter [4] to which additional cross amplifiers are added (h_1, h_2, h_4, h_5). The architecture allows that each of the delay values is equal to (a multiple of) the tap spacing, unlike conventional analog travelling wave FIR filters, where each delay element must have a physical value that is only a fraction of the tap spacing. This allows efficient implementation of the input delay line in the digital domain while maintaining a distributed analog summation at the output. This reduces loading such that a high bandwidth can be obtained. The generation of 2 bit digital delays at full rate ($= 2T_s$) is performed by delaying the retimed quarter rate signals using high-speed latches. A two stage 4:1 MUX topology is implemented based on a half-rate clock. Shunt inductive peaking is added in the second MUX-stage to enhance the bandwidth. The filter coefficients are represented by analog variable gain amplifiers (VGAs), implemented by 2 parallel differential pairs (Q_{v0} - Q_{v1} and Q_{v2} - Q_{v3}) with variable tail currents, controlled by a 7-bit differential DAC

(with outputs $I_0 + a$ and $I_0 - a$, I_0 the nominal bias current and " a " defining the gain setting). To save area, compact analog delay cells are used instead of passive delay lines. The active analog delay circuit is formed by the summation of 2 signal paths followed by an EF. A first path is formed by a normal differential pair (Q_{d0} - Q_{d3}). The second path is formed by a cascoded differential pair (Q_{d1} - Q_{d2}) with double gain that is connected with the inverse sign to the output. The emitter of the cascodes (Q_{d4} - Q_{d5}) are loaded with an additional capacitance. In this way, a right half plane zero is introduced, providing both bandwidth peaking and increased delay. The summation of both signal paths is combined with the summation of the different VGA signals, provided via separate cascode transistors (Q_{d6} - Q_{d7}), in a single resistive load R_{sum} with shunt inductive peaking to increase the bandwidth at the summation node. A fixed analog delay around 8.3ps is obtained with a summation bandwidth >83GHz.

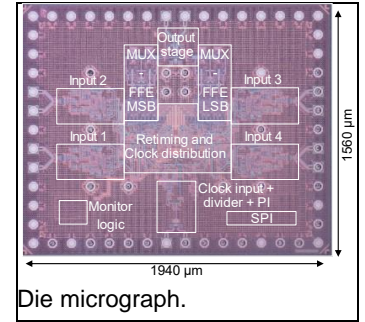
The architecture of the output stage is given in Fig.4. The equalized MSB and LSB components are pre-amplified by separate emitter degenerated differential pairs and summed together in a shared load $R_{sum,pre}$. The pre-drivers are followed by an EF and 100Ω differential output driver with cross-coupled compensation capacitors and series/shunt inductors to compensate for the pad and ESD parasitic capacitance and bump parasitic inductance. The output stage has a maximum differential output swing of 1.2Vpp when generating PAM-4 signals. A single filter tap (only MSB component) can provide up to 300mVpp swing. Hence, up to 8.5dB of overshoot can be introduced in the filter without having to lower the DC gain.

The chip is fabricated in a 55nm BiCMOS technology and flip-chipped on a high-speed PCB. The output is connected via a 2cm differential trace, a 1.8mm connector, 10cm RF-coaxial cable and DC blocking capacitors to the sampling heads of a 100GHz sampling oscilloscope. This leads to a total added loss of 8dB at 60GHz. A bench-top clock source is used to generate the half-rate clock (CLK) with a maximum frequency of 60GHz. A 92GS/s AWG generates the quarter-rate PAM-4 or half-rate NRZ signals. By using an SPI-interface, on-chip settings such as FFE coefficients can be set and monitoring information can be read. Using a single 2.5V supply, the TX consumes 2W when the input decoders are configured for NRZ and 2.16W when configured to decode PAM-4. From this power, approximately 680mW is consumed in the analog part (VGAs, delay circuits and output stage), 300mW in the MUX and retiming, and 560mW for clock distribution. The chip measures 3.03mm².

In Fig. 5, the measured PRBS15 NRZ (MSB only) and PAM-4 eye-diagrams at respectively 100,112 and 120Gbaud are shown after optimization of the MSB and LSB FFE coefficients. The filters are optimized to reach a peak-to-peak voltage at the scope input of 500mVpp for the PAM-4 signals (measured at the center of the upper and lower noise band) in all three cases. The measured level separation mismatch ratio (RLM) is > 98.3%, close to the ideal 100%, for all cases. The maximum overshoot, introduced by the 7-tap filter responses, are respectively 3, 5 and 6 dB, while having a DC-gain around 1.2dB. In Fig. 6, the TX performance is summarized and compared against several integrated state-of-the-art solutions in different technologies. This work shows a doubling of the operating rate compared to FinFET solutions and closely matches the speed and power obtained in InP solutions which lack any FFE functionality.

References:

- [1] Z. Toprak-Deniz et al., "A 128Gb/s 1.3pJ/b PAM-4 transmitter with reconfigurable 3-tap FFE in 14nm CMOS," ISSCC, Feb. 2019
- [2] E. Groen et al., "A 10-to-112Gb/s DSP-DAC-based transmitter with 1.2Vppd output swing in 7nm FinFET," ISSCC, Feb. 2020
- [3] M. Nagatani et al., "A 256-Gbps PAM-4 signal generator IC in 0.25- μ m InP DHBT technology," BCICTS, Oct. 2018.
- [4] J. Verbist et al., "Real-Time 100 Gb/s NRZ and EDB transmission with a GeSi electroabsorption modulator for short-reach optical interconnects," JLT, Jan. 2018.



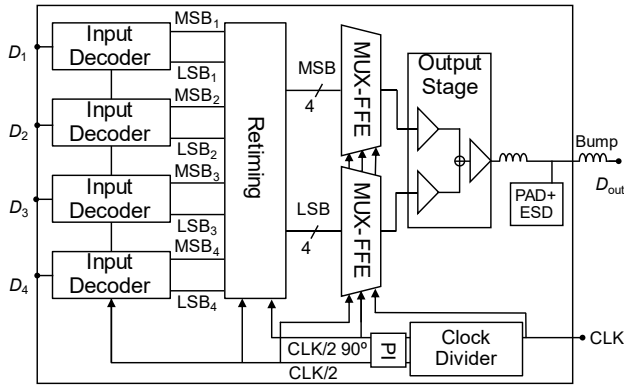


Fig. 1. Block diagram of the 4:1 PAM-4 serializer chip with mixed-signal FFE. All signals are fully differential.

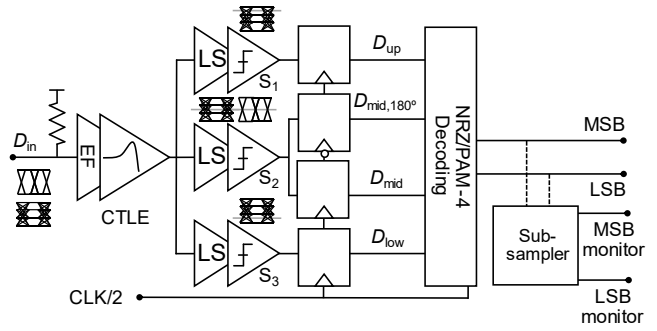


Fig. 2. Block diagram of NRZ/PAM-4 input decoders.

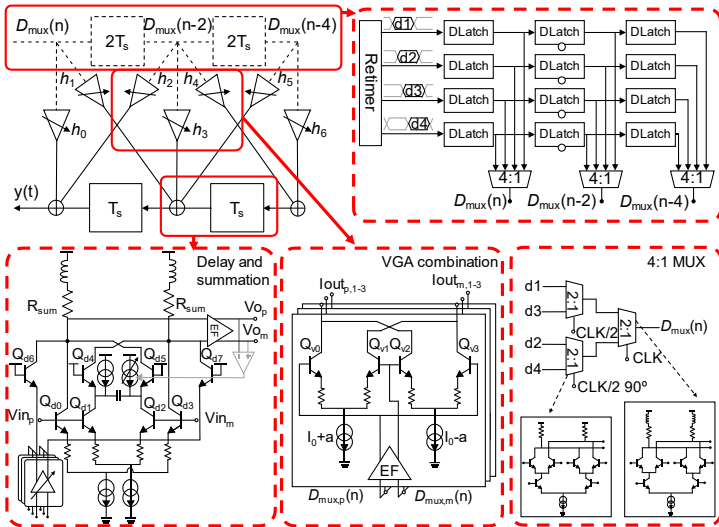


Fig. 3. Architecture of the MUX-FFE with the simplified schematics of the 4:1 MUX, (triple) VGA combination and the delay and summation block.

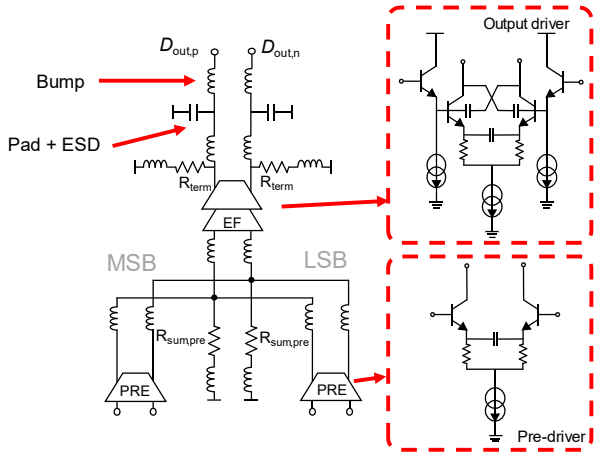


Fig. 4. Block diagram and simplified schematics of the output stage.

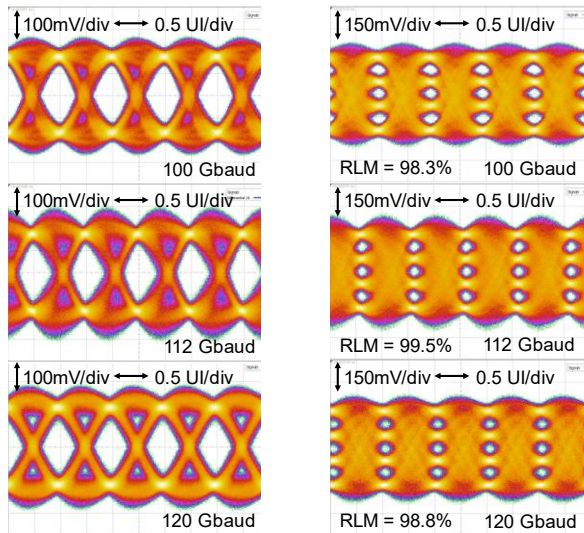


Fig. 5. Measured PRBS-15 NRZ (MSB only) and PAM-4 eye diagrams at 100,112 and 120Gbaud on a flip-chipped sample with the FFE optimized to reach 500mVpp output for the PAM-4 signals.

Ref.	[1]	[2]	[3]	[4]	This work
Technology	14nm FinFET	7nm FinFET	InP DHBT	55nm BiCMOS	55nm BiCMOS
Architecture	4:1MUX	DSP-DAC	2:1MUX	4:1MUX	4:1 MUX
Modulation	PAM-4	PAM-4	PAM-4	NRZ	PAM-4
Baudrate [GS/s]	64	5-56	128	100	120
Bitrate [Gb/s]	128	10-112	256	100	240
Equalization	3-tap FFE	4-tap FFE	-	6-tap FFE	7-tap FFE
Max. Transmit swing [Vpp]	1	1.2	0.9	-	1.2
Area [mm ²]	0.048*	0.193*	4	3.8	3 (0.295**)
Power [W]	0.166	0.118***	2	0.75	2.16 (PAM-4 mode) 2 (NRZ mode)
Efficiency [pJ/bit]	1.3	1.05	7.8	7.5	9 8.33

* Active area

** Area of MUX-FFE (x2) and output stage

*** Reported power without clocking

Fig. 6. Comparison with published state-of-the-art TX solutions for different technologies