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Efficient Offline Outer/Inner DAC Mismatch Calibration in Wideband $\Delta\Sigma$ ADCs

Hui Liu, Pieter Rombouts, *Member, IEEE*, and Georges Gielen, *Fellow, IEEE*

Abstract—Distortion due to feedback DAC mismatch is a key limitation in $\Delta\Sigma$ ADCs for wideband wireless communications. This paper presents an efficient frequency-domain mask-based offline mismatch calibration method of both the outer DAC and the inner DACs in a $\Delta\Sigma$ ADC. The test stimulus for the calibration is a two-tone signal near the band edge. To avoid the need for high-performance signal generation, a frequency mask is applied to void the stimulus signal and its phase noise. In this way, the method is robust against distortion and jitter in the stimulus signal, which therefore could be combined from two low-quality signal generators. The two-tone band-edge signal has the additional benefit that the number of needed samples of the excitation signal is very modest because as many intermodulations as possible contribute to the calculation of the mismatch errors of the DACs. Experimental results confirming the calibration method are obtained from a prototype chip, designed for an 85MHz signal bandwidth in 28nm CMOS technology. A two-tone stimulus around 78 MHz is applied to calculate the mismatch of the outer DAC and the inner DAC with only 68K samples. With the DACs calibrated, an SFDR improvement of 28.1 dB is achieved for a single-tone input at 5 MHz, while for a two-tone input around 71 MHz, the IM3 is improved from -63.6 dBc to below the noise floor (<-94.1 dBc). This illustrates the effectiveness of the approach.

Index Terms—Offline calibration, continuous-time, discrete-time, wideband, $\Delta\Sigma$, analog-to-digital converter, DAC mismatch.

I. INTRODUCTION

THE growth of mobile data is larger than that of the number of registered connections, which means that ever wider bandwidths (BW) are required for each wireless connection to integrate different radio bands [1], [2]. In the unavoidable presence of unwanted signals, including various blockers and other users, the analog-to-digital converter (ADC), as a critical block in the receiver system, needs to achieve not only the higher BW, but also a high linearity to suppress the harmonic and intermodulation (IM) distortions of these unwanted signals to below the minimum in-band signal [2], [3]. Multi-bit continuous-time (CT) $\Delta\Sigma$ ADCs with flat signal transfer function (STF) are widely applied in wireless communication systems for their good blocker immunity, inherent anti-aliasing and wide bandwidth [3]–[7].

Compared to single-bit CT $\Delta\Sigma$ ADCs like in [2], the limitation for multi-bit CT $\Delta\Sigma$ ADCs to achieve higher linearity is the component mismatch in the multi-bit digital-to-analog converters (DAC) in the feedback path [8]. As illustrative

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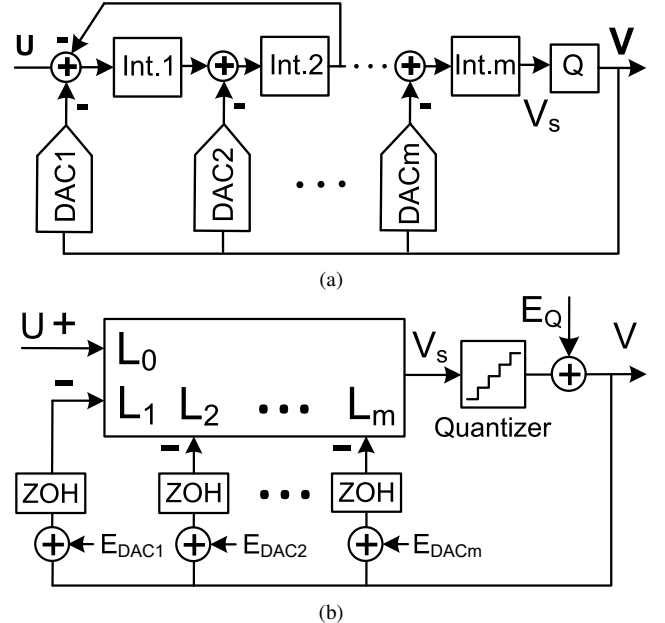


Fig. 1. (a) Block diagram of a general m -th-order CRFB $\Delta\Sigma$ ADC, and (b) its equivalent model, with the DACs' mismatch errors and the quantization error indicated.

architecture, Fig. 1(a) shows the block diagram of the cascade-of-resonators-with-feedback (CRFB) $\Delta\Sigma$ ADC topology. It has a low-pass STF (without peaking), which is known to achieve good blocker immunity and high in-band dynamic range in wireless communications [9]. When non-return-to-zero (NTZ) DACs are used, the ADC's equivalent model is shown in Fig. 1(b), where the DACs' mismatch (E_{DAC1} to E_{DACm} for an m -th-order $\Delta\Sigma$ ADC) and the zero-order hold (ZOH) and quantization error (E_Q) are added to the model. The mismatch of the outer DAC₁ directly contributes to the digital output, causing distortion and limiting the dynamic range. While the mismatches of the inner DACs are suppressed by their prior stages, they do contribute to the digital output in case of wideband converters with low oversampling ratio (OSR), as will be shown below.

There are several ways to reduce the impact of the mismatch of the DACs in $\Delta\Sigma$ ADCs. The most intuitive way is to size up the cell unit of the DAC, which definitely increases the excess loop delay (ELD) of the closed-loop system, consumes more power and causes a larger dynamic error [4], [10]. Dynamic element matching techniques such as [11] have also been used to achieve high linearity. However, these techniques are less effective at low OSR and also increase the ELD, and therefore are not suitable for high-bandwidth designs. Several other methods that don't cause extra ELD, have been implemented in the analog domain. In [12], the current-copier technique

has been proposed and verified on silicon [13], [14], but it suffers from charge leakage, charge injection and refresh spurs at low frequency [15]. To avoid the frequent refresh, a 1-bit DAC and DC value are used to only toggle two adjacent DAC elements and the DAC step size is calculated according to the digital output [16], [17]. The calculated mismatches of the DAC are calibrated through an injected analog compensation, which is a complicated the calibration procedure. Another similar technique is to measure the value of each DAC element, which requires extra complex mixed-signal circuitry [18]. The mismatch between the calculated digital value and the injected analog unit may also be problematic in [18]. In [19], a dithering-based technique has been used, but its performance was limited to a spurious-free dynamic range (SFDR) improvement of several dBs only.

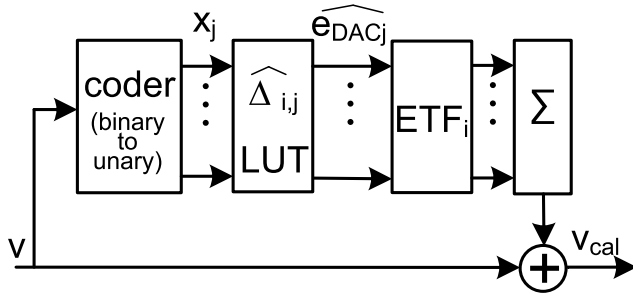


Fig. 2. Principle concept of digital calibration.

The mismatch of the DACs in a $\Delta\Sigma$ ADC can also be calibrated in the digital domain. As shown in Fig. 2, the calibration is performed by collecting estimated digital correction terms $\widehat{\Delta}_{i,j}$ from a look-up-table (LUT) and (after optional filtering with the corresponding error transfer function ETF_i) adding them to the modulator's digital output V to obtain a calibrated output signal V_{cal} . There are two families of digital calibration techniques. In the first family, the correction terms are obtained in an offline calibration cycle [20]–[22], while in the second family the correction terms are continuously updated online by some continuous adaptation technique [23]–[25]. This work focuses on offline calibration techniques, which have the advantage that no modification at all of the analog modulator core is needed and that they can also be used for debug and evaluation purposes. When looking at related prior art, the time-domain techniques [20], [21] suffer from the fact that a high-quality low-jitter low-distortion signal generator is required for the calibration. In [22], an alternative frequency-domain method has been demonstrated, without the need of a high-quality signal generator. However, since a large portion of the DAC mismatch energy falls outside the band and is not used for the mismatch calculation, a very large number of samples is required for this method to significantly improve the performance, which is a challenge for wideband ADCs with high sampling speed. Our proposed method solves this issue.

For the inner DACs, such as DAC_2 or DAC_m in Fig. 1(a), it is widely assumed that their errors can be neglected, because their effect is reduced by the gain of the preceding integrators, and only recently authors have attempted to correct

the corresponding errors. However, in wideband modulators, the OSR inevitably is very low, and hence the gain of prior integrators can be disappointingly low near the edge of the signal bandwidth. The inner DACs, especially the first inner DAC, can easily dominate the performance for higher input frequencies near the band edge, and therefore the errors of this inner DAC also need to be calibrated.

This paper therefore presents an efficient offline frequency-domain mask-based method to calibrate the mismatch of both the outer DAC and the inner DACs in wideband $\Delta\Sigma$ ADCs. The proposed method does not require an expensive signal generator nor too many data points. The effectiveness of the technique will be demonstrated on an experimental chip. Section II will illustrate the mechanism of DAC errors in $\Delta\Sigma$ ADCs. Section III will elaborate more about prior offline calibration techniques. The proposed offline calibration method will be explained in Section IV. Simulation and experimental results will be given in Section V and in Section VI, respectively. The paper will be concluded in Section VII.

II. DAC ERROR BEHAVIOR

A. Error Transfer Function

The error transfer function (ETF) is the transfer function from the mismatch error of one of the feedback DACs to the digital output. To explain the method, we start with the cascade of resonators with feedback (CRFB) structure of Fig. 1. The output signal V for the system of Fig. 1(b) can be written as ¹:

$$V = STF \cdot U + NTF \cdot E_Q - \sum_{i=1}^m (ETF_i \cdot E_{DAC_i}) \quad (1)$$

$$\begin{cases} STF = \frac{L_0}{1 + \sum_{i=1}^m L_i} \\ NTF = \frac{1}{1 + \sum_{i=1}^m L_i} \\ ETF_i = NTF \cdot L_i \end{cases} \quad (2)$$

where L_0 and $L_{i(1-m)}$ are the z -domain expression of the transfer function from the ADC input U to the node V_s in front of the quantizer, and the z -domain expression of the transfer function from $DAC_{i(1-m)}$ to the node V_s in Fig. 1(a), respectively. NTF is the noise transfer function of the $\Delta\Sigma$ ADC for the quantization noise. From (1) it is clear that, if ETF_i and E_{DAC_i} are known for all DACs, the effect of DAC mismatch can be eliminated from the digital output of the $\Delta\Sigma$ ADC by subtracting suitable correction terms. In the past, many authors have used the simplifying assumption that only the first DAC's errors should be corrected and additionally that the first error transfer function ETF_1 is equal to a constant (typically unity) across the entire band. While both assumptions are approximately valid for the case of a high OSR, they are incorrect in the wideband case (where the OSR is low), as we will demonstrate below.

To improve the quantization noise shaping performance, typically local feedback resonators are used [8]. However when doing this, the ETF is no longer constant, neither for the cascade of resonators with feedforward (CRFF) topology nor for the CRFB topology. To investigate the ETF for an effective example, we illustratively study a fourth-order CRFB

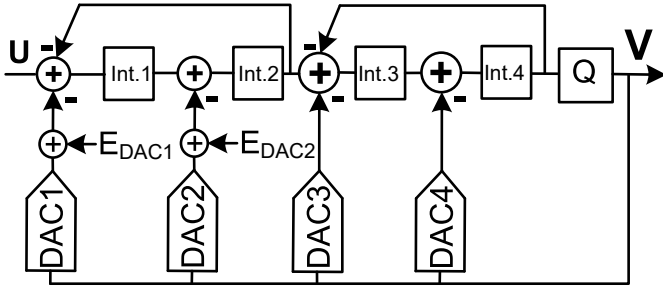


Fig. 3. Case study of a 4th-order CRFB $\Delta\Sigma$ ADC, with mismatch in both the outer DAC₁ and the inner DAC₂ indicated.

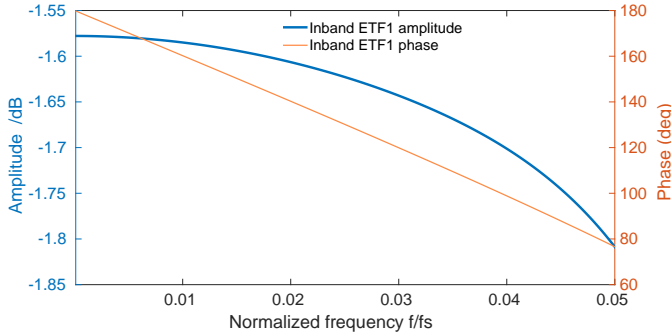


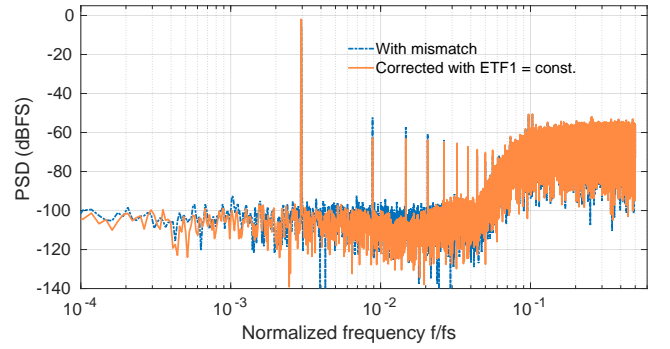
Fig. 4. The in-band amplitude and phase of the ETF of the DAC₁ mismatch for the $\Delta\Sigma$ ADC of Fig. 3.

$\Delta\Sigma$ ADC with 4-bit quantizer, shown in Fig. 3, where also the DAC₁ mismatch is indicated. The in-band ETF for the nominal modulator design (with ideal integrators) is illustrated in Fig. 4 for an OSR=10. The amplitude of ETF₁ shows a modest fluctuation of about 0.2 dB, but the phase of ETF₁ varies significantly: from 180 degrees to 76.7 degrees. With finite opamp gain and bandwidth included, the fluctuation can be larger.

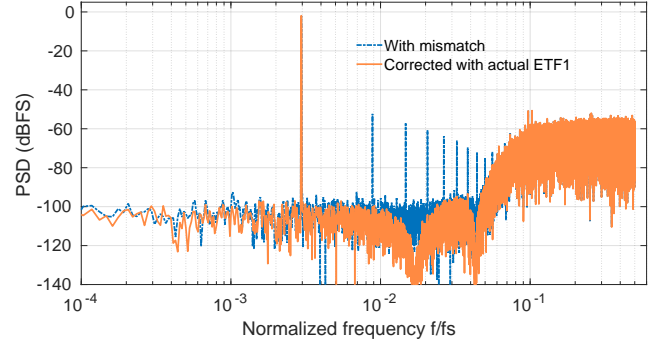
The mismatch of DAC₁, without any calibration, results in significant distortion, as shown in Fig. 5. When ETF₁ is approximated as a constant (0.83 = -1.62 dB) like in [20] and [22], the calibrated spectrum, with the correct DAC mismatch values, is shown in Fig. 5(a). With the approximated constant ETF₁ of 0.83 the calibrated output is given by:

$$V_{cal} = STF \cdot U + NTF \cdot E_Q + (0.83 - ETF_1) \cdot E_{DAC1} \quad (3)$$

Since ETF₁ in reality is not exactly a constant, as shown in Fig. 4, the output spectrum V_{cal} can not perfectly be reconstructed and has large distortions, which was also observed in [20] and [22]. Doing the calibration with the actual ETF₁ and the exact mismatch values of DAC₁, the ideal output spectrum is obtained, as shown in Fig. 5(b). Hence, in addition to using an accurate estimate of E_{DAC} , it is also important to use the correct ETF both in amplitude and phase, especially for the CRFB topology (Fig. 1), where the phase shifts drastically. Note that these ETFs in principle are known (i.e. they are defined by the loop filter design). However, due to circuit imperfections such as finite opamp bandwidth and parasitic loop delay, the actual ETF can deviate from its nominal case. We will come back to this in section VI.



(a)



(b)

Fig. 5. Output spectra of the CRFB topology of Fig. 3 for the case where there is only DAC₁ mismatch without calibration compared to: (a) correction with the approximation of ETF₁ = 0.83, and (b) correction with the actual ETF₁.

B. DAC error

We assume that all the DACs in Fig. 1 have k elements (for a n -bit quantizer: $k = 2^n - 1$), which are driven by control signals X_j derived from the output of the quantizer V in such a way that:

$$V = \sum_{j=1}^k X_j \quad (4)$$

Each control signal can take two values, depending on whether the element is selected or not. For a differential circuit, we adopt the most convenient notation by using +1 or -1 for X_j . Then the DAC _{i} error e_{DACi} can be expressed as:

$$E_{DACi} = \sum_{j=1}^k \Delta_{i,j} X_j \quad (5)$$

where $\Delta_{i,j}$ is the mismatch of the j th element of DAC _{i} . The offset of the DAC element is omitted for simplicity, because it only generates an overall offset, which is a less critical concern [4]. The control signals X_j are known from the quantizer output V , hence to estimate the DAC error E_{DACi} , only the element mismatches $\Delta_{i,j}$ need to be estimated.

C. Offline calibration core idea

The general flow of an offline calibration consists of the following steps. First, the ADC is stimulated by some input stimulus signal and the corresponding output signal V is collected. Then in the second step the input signal as well as (most) of the quantization noise is removed, either in the

time domain or in the frequency domain, from V to obtain a measured error signal V_{err} . From (1) and (5), we immediately see that:

$$V_{err} = - \sum_{i=1}^m ETF_i \sum_{j=1}^k \Delta_{i,j} X_j + N_{cal} \quad (6)$$

Here N_{cal} refers to noise that is uncorrelated to the DAC errors. This noise may come from circuit noise during the measurements, but also from incompletely removed quantization noise. In (6), the signals V_{err} and X_j are known after the calibration cycle. If there would be no noise, the mismatches $\Delta_{i,j}$ can then be computed by solving directly the above equation. In the presence of noise, the mismatches $\Delta_{i,j}$ can typically be found by solving this equation by minimizing its mean square error.

III. PRIOR OFFLINE CALIBRATION METHODS

With regard to the core calibration approach described above, prior art methods differ in two aspects: 1) in the choice of the input stimulus, and 2) in the way how the input signal and the quantization noise are removed from the measurement.

The first implementations of this approach were the sinusoidal-signal-based time-domain calibration techniques of [20], [21], which have been applied to several state-of-the-art designs [26], [27]. For these methods in-band sinusoidal signals, that are large enough to activate all the DAC elements, are fed to the ADC. Then the input stimulus signal is removed by curve fitting in the time domain, and the estimation of the $\Delta_{i,j}$ is obtained by minimizing the time-domain error.

Unfortunately, these time domain methods are computationally intensive due to the need to perform time-domain curve fitting and filtering [20], [21]. Moreover, they are sensitive to harmonic distortion and, even worse, jitter or phase noise present in the input signal. This is shown in Fig. 6(a) where the simulated results are shown for the case of an input signal with jitter. For the simulations, a 4-bit, 4th-order CRFF synthesized with an $H_\infty = 2$ and an OSR=10 was used [8], [28]. Note that the figure uses a Hann window in such a way that the window effect is entirely cancelled and the (still relatively narrow) line width seen in the figure is due to the intentionally added jitter. It is clear from Fig. 6(a) that the calibration of [20], [21] fails catastrophically, which is due to the fact that the algorithm tries to find correction coefficients that cancel the phase noise in the used input signal.

In [22], an alternative technique is proposed based on the frequency-domain processing of an out-of-band signal, to avoid the need for a high-linearity low-jitter input signal. Unfortunately, this technique requires a large number of samples to do the calibration. To illustrate this, we performed this calibration technique where we used a sinusoidal input signal just outside the signal band. First, we carried out the calibration with the same number of data points (i.e. 40K) as in the other cases. The result for this case is shown in Fig. 6(b). It is clear that the result is poor and that, although the noise floor is decreased, the distortion actually gets worse. When a larger number of samples is used, the accuracy of [22] gets better. For example, when 10M data points are used in the calibration, the

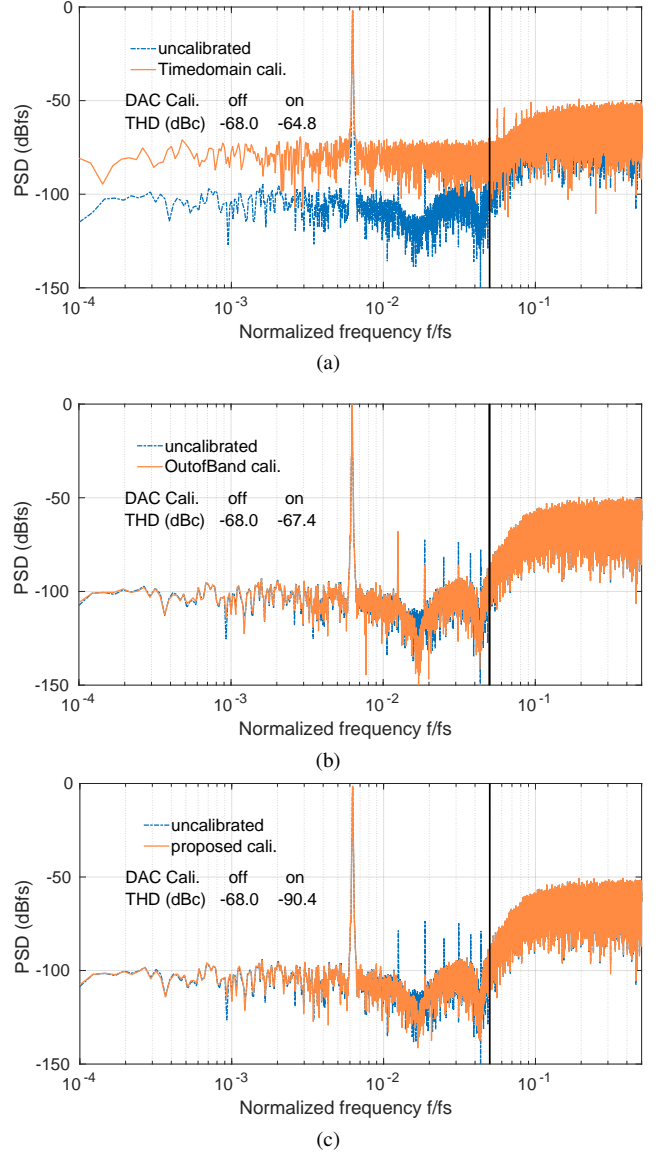


Fig. 6. Comparison of the calibration techniques for the case of an input signal with jitter (40K FFTs). (a) Time-domain technique of [20]; (b) out-of-band excitation technique of [22]; (c) proposed mask-based frequency-domain technique.

distortions of nine DAC elements reduce to about -100 dBc, which is still significantly less good than for our proposed new method with only 40K data points (Fig. 6(c)). An additional pitfall of [22] is that the method is not elaborated for the case where ETF is not a constant. Furthermore, despite the inherent anti-aliasing of a continuous-time $\Sigma\Delta$ modulator, when the OSR is very low, aliased harmonics of the out-of-band stimulus may also cause in-band spurs, partially offsetting the main advantage of the technique that no accurate signal source is needed. These disadvantages are overcome in our method.

IV. PROPOSED CALIBRATION METHOD

A. Input Stimulus selection

For the case of wideband $\Delta\Sigma$ ADCs with a low OSR, the band-edge gain of all integrators in the feedback loop

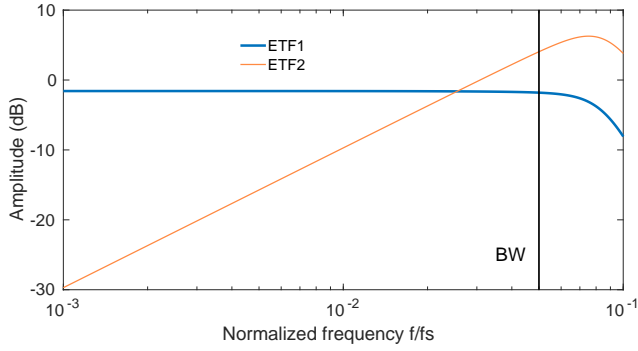


Fig. 7. Magnitude plot of the ETF of the mismatch for the outer DAC₁ and the inner DAC₂ in the architecture of Fig. 3, with ETF₂ becoming large near the signal band edge.

inevitably becomes relatively low. This is particularly the case for the first integrator in the CRFB topology in Fig. 3 [4], [8]. For example, for the illustrative case of a 4-bit, 4th order CRFB topology with $H_\infty = 2$ and $OSR=10$, the band-edge gain is below zero dB, which leads to an ETF₂ gain of 4 dB at the band edge, as shown in Fig. 7. Therefore, the common assumption that the mismatch of DAC₂ can be neglected is definitely incorrect in this case. This mismatch manifests itself clearly near the bandwidth edge and also needs to be calibrated. While the first integrator gain is very low in the CRFB topology, the other integrator coefficients are significantly larger (e.g. in our numerical example the second integrator gain is more than 10dB higher than that of the first one). As a consequence, the input-referred distortion of the third and later DACs indeed do not limit the ADC performance, but the mismatch of DAC₂ becomes important. Hence, we will elaborate in this paper the mismatch calibration of the outer DAC₁ and of the first inner DAC, i.e. DAC₂. The method can straightforwardly be extended to the calibration of more than two DACs.

The model of the CRFB $\Delta\Sigma$ ADC of Fig. 3 was built with Schreier's well known toolbox [8], [28]. It has resonators to optimize the zeros location to achieve maximum signal-to-quantization-noise ratio (SQNR). The ADC has a 4-bit quantizer, an $OSR = 10$, and $H_\infty = 2$, achieving a corresponding bandwidth of 85 MHz. As shown in Fig. 7, the amplitude of the mismatch ETF of DAC₁ remains almost constant, slightly smaller than 1, across the signal bandwidth, while that of DAC₂ behaves as a first-order differentiation (increasing with 20dB/decade) within the bandwidth. The mismatch of DAC₂ is therefore attenuated at low frequencies. When the frequency increases, the ETF₂ magnitude becomes larger than 0dB. Therefore, the mismatch of DAC₂ dominates the distortion in the upper part of the bandwidth (in this example above 50 MHz).

While the proposed calibration technique (see below) can work with a sinewave excitation, as was done for Fig. 6(c), this is not the best choice. Ideally, we want an input signal that does not put any requirements on the signal generator in terms of low distortion or jitter. To also efficiently calibrate the inner DAC(s), a significant part of the DAC-induced distortion should be in the upper part of the signal band. To alleviate

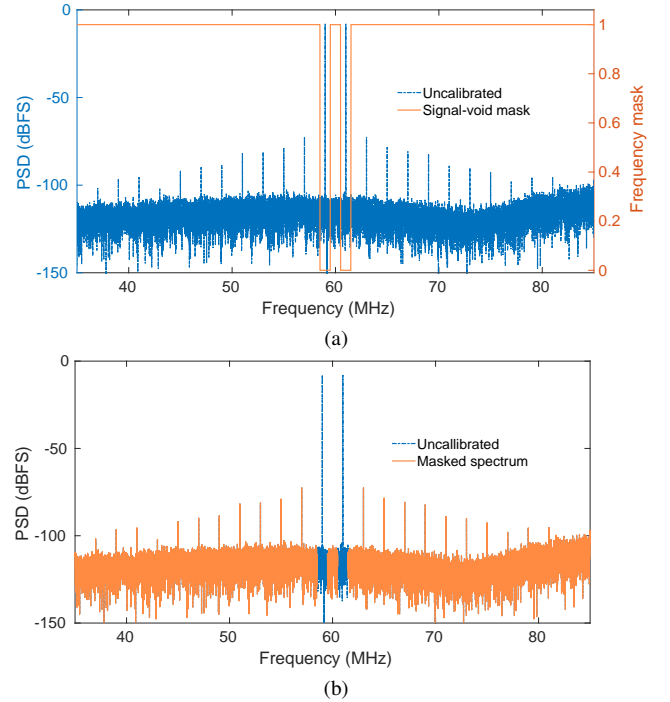


Fig. 8. (a) The uncalibrated output spectrum and the frequency-domain mask used, and (b) the masked uncalibrated spectrum.

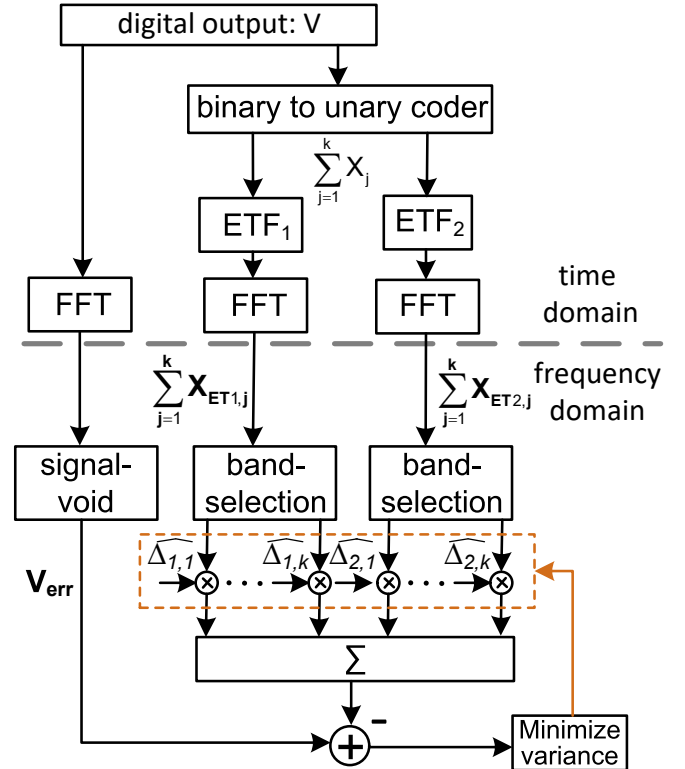


Fig. 9. Schematic representation of the proposed calibration technique.

this, we propose to use a closely spaced two-tone excitation, that could equally well be generated with two independent low-quality signal sources of which the outputs are combined. The frequency of the two-tone signals should be above half the bandwidth, such that all harmonic distortions of the signal

generator are outside the bandwidth. With such an input signal, DAC mismatches will manifest themselves as intermodulations falling within the bandwidth. This is shown in Fig. 8(a), where our example 85MHz-BW CRFB modulator is excited with two -8dBFS input tones at 59 MHz and 61 MHz. With this choice, all the DAC elements are activated and most intermodulation components are within the bandwidth of 85 MHz.

B. Frequency-Domain Mask-based Calibration

The actual calibration calculations are carried out in the frequency domain. Basically this is done by constructing an FFT approximation of (6). A schematic representation of the overall calibration approach is shown in Fig. 9.

The first step is to take the FFT of the digital output signal $v(n)$ (after proper windowing e.g. with a Hann or Blackman window) [29]. This provides the FFT result \mathbf{V} , which we represent as a row vector over the discrete frequency values.

To remove the out-of-band quantization noise and the input signal, a frequency-domain signal-void mask is applied. If the input stimuli have in-band imperfections, such as phase noise, the mask can also be used to remove these. With our choice of a two-tone stimulus near the band edge, phase noise is normally the only in-band imperfection, which is readily removed by the signal-void mask $M_s(f)$ defined as follows:

$$\begin{aligned} M_s(f) &= 0, & \forall f > BW \text{ and } \forall f \approx f_{sig} \\ &= 1, & \text{elsewhere} \end{aligned}$$

The signal-void mask $M_s(f)$ is shown in Fig. 8(a). The window of the mask, i.e. where $M_s(f)$ is 0 near the input frequencies, should properly attenuate the non-ideal input signal, such as phase noise, while keeping all the intermodulation components. To maintain a consistent notation, we will use the notation \mathbf{M}_s for the row vector containing the mask evaluated on the same frequency grid as the FFT signal \mathbf{V} . The masked output spectrum \mathbf{V}_{err} is then:

$$\mathbf{V}_{err} = \mathbf{V} \cdot \mathbf{M}_s \quad (7)$$

where \cdot is used to denote the element-wise multiplication. This masked output spectrum \mathbf{V}_{err} corresponds to the FFT of V_{err} , see Eq. (6), and is shown in Fig. 8(b).

The DAC element control signal, X_j ($x_j(n)$ in the time domain) are filtered by both ETF_1 and ETF_2 , which are assumed to be known or simulated, and then the corresponding FFTs are applied, leading to:

$$\begin{aligned} \mathbf{X}_{\text{ET1},j} &= \text{FFT}\{x_j(n) * \text{etf}_1(n)\} \\ \mathbf{X}_{\text{ET2},j} &= \text{FFT}\{x_j(n) * \text{etf}_2(n)\} \end{aligned} \quad (8)$$

Here, $*$ stands for the convolution, and etf_1 and etf_2 stand for the impulse response of the respective error transfer functions. Again, each Fourier transform is represented as a column vector over the frequency grid. To remove the out-of-band components, the band-selection mask M_b is defined as follows:

$$\begin{aligned} M_b(f) &= 0, & \forall f > BW \\ &= 1, & \text{elsewhere} \end{aligned}$$

Again, the notation \mathbf{M}_b is used for the row vector containing the mask evaluated on the same frequency grid as the FFT

signals. Now, we obtain the band-limited FFTs $\mathbf{X}_{\text{ETb1},j}$ and $\mathbf{X}_{\text{ETb2},i}$ of the filtered selection signals:

$$\begin{aligned} \mathbf{X}_{\text{ETb1},j} &= \mathbf{X}_{\text{ET1},j} \cdot \mathbf{M}_b \\ \mathbf{X}_{\text{ETb2},i} &= \mathbf{X}_{\text{ET2},i} \cdot \mathbf{M}_b \end{aligned} \quad (9)$$

Then we define the total \mathbf{X}_t matrix, by combining the FFT column vectors for both DAC_1 and DAC_2 as follows:

$$\mathbf{X}_t = [\mathbf{X}_{\text{ETb1},1} \cdots \mathbf{X}_{\text{ETb1},k} \mathbf{X}_{\text{ETb2},1} \cdots \mathbf{X}_{\text{ETb2},k}] \quad (10)$$

where k stands for the number of DAC elements. The mismatch vector of the two DACs, \mathbf{W} , is combined as:

$$\mathbf{W} = [\widehat{\Delta}_{1,1} \cdots \widehat{\Delta}_{1,k} \widehat{\Delta}_{2,1} \cdots \widehat{\Delta}_{2,k}]^T \quad (11)$$

where $\widehat{\Delta}_{i,j}$ represents the estimated mismatch value to be distinguished from the actual real mismatch value $\Delta_{i,j}$. Next, the FFT-domain version of (6) for the case that there is no other noise can be written as:

$$\mathbf{X}_t \cdot \mathbf{W} = \mathbf{V}_{err} \quad (12)$$

Now, the mismatch vector Δ can be found by solving this system of complex equations (remember that the FFTs have both real and imaginary components). The number of equations in this system is equal to the number of baseband frequency points (7.2K equations in the examples below), while the number of unknown elements in \mathbf{W} is the total number of DAC elements ($2k = 30$ in the examples below). Furthermore, due to the presence of noise (due to the residue quantization noise or other noise), this system is always overdetermined and needs to be solved in a least mean square way, with the mathematical constraint that Δ should be real. Straightforward algebraic manipulation similar to [20], [22] shows that the solution is equivalent to solving the linear system of equations:

$$[\text{Re}(\mathbf{X}_t^H \mathbf{X}_t)] \cdot \mathbf{W} = \text{Re}(\mathbf{X}_t^H \mathbf{V}_{err}) \quad (13)$$

where \mathbf{X}_t^H stands for the conjugate transpose of \mathbf{X}_t

Once the mismatches $\widehat{\Delta}_{i,j}$ are known, they can be stored in a LUT. During normal $\Delta\Sigma$ ADC operation, an accurate estimation $e_{\text{DAC}i}$ of the DAC error is obtained as $\sum_{j=1}^k \widehat{\Delta}_{i,j} x_j(n)$, and the digital output of Fig. 3 can be corrected as:

$$\begin{aligned} V + \sum_{i=1}^2 (\text{ETF}_i \cdot \widehat{E}_{\text{DAC}i}) &= \text{STF} \cdot U + \text{NTF} \cdot E_Q \\ &+ \underbrace{\sum_{i=1}^2 (\text{ETF}_i \cdot (\widehat{E}_{\text{DAC}i} - E_{\text{DAC}i}))}_{\approx 0} \end{aligned} \quad (14)$$

Clearly, the error due to mismatch of the two feedback DACs is almost eliminated.

V. SIMULATION RESULTS

To illustrate the effectiveness of the proposed method, it has been applied to the CRFB model of Fig. 3. DAC_1 and DAC_2 are given mismatches with a standard deviation (σ) of 0.3% and a standard deviation of 0.5%, respectively. The calibration has been performed with the excitation signal shown in Fig.

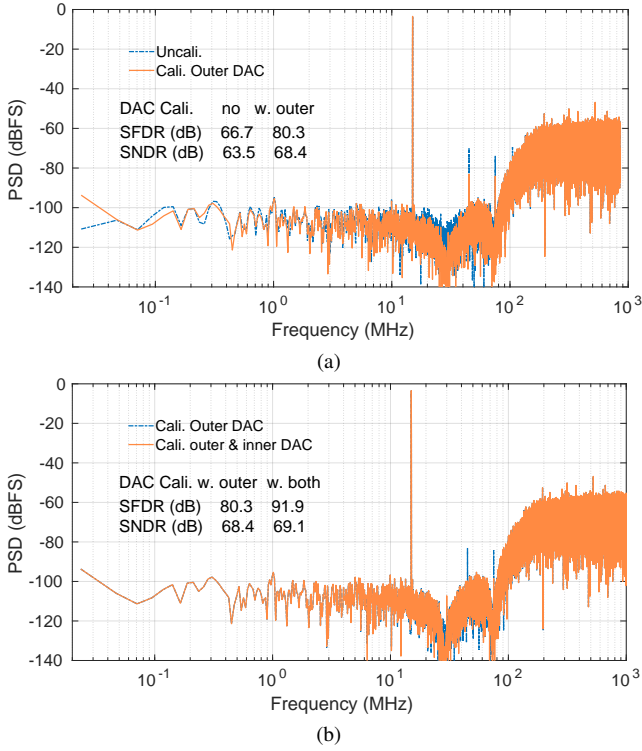


Fig. 10. Simulated single-tone spectra: (a) with only the outer DAC₁ calibrated, and (b) with both the outer DAC₁ and the inner DAC₂ calibrated. The latter case has no residual distortion.

8. A simulated in-band sequence of 68K samples is used for the calculation, and the exact ETFs, known through simulation, are used. For a -3.4 dBFS 15 MHz input signal, the uncalibrated spectrum with 72K-point FFT is shown in Fig. 10(a). Due to the DACs' mismatch, the SFDR and SNDR are limited to 66.7 dB and 63.5 dB, respectively. The estimated values are calculated using equation (12). When only the outer DAC₁ is calibrated, the calibrated spectrum is presented in Fig. 10(a), where both the SFDR and SNDR are improved. However, the distortion due to the inner DAC₂ is still visible in the spectrum. The result after calibrating both the outer DAC₁ and the inner DAC₂ is shown in Fig. 10(b), where the SFDR and SNDR are further improved to 91.9 dB and 69.1 dB, respectively.

In addition, the calibration has been applied to the case of a band-edge two-tone input signal with two -8.7 dBFS input tones at $f_1 = 77$ MHz and $f_2 = 79$ MHz, respectively. For this, the same calculated mismatch values obtained from the calibration shown in Fig. 8 were used. The results are depicted in Fig. 11. With the calibration of the outer DAC₁, IM3 is -76.0 dBc at 75 MHz ($2f_1 - f_2$) and is -75.6 dBc at 81 MHz ($2f_2 - f_1$). When both the outer DAC₁ and the inner DAC₂ are calibrated, IM3 is further improved to -103 dBc at 75 MHz and to -91.8 dBc at 81 MHz. Clearly, the distortion is reduced hugely.

VI. EXPERIMENTAL RESULTS

To illustrate the method on real silicon, the above described calibration technique has been applied to a fabricated continuous-time $\Delta\Sigma$ modulator chip for wideband wireless communication that was available to the authors, with topology

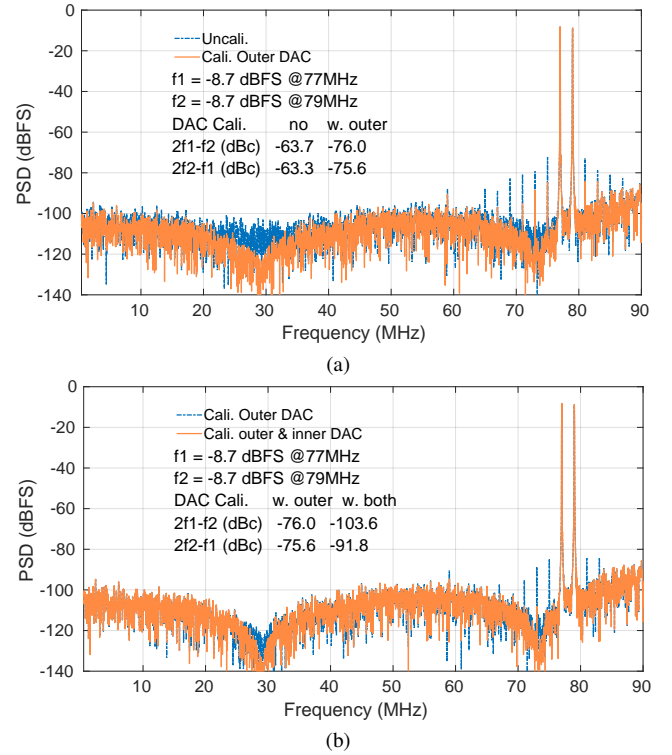


Fig. 11. Simulated two-tone spectra: (a) with only the outer DAC₁ calibrated, and (b) with both the outer DAC₁ and the inner DAC₂ calibrated, resulting in high distortion suppression.

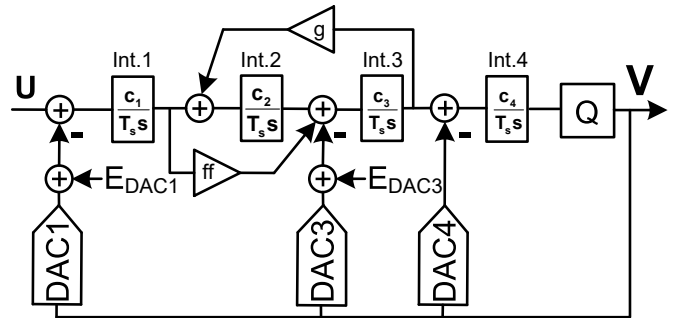


Fig. 12. The topology of the experimentally tested CIFF-B CT $\Delta\Sigma$ ADC.

shown in Fig. 12. It is the cascade-of integrators with feed-forward and feedback (CIFF-B) topology. It differs from the previously described illustrative topology of Fig. 3 in the sense that DAC₂ is missing. This topology was adopted because of its good tradeoff between the power consumption and the out-of-band blocker immunity [8]. Designed in 28nm CMOS, it has a sampling frequency of 1.7 GHz and an OSR of 10, corresponding to a bandwidth of 85 MHz. A discrete-time second-order noise-shaping quantizer is used to reduce the quantization noise, without suffering from the mismatch of the signal transfer function of the multi-stage topology [13]. The quantizer has a STF of 1 and outputs 4 digital bits per sampling. The integrator time constants are trimmed to account for the $\pm 20\%$ process variations.

All DACs have a relatively small unit size to reduce the ELD as well as the dynamic errors. In this CIFF-B topology, *Int.4* has a larger band-edge gain than *Int.3* and, similarly, the

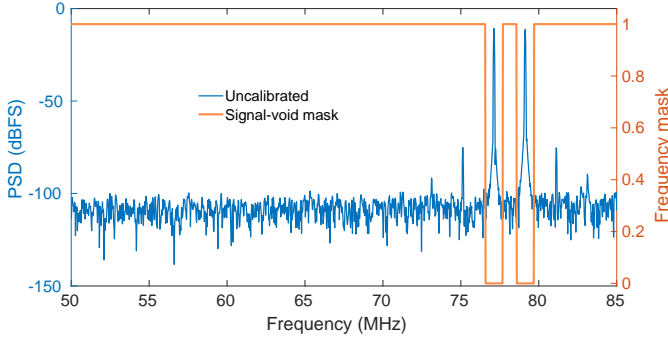


Fig. 13. Measured uncalibrated output spectrum for the $\Delta\Sigma$ ADC of Fig. 12 for a band-edge two-tone input and the applied frequency-domain mask used in the calibration.

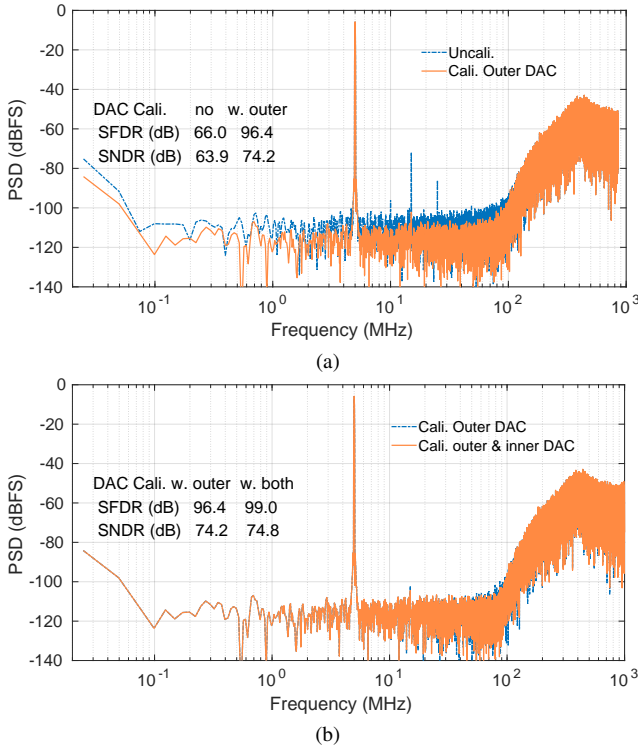


Fig. 14. Measured single-tone output spectra for the architecture of Fig. 12 for low-frequency input signals: (a) with only the outer DAC₁ calibrated, and (b) with both the outer DAC₁ and the inner DAC₃ calibrated, showing highly reduced distortion.

band-edge gain of Int_3 is larger than that of both Int_1 and Int_2 . Hence, with the integrator coefficients for this design, the mismatch of DAC₃ is relevant, while the mismatch of DAC₄ is negligible. Therefore, the calibration of the experimental chip of Fig. 12 focuses on the mismatch calibration of the outer DAC₁ and of the inner DAC₃.

Two -10.8 dBFS input tones at 77.125 MHz and 79.125 MHz are used as excitation to calculate the errors of both DACs. The measured spectrum is shown in Fig. 13. Without any calibration, the mismatches of the DACs result in obvious intermodulation components near the actual signals. The two frequencies are chosen to make sure that all intermodulation components over -100 dB fall within the bandwidth. The frequency-domain mask to void the input tones is also shown

in Fig. 13. The window width where the mask is ‘0’ around the input was chosen as 1.2 MHz in our experiments. It should be wide enough to void the input tone and its phase noise. If the window of the mask is chosen too large, then more useful frequency information is discarded and more samples are needed to achieve the same linearity. In our test, 68K samples are used to calculate the mismatches of DAC₁ and DAC₃, using (12).

In our experiments, we used the nominally designed filter for the first Error Transfer Function ETF₁. However, for the other Error Transfer Function, ETF₃, this did not give good results. After investigation we found that this was due to a mismatched delay between the actual ETF₃ and the designed one, and we found that this delay had to be determined quite accurately to obtain good results. The amplitude characteristic of ETF₃, on the other hand, was found to be quite uncritical and very well approximated by a simple double differentiation. In this way, we used for ETF₃ the following double-differentiation filter, combined with a delaying phase shifter (with sub-fractional delay equal to $T_s(n_{d,i} + n_{d,f})$) according to:

$$\widehat{ETF}_3 = (1 - z^{-1})^2 \cdot z^{-n_{d,i}} \cdot \frac{1 - \alpha + \alpha z^{-1}}{1 + \alpha - \alpha z^{-1}} \quad (15)$$

where α is equal to $n_{d,f}/2$. The correct value of the total delay was found by a trial and error procedure and turned out to be equal to $4.8T_s$. Note that this error transfer function enables a very simple implementation.

Fig. 14(a) plots the measured FFT for a 5MHz -4.0dBFS input signal with and without outer DAC₁ calibration. Without calibration of the outer DAC₁, the SNDR and the SFDR are limited to 63.9 dB and 66.0 dB, respectively. The mismatch values of the outer DAC₁ and the inner DAC₃ are calculated from the measurement of Fig. 13. When only the outer DAC₁ is calibrated using (14), the spectrum is shown in Fig. 14(a): the SNDR and the SFDR are significantly improved to 74.2 dB and 96.4 dB, respectively. When both the outer DAC₁ and the inner DAC₃ are calibrated, the spectrum is shown in Fig. 14(b): the SNDR and the SFDR are even further improved to 74.8 dB and 99.0 dB, respectively. At low frequencies, however, the performance improvements due to the DAC₃ calibration are limited, which is due to the high attenuation of the double differentiation property of ETF₃. The small residual third harmonic distortion of the calibrated spectrum is most probably due to the signal generator used.

The same calculated mismatches values have then been applied to calibrate the digital output of a high-frequency two-tone input near the band edge, as shown in Fig. 15. The uncalibrated spectrum for two -11.5 dBFS input tones at 70 MHz (f_1) and 72 MHz (f_2) is shown in Fig. 15(a). Without any DAC calibration, IM2 is -85.8 dBc at 1 MHz ($f_2 - f_1$), and IM3 is -64.3 dBc at 68 MHz ($2f_1 - f_2$) and 63.6 dBc at 74 MHz ($2f_2 - f_1$). When only the outer DAC₁ is calibrated, IM2 is improved to below -100 dBc, and IM3 is improved to -79.0 dBc at 68 MHz and to -77.7 dBc at 74 MHz. Due to the high gain of ETF₃ at these near-band-edge frequencies, this first calibrated result still displays strong intermodulations, as shown in Fig. 15(a). When both the outer DAC₁ and the inner

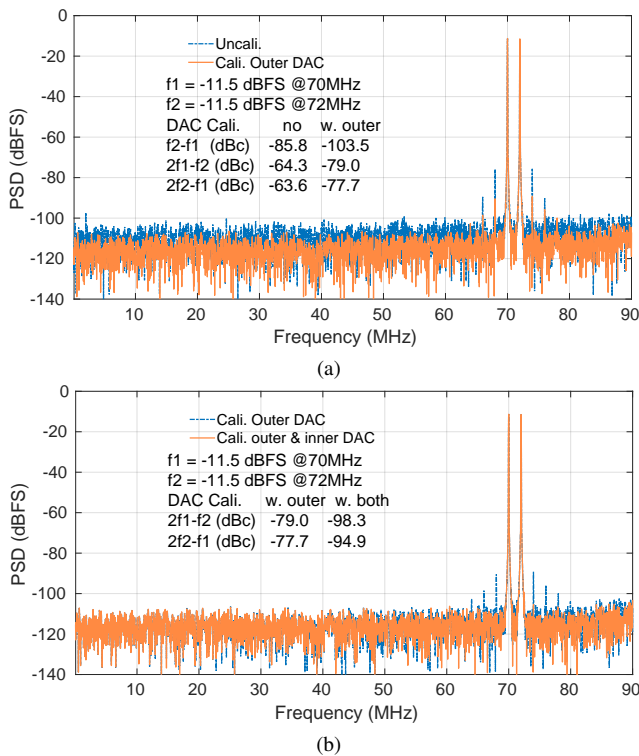


Fig. 15. Measured two-tone output spectra for the architecture of Fig. 12 for high-frequency input signals: (a) with only the outer DAC₁ calibrated, and (b) with both the outer DAC₁ and the inner DAC₃ calibrated, showing highly reduced distortion.

DAC₃ are calibrated, IM3 is further improved to -98.3 dBc at 68 MHz and to -94.9 dBc at 74 MHz, as shown in Fig. 15(b). This clearly shows that the presented calibration method for both the outer DAC and the inner DAC drastically reduces the impact of the DAC mismatches on the ADC's nonlinearity.

VII. CONCLUSIONS

This paper has presented an efficient frequency-domain mask-based offline mismatch calibration method for both the outer DAC and the inner DACs in continuous-time $\Delta\Sigma$ ADCs for wideband wireless communications. To avoid the need for high-performance signal generation, a frequency mask is applied to void the input signal and its phase noise. Moreover, a two-tone band-edge signal is chosen as the input stimulus during calibration. In this way, the method is robust against the harmonic distortion and phase noise in the input signal, and could be generated from two low-quality signal generators. Using the two-tone band-edge signal has the additional benefit that the number of needed samples of the excitation signal is very modest because nearly all intermodulations contribute to the calculation of the mismatches of the DACs. Simulation results have been presented that are in full agreement with the theory. They have also been confirmed by measured experimental results on a prototype chip, designed for an 85MHz signal bandwidth in 28nm CMOS technology. In this experiment, the calibration to calculate the DAC mismatch has been done with only 68K samples. With the DACs calibrated, an SFDR improvement of 28.1 dB has been achieved for a single-tone input at 5 MHz, while the IM3 at 74 MHz has

been improved from -63.6 dBc to -94.1 dBc for a two-tone input around 71 MHz. The experimental results have proven the effectiveness of the proposed calibration method.

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