Full Papers

Implementation of a 16-phase 8-branch Charge Pump with Advanced Charge Recycling Strategy

Hui Peng†, *member*, Pieter Bauwens†, Herbert De Pauw†, and Jan Doutreloigne†, *nonmember*

SUMMARY A fully integrated 16-phase 8-branch Dickson charge pump is proposed and implemented to decrease the power dissipation due to parasitic capacitance at the bottom plate of the boost capacitor. By using the charge recycling concept, 87% of the power consumption related to parasitic capacitance is saved. In a 4-stage version of this charge pump, a maximum power efficiency of 41% is achieved at 35 µA output current and 11 V output voltage from a 3.3 V supply voltage. The proposed multi-branch charge pump can also reach a very low output voltage ripple of only 0.146% at a load resistance of 1 MΩ, which is attributed to the fact that the 8-branch charge pump can transfer charges to the output node eight times consecutively during one clock period. In addition, a high voltage gain of 4.6 is achieved in the 4-stage charge pump at light load conditions. The total chip area is 0.57 mm^2 in a 0.35µm HV CMOS technology.

key words: *8-branch charge pump, Charge recycling, High efficiency, Low voltage ripple.*

1. Introduction

Charge pump (CP) circuits are widely used in flash memory [1], power management blocks of System on Chip [2], energy harvesting systems for wireless sensor nodes of Internet of Things [3] and implantable biosensors [4]. Fig. 1 shows the classical Dickson charge pump that uses a diode-connected n-type MOSFET as charge transfer device [5]. It has the advantage that it can be integrated in monolithic chips since the capacitors and charge transfer devices are all available in CMOS technology. However, the main drawback of CP circuits is their relatively low efficiency compared with the inductor-based converters. One of the main reasons for the efficiency reduction is the parasitic capacitance of the flying boost capacitor. In each clock period, the parasitic capacitance Cp always needs to be charged and discharged, but it doesn't make any useful contribution to the CP operation.

In order to increase the power efficiency, the charge sharing concept is introduced in [6]. The basic principle of charge recycling is: before the clock signal at the bottom plate of the boost capacitor charges from GND to the supply voltage VDD (or discharges from VDD to GND), the bottom plates of the boost capacitors in 2 consecutive stages having

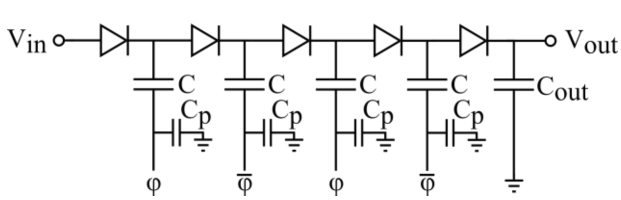

Fig. 1 Four-stage Dickson charge pump

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different potentials are shorted, so that both of them have an intermediate potential of VDD/2. As a result, at the next clock period only charging from VDD/2 to VDD is required by the supply voltage. This method can save 50% of the power consumption attributed to the parasitic capacitance. It also can be implemented in a cross-coupled CP to reuse the charges between two branches of one stage [7] and several papers deal with the optimization of the charge recycling CP, demonstrating that charge recycling is a meaningful method to improve CP efficiency [8], [9]. In this paper, a 16-phase 8-branch CP using charge recycling strategy is proposed, which can save 87% of the power consumption related to the parasitic capacitance.

2. Circuit Implementation

2.1 The Principle of a 4-phase 2-branch CP

Fig. 2 depicts one stage of a 4-phase 2-branch CP and the corresponding clock waves. Phases φ1 and φ2 are two non-overlapping clock signals that drive the gates of the n-type MOSFETs which connect the top plate of the boost capacitor to the front stage or connect the bottom plate of the boost capacitor to GND. Phases $\overline{\varphi 1}$ and $\overline{\varphi 2}$ drive the gates of the p-type MOSFETs which connect the top plate of the boost capacitor to the next stage or connect the bottom plate of the boost capacitor to VDD. Signal T controls the transmission gate (TG) to short the bottom plates of the boost capacitors.

The operation of this 4-phase 2-branch CP is explained in Fig. 3 where the transistors controlled by phases φ1, φ2, $\overline{\varphi 2}$ and $\overline{\varphi 1}$ are simply denoted by S1, S2, S3 and S4 respectively, whereas S5 represents the TG. There are four operation periods, detailed as follows: I. During the period t1, S1 and S4 are turned on, S2 and S3 are turned off, S5 is also turned off. Node C1 is connected to GND, node C2 is connected to VDD, and charge is flowing as indicated by the arrows in Fig. 3(a). II. During period t2, S1-S4 are all turned off, only S5 is on. As shown in Fig. 3(b), the charge recycling takes places and charge flows from C2 to C1. Hence, both nodes C1 and C2 will have a potential of VDD/2. III. During period t3, S1 and S4 are turned off, S2 and S3 are turned on, S5 is turned off again, as shown in Fig. 3(c). At this moment, node C1 is connected to VDD and the supply voltage only needs to charge it from VDD/2 to VDD,

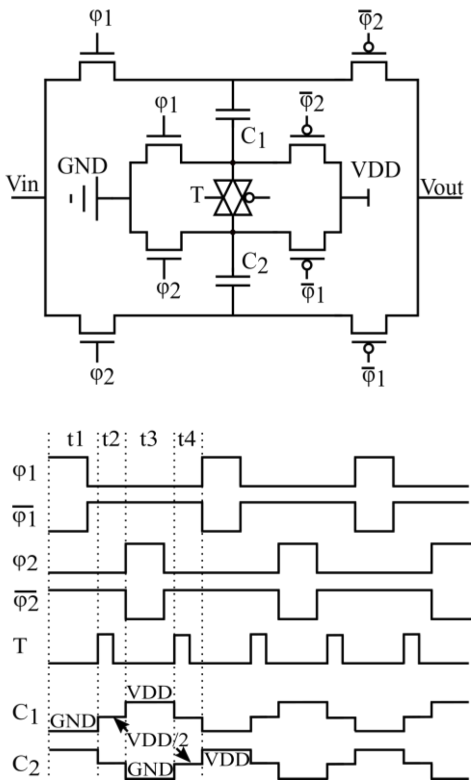

Fig. 2 One stage of the 4-phase 2-branch CP structure and the corresponding clock scheme

but not from GND to VDD. At the same moment, node C2 is connected to GND and it's discharged from VDD/2 to GND. IV. During period t4, as shown in Fig. 3(d), the switch states are the same as in period t2. The only difference is the charge recycling direction, from C1 to C2 this time.

For the 1-branch Dickson CP in Fig. 1, during one clock signal period, the parasitic capacitance needs to be charged from GND to VDD one time, and the corresponding energy consumption is:

$$Ec = Cp \cdot \ VDD^2$$

For the 4-phase 2-branch CP, if every stage has the same total value of boosting capacitance as in the 1-branch Dickson CP, every boost capacitor should have a value C/2. The corresponding parasitic capacitance is then Cp/2. The two parasitic capacitors need to be charged to VDD, which

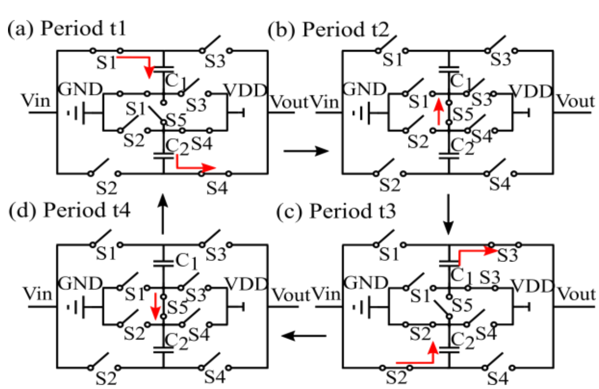

Fig. 3 4-phase 2-branch CP operation states

happens during periods t1 and t3 respectively, after they have been pre-charged to VDD/2 during periods t4 and t2. The corresponding energy consumption is:

$$Ec = \frac{Cp}{2} \cdot \ VDD \ \cdot \left(VDD - \frac{VDD}{2}\right) \cdot 2 = Cp \cdot \frac{VDD^2}{2}$$

This means that there is only half of the energy consumption related to the parasitic capacitance in the 4-phase 2-branch CP compared with the 1-branch Dickson CP.

2.2 Proposed 16-phase 8-branch CP

The proposed 16-phase 8-branch CP is shown in Fig. 4(a), which is the extension of the 4-phase 2-branch CP. Every branch is the same as in the 4-phase 2-branch CP and has one boost capacitor and four MOS switches. In every stage the bottom plates of the boost capacitors are connected by a TG matrix as shown in Fig. 4(b), where the switches represent the TGs.

φ1 - φ8 are eight non-overlapping clock signals. At any particular moment there is only one boost capacitor connected between the previous stage and GND, and at the same time there is another single boost capacitor connected between the next stage and VDD. The other six boost capacitors are all separated from other stages, as well as from GND and VDD, but they take part in the charge recycling through the TG matrix.

Fig. 5 shows one of the 16-phase 8-branch CP boost capacitor's bottom plate waveforms and the charge

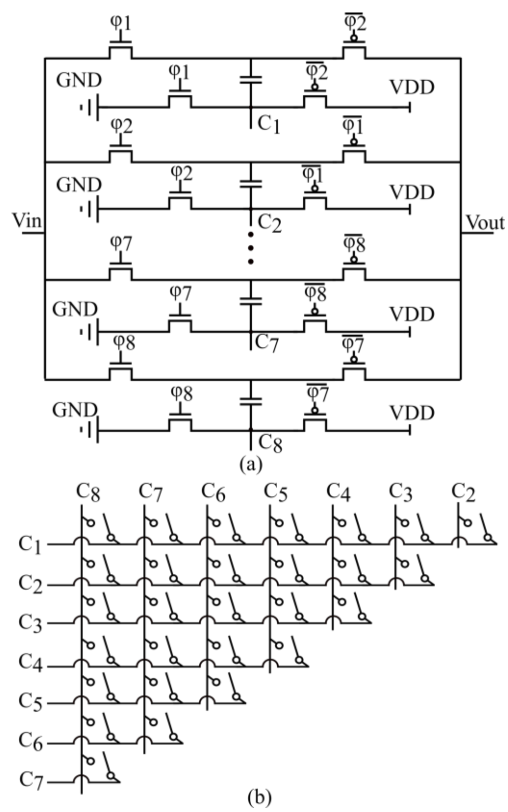

Fig. 4 (a) One stage of the 16-phase 8-branch CP structure (b) TG matrix

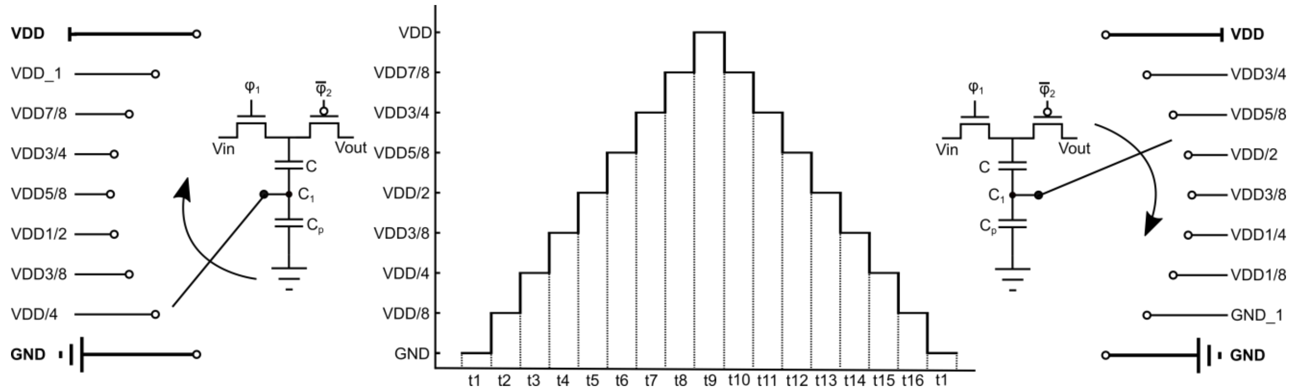

Fig. 5 16-phase 8-branch CP boost capacitor's bottom plate waveform

recycling procedure. In the 4-phase 2-branch CP there is only one intermediate voltage VDD/2 which is achieved by shorting bottom plates previously charged to VDD or discharged to GND. In this 16-phase 8-branch CP, we have seven intermediate voltages VDD/8, VDD/4, VDD3/8…. VDD7/8. t1-t8 are the potential increasing periods and t10-t16 are the potential decreasing periods. During t1 the phase φ1 is high and φ2 is low. Consequently, node C1 is connected to GND and charge is flowing from the previous stage to the boost capacitor C. During t2-t8 φ1 and φ2 are both low, which keeps the four MOS switches in this branch off. At period t2 node C1 is connected to a node Cx that has a potential of VDD/4. At this moment branch x is in a potential decreasing period, exactly the same situation as node C1's period t16. As a result, both nodes C1 and Cx will have a potential VDD/8. At period t3 node C1 is connected to a node Cy that has a potential of VDD3/8. At this instant branch y is in the decreasing period that corresponds to node C1's period t15. Both nodes C1 and Cy will reach a potential VDD/4. During periods t4-t8 we can get other intermediate voltages by using this strategy.

One thing to note is that during t8, in order to get a potential VDD7/8, node C1 needs to be shorted to a node Cz that has a potential of VDD. For this potential on node Cz, which will be discharged to VDD7/8, we use VDD_1 in Fig. 5 so as to distinguish it from the supply voltage VDD itself which will always keep its original potential (analog reasoning for node potential GND_1). During period t9, φ1 is low and φ2 is high, so that C1 is now connected to the supply voltage which only needs to charge the parasitic capacitance from VDD7/8 to VDD. At the same time the switch that connects xthe boost capacitor to the next stage will be on and will transfer charge to the next stage. During the potential decreasing periods t10-t16, node C1 will be shorted sequentially with other nodes which are in a potential increasing period until its potential arrives at VDD/8. Then the phase φ1 changes to high again and discharges node C1 to GND.

In the 16-phase 8-branch CP, the nominal and parasitic capacitance of the boost capacitors are C/8 and Cp/8 respectively. The energy consumption related to the total parasitic capacitance in one stage is:

$$Ec = \frac{Cp}{8} \cdot \ VDD \ \cdot \left(VDD - \frac{7VDD}{8}\right) \cdot 8 = Cp \cdot \frac{VDD^2}{8}$$

This means 87.5 % of the energy consumption is saved compared with the 1-branch Dickson CP. When we extend this technique to an arbitrary n-branch charge pump, the equation for the energy consumption becomes:

$$Ec = \frac{Cp}{n} \cdot \ VDD \ \cdot \left(VDD - \frac{(n-1) \cdot VDD}{n}\right) \cdot n = Cp \cdot \frac{VDD^2}{n}$$

As the number of branches increases, the energy consumption related to the parasitic capacitance decreases accordingly. But when the number of branches in the CP increases, the number of components and control signals increases as well, as shown in Fig. 2 and Fig. 4, which means that the complexity of the clock generation circuit and the associated power consumption will also increase. According to our simulations, when the number of branches reaches 16, the efficiency of the CP starts to decrease.

2.3 Clock Generation Circuit

To control this 16-phase 8-branch CP, a precise and stable clock signal is necessary. Fig. 6 shows the schematic of the on-chip clock generation circuit. The frequency of this circuit is determined by the control voltage (V_C) which is connected to the gate of p-type MOSFET P_1. V_C controls the drain current of P1, which drives the unity-gain current mirror N_1 + N_2, resulting in a ring oscillator bias current equal to the current through P_1. The ring oscillator's frequency is determined by:

$$f=1/2\tau n \tag{1}$$

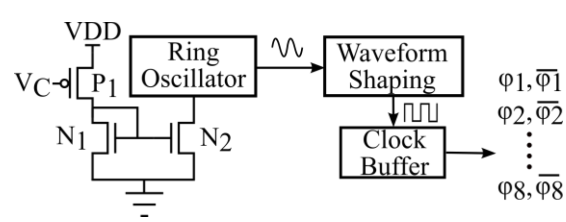

Fig. 6 The schematic of the clock generation circuit

in which τ is the average inverter delay and n is the number of inverters. In this work the number of inverters is 17. When the current through the oscillator increases, the charge and discharge time for one inverter is becoming shorter, which means the inverter delay τ is decreased. By (1), the oscillator's frequency will increase. It is therefore clear that the control voltage V_C and the oscillator's frequency exhibit a negative correlation. The signal from the oscillator then passes through the waveform shaping and clock buffer circuits to become the expected clock signals $\varphi 1$, $\overline{\varphi 1}$, $\varphi 2$, $\overline{\varphi 2}$ .... $\varphi 8$, $\overline{\varphi 8}$ to control the CP.

3. Measurement Results

In order to verify the design of the proposed CP, a 0.35μm HV CMOS technology was chosen to fabricate this 16-phase 8-branch CP. The maximum operation voltage of this technology is 120 V, which makes it easy to extend this design to applications that demand higher voltages. Fig. 7 shows the chip photograph and the core area is 2.04 mm × 0.28 mm. The CP has four cascaded stages and in every stage there are 8 boost capacitors of 2 pF.

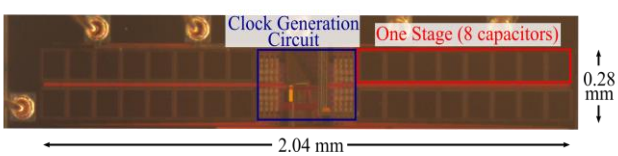

Fig. 7 Chip photograph

The output voltage of the CP as a function of the output current at different values of the supply voltage (VDD) is shown in Fig. 8, measured at a clock frequency of 2.2 MHz. In the light load condition the maximum voltage gain that can be achieved is 4.6 for all supply voltage values. Fig. 9 shows the measured output voltage waveforms of the CP at different resistive loads. The voltage ripple is 18 mV peak-to-peak at a load resistance of 1 MΩ, which is only 0.146% of the output voltage. For a load resistance of 0.1 MΩ, the voltage ripple is 35 mV.

The power efficiency is also characterized as a function of the output current at different supply voltage values as shown in Fig. 10. The efficiency takes the losses in the clock generation circuit into account and there is a one-to-one correspondence between the measurement points of efficiency in Fig. 10 and output voltage in Fig. 8. The maximum efficiency around 41% is achieved at an output current of approximately 35 μA with different supply wwvoltages. At the light load condition, the efficiency of the CP is decreasing when the supply voltage is increased from

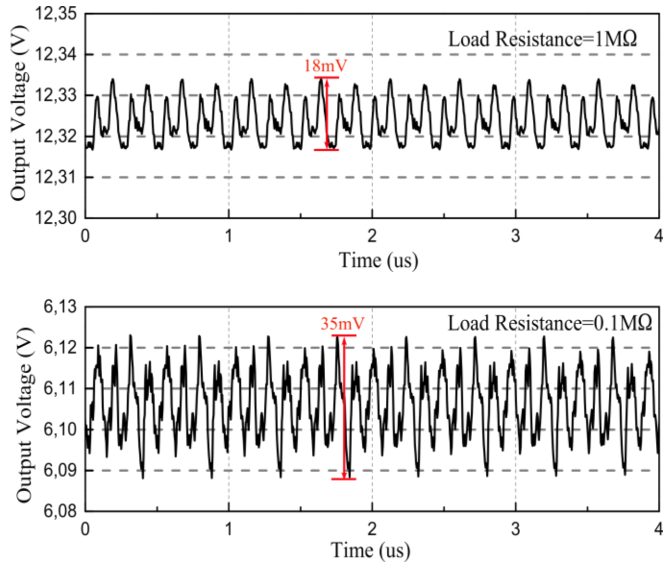

Fig. 9 Measured output voltage waveform at different resistive load

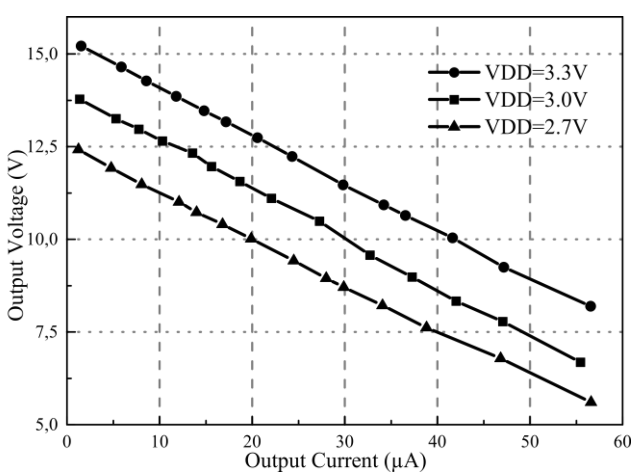

Fig. 8 Measured output voltage versus output current at different VDD values

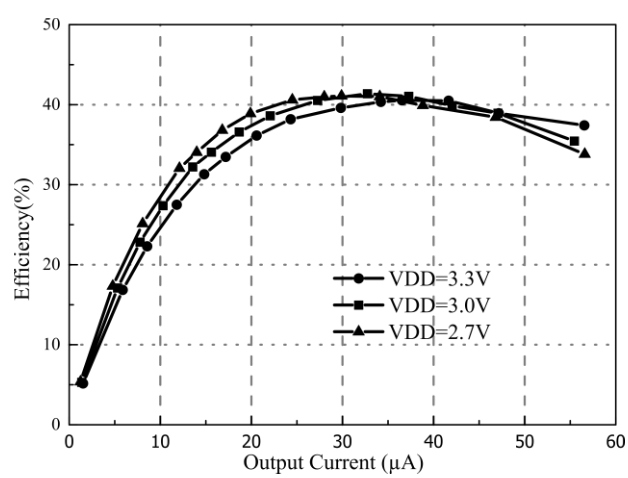

Fig. 10 Measured efficiency versus output current at different VDD values

Table I Performance summary and comparison

Parameter	[10]	[11]	[12]	This work
Technology	0.16 µm	HV 0.35 µm	0.18 µm	HV 0.35 µm
# stages	6	10	3	4
Vin	3.3 V	3.3 V	3.3 V	3.3 V
Vout	16 V	17 V	10.5 V	15.2 V
Total capacitors	SMD 1.32 µF	500 pF	MIMCAP 400 pF	PIPCAP 64 pF
Frequency	6.67 MHz	2.5 MHz	86.1 MHz	2.2 MHz
Area	1.65 mm^2	17.68 mm^2	N/A	0.57 mm^2
Efficiency	70%	10%	69%	41%
Voltage ripple	1%	N/A	2.7%	0.146%

2.7 V to 3.3 V. In Table I the chip performance is summarized and compared with other CPs reported in literature [10], [11], [12].

4. Conclusion

In this work, a fully integrated 16-phase 8-branch CP is proposed and demonstrated using a 0.35 µm HV CMOS technology. The chip area of this 4-stage CP is 2.04 × 0.28 mm^2. By employing the charge recycling concept in this CP, a maximum power efficiency of 41% is achieved at 35 µA output current and 11 V output voltage from a 3.3 V supply voltage. The output voltage ripple is limited to 0.146% of the output voltage under a 1 MΩ resistive load.

Acknowledgments

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References

[1] C. Zambelli, R. Micheloni, L. Crippa, L. Zuolo and P. Olivo, "Impact of the nand flash power supply on solid state drives reliability and performance", IEEE Trans. Device Mater. Rel, vol.18, no.2, pp. 247-255 2018. doi:10.1109/TDMR.2018.2819720.
[2] Y. Lu, J. Jiang and W.-H. Ki, "Design considerations of distributed and centralized switched-capacitor converters for power supply on-chip", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol.6, no.2, pp. 515-525 2018. doi:10.1109/JESTPE.2017.2747094.
[3] S. Yoon, S. Carreon-Bautista and E. Sánchez-Sinencio, "An area efficient thermal energy harvester with reconfigurable capacitor charge pump for iot applications", IEEE Trans. Circuits Syst. II, Exp. Brief, pp. 1974 - 1978 2018. doi: 10.1109/TCSII.2018.2794299.
[4] J. Olivo, S. Carrara and G. De Micheli, "Energy harvesting and remote powering for implantable biosensors", IEEE Sensors Journal, vol.11, no.7, pp. 1573-1586 2011. doi: 10.1109/JSEN.2010.2085042.
[5] J. F. Dickson, "On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique", IEEE J. Solid-State Circuits, vol.11, no.3, pp. 374-378 1976. doi: 10.1109/JSSC.1976.1050739.
[6] C. Lauterbach, W. Weber and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps", IEEE J. Solid-State Circuits, vol.35, no.5, pp. 719-723 2000. doi:10.1109/4.841499.
[7] H.-W. Hwang, J.-H. Chun and K.-W. Kwon, "A low power cross-coupled charge pump with charge recycling scheme", in Signals, Circuits and Systems (SCS), 2009 3rd International Conference on, pp. 1-5, IEEE, 2009.
[8] J. Doutreloigne, "Fully integrated dickson charge pumps with optimized power efficiency", in WCECS, pp. 811-817, 2010.
[9] H. Zhu, M. Huang, Y. Zhang and T. Yoshihara, "A 4-phase cross-coupled charge pump with charge sharing clock scheme", in 2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA),, pp. 73-76, IEEE, 2011.
[10] R. Karadi and G. V. Pique, "3-phase 6/1 switched-capacitor dc-dc boost converter providing 16v at 7ma and 70.3% efficiency in 1.1 mm^3", in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, pp. 92-93, IEEE, 2014.
[11] L. Bisoni, C. Carboni, L. Raffo, N. Carta and M. Barbaro, "An hv-cmos integrated circuit for neural stimulation in prosthetic applications", IEEE Trans. Circuits Syst. II, Exp. Brief, vol.62, no.2, pp. 184-188 2015. doi:10.1109/TCSII.2014.2387679.
[12] Z. Luo, M.-D. Ker, W.-H. Cheng and T.-Y. Yen, "Regulated charge pump with new clocking scheme for smoothing the charging current in low voltage cmos process", IEEE Trans. Circuits Syst. I, Reg. Papers, vol.64, no.3, pp. 528-536 2017. doi:10.1109/TCSI.2016.2619693.

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