

High-yield parallel transfer print integration of III-V substrate-illuminated C-band photodiodes on silicon photonic integrated circuits

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ABSTRACT

Transfer printing is an enabling technology for the efficient integration of III-V semiconductor devices on a silicon waveguide circuit. In this paper we discuss the transfer printing of substrate-illuminated III-V C-band photodetectors on a silicon photonic waveguide circuit. The devices were fabricated on an InP substrate, encapsulated and underetched in FeCl₃, held in place by photoresist tethers. Using a 2x2 arrayed PDMS stamp with a pitch of 500 μm in x-direction and 250 μm in y-direction the photodiodes were transfer printed onto DVS-BCB-coated SOI waveguide circuits interfaced with grating couplers. 83 out of 84 devices were successfully integrated.

Keywords: Heterogeneous integration, photodiodes, photonic integration, transfer printing, silicon photonics.

1. INTRODUCTION

Heterogeneous III-V-on-Si integration for photonics has been an intense research topic in recent years. With the intention to integrate an efficient laser source on silicon photonic integrated circuits (PICs), several integration approaches such as direct III-V growth [1] and die-to-wafer bonding [2-4] are being studied, however a compelling industrial wafer scale technique is still unavailable.

Transfer printing is a novel pick-and-place technology whereby devices processed in a dense array on the III-V wafer can be selectively picked using a polydimethylsiloxane (PDMS) stamp and printed on a silicon photonics wafer with high alignment accuracy (better than $\pm 1 \mu\text{m}$, 3σ [5]). Recently, several demonstrations of this technology have been reported, including transfer printing III-V photodiodes [6] and lasers [7-9] but also PbS quantum dot films [10], Si-Ge devices [11], etc., showcasing the versatility of the technology.

The main advantage of the transfer printing is the *parallel* integration of the III-V components without requiring large bond pads as are needed for flip-chip integration. This enables a time- and material-efficient integration of III-V devices on 200 mm or 300 mm silicon photonics wafers in several printing cycles. This paper is dealing with transfer printing arrays of III-V substrate illuminated C-band photodiodes on silicon photonics waveguide circuits. Using a 2x2 array stamp we picked and printed 84 devices. We present the successful fabrication, release, transfer printing, post-processing and characterization, obtaining a yield of 98.8%.

2. DESIGN AND FABRICATION

2.1 Design

The silicon photonic target wafers were fabricated in imec's passive technology platform using a 220 nm thick silicon device layer, a 1.2 μm thick top oxide cladding and 70 nm, 150 nm and 220 nm etch depths [12]. The schematic layout of the target waveguide circuit is displayed in Fig. 1 a). The circuit consists of arrays of 6x14 C-band input and output grating couplers, placed with a 500 μm / 250 μm pitch in x- and y-direction. The top 42 grating couplers are 1D grating couplers (4.5 dB single mode fiber-to-chip loss per coupler at 1550 nm) and the bottom 42 are 2D grating couplers (6 dB single mode fiber-to-chip loss per coupler at 1550 nm). Tetris-brick alignment markers were added to aid to the high printing alignment accuracy as will be discussed below.

On the III-V source wafer, $55 \times 55 \mu\text{m}$ square photodiodes with $23 \mu\text{m}$ circular apertures were designed in a dense array on a pitch of $100 \mu\text{m}$ and $125 \mu\text{m}$ in x- and y-direction respectively (Fig 1 b)). The photodiodes are to be released and transfer printed using a 2×2 arrayed stamp spaced with a $500 \mu\text{m} \times 250 \mu\text{m}$ pitch.

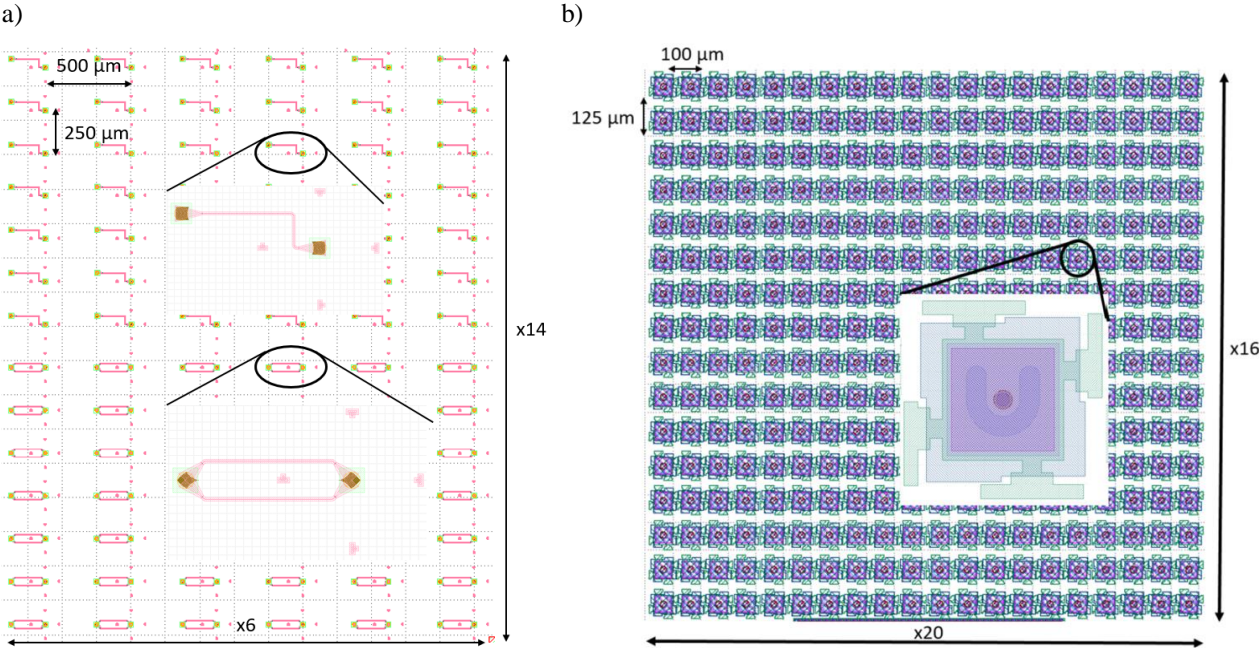


Fig. 1. a) Schematic layout of the silicon photonic target wafer; b) schematic layout of the III-V source wafer.

2.2 Photodiode Fabrication

The epitaxial material stack of the III-V photodiodes is presented in Table 1. The p-i-n layer stack consists of an intrinsic InGaAs absorber sandwiched between InP p-type and n-type cladding layers and an additional bottom InGaAs layer which acts as a release layer. The p-contact is formed on a heavily doped InGaAs layer.

Table 1. Epitaxial III-V layer stack for photodiode fabrication.

Layer	Material	Thickness (um)	Doping	Function
1	InP	100	n.i.d	Cap
2	InGaAs	100	$>1 \times 10^{19}$	p-contact
3	InGaAs	200	1×10^{19}	p-contact
4	InP	300	5×10^{17}	p-contact
5	InGaAs	1000	n.i.d	Absorption
6	InP	240	1×10^{18}	n-contact
7	InP	60	n.i.d.	n-contact
8	InGaAs	1000	n.i.d.	Release
9	InP	150	n.i.d.	Buffer/Substrate
10	InP		n-type	Substrate

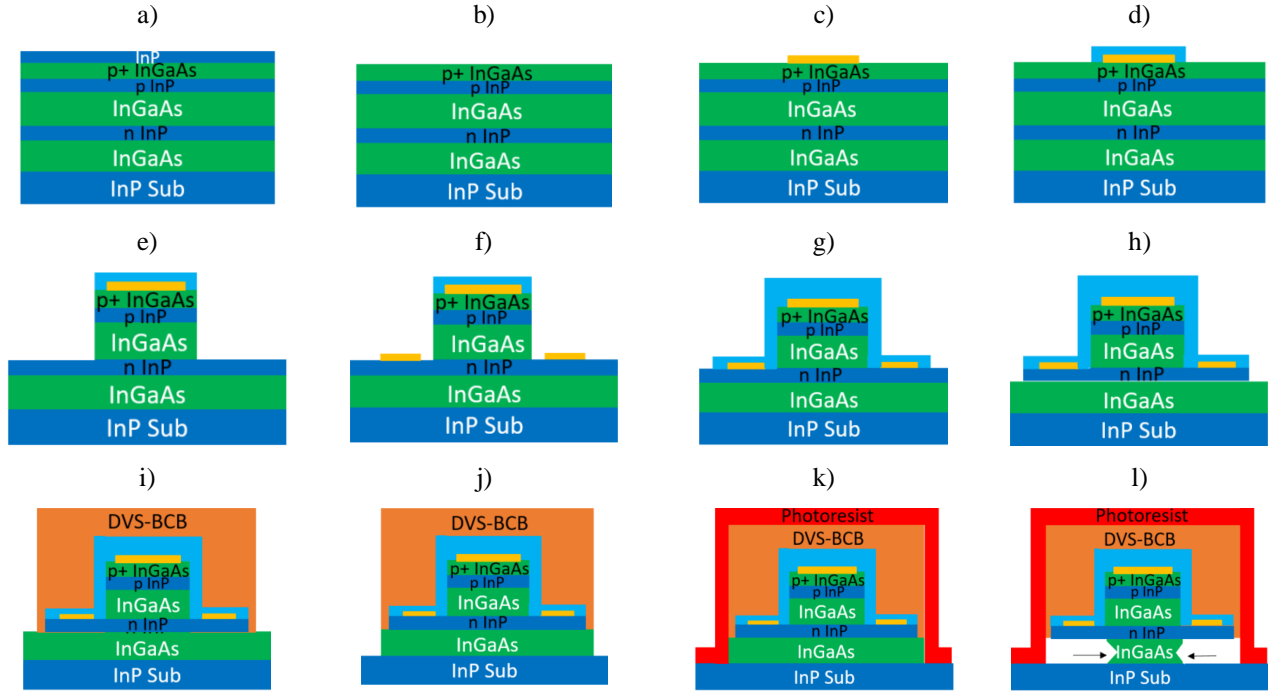


Fig. 2. Schematic illustration of III-V photodiode fabrication, release processes.

III-V photodiode fabrication was performed in the Ghent University cleanroom and the full sequence is schematically depicted in Fig. 2. We start with the full layer stack (Fig. 2 a)) and used HCl wet etching for about 20 seconds to remove the InP cap layer (Fig. 2 b)). Then, circular 21 μm diameter Ti/Au p-contacts were deposited (Fig. 2 c)). By depositing and patterning a 150 nm thick plasma-enhanced chemical vapor deposition (PECVD) mixed frequency silicon nitride (MF-SiNx), the p-metal was protected (Fig. 2 d)). Using the layer as a hard mask to define the 23 μm circular mesa by etching it using inductively coupled plasma (ICP) using CH_4/H_2 for 40 min. The etch was stopped on top of the n-InP layer and the residual intrinsic InGaAs was removed by dipping the sample into a Piranha 1:1:10 solution for 30 seconds (Fig. 2 e)). Then, the U-shape Ni/Ge/Au n-contacts (Fig. 2 f)) and an additional 150 nm of MF-SiNx, which was patterned in square patterns of 50 x 50 μm was defined (Fig. 2 g)). This SiNx pattern was used as a hard mask to etch the n-InP layer and stop on the InGaAs release layer using a combination of ICP dry etching and $\text{HCl}:\text{H}_2\text{O}$ 1:1 wet etching for 45 seconds (Fig. 2 h)). ~1.5 μm divinyl-siloxane-bis-benzocyclobutene (DVS-BCB) passivation was spin-coated, cured at 280°C and patterned (Fig. 2 i)). Afterwards the release layer was patterned using ICP (Fig. 2 j)) and the device was encapsulated using a ~3 μm thick photoresist. After patterning the photoresist tethers (Fig. 2 k)) the release was performed by placing the devices in an $\text{FeCl}_3:\text{H}_2\text{O}$ (1 mg : 2 ml) solution at 3°C for about 55 minutes to underetch the InGaAs release layer and make the devices free hanging, anchored to the substrate by the photoresist tethers (Fig. 2 l)). The top view of a fabricated and released 20 x 7 array of photodiodes is depicted in Fig. 3.

2.3 Transfer Printing

Transfer printing was performed using the μTP -100 lab scale printer using the automatic printing mode. We used square 60 x 60 μm PDMS posts in a 2x2 array on a pitch of 500 by 250 μm . The process is schematically depicted in Fig. 4. Devices are picked when the stamp is laminated with the released devices and quickly moves up (Fig. 4 a)). In this case the tethers break at their weakest points and devices are attached to the stamp (Fig. 4 b)). For printing, the stamp is brought in close proximity of the target wafer and the devices are first aligned with respect to the target wafer (Fig. 4 c)). Printing is performed by laminating the device against the ~50 nm thick DVS-BCB spin-coated target wafer and slowly moving the stamp in the vertical direction (Fig. 4 d)). This way, the devices stay attached to the target substrate.

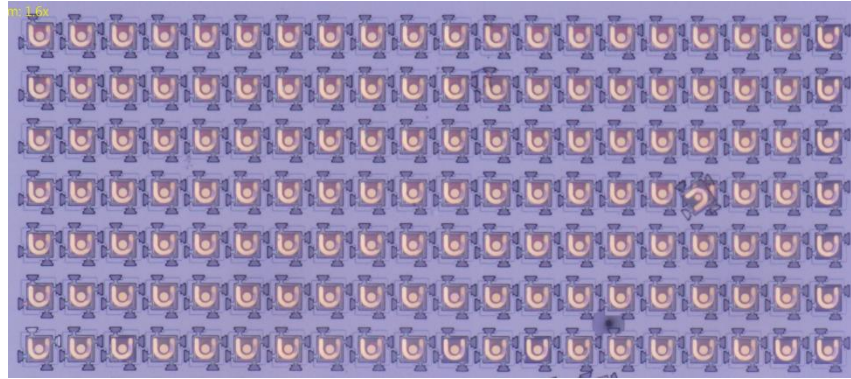


Fig. 3. Top view of the fabricated and released 20x7 array of C-band photodiodes.

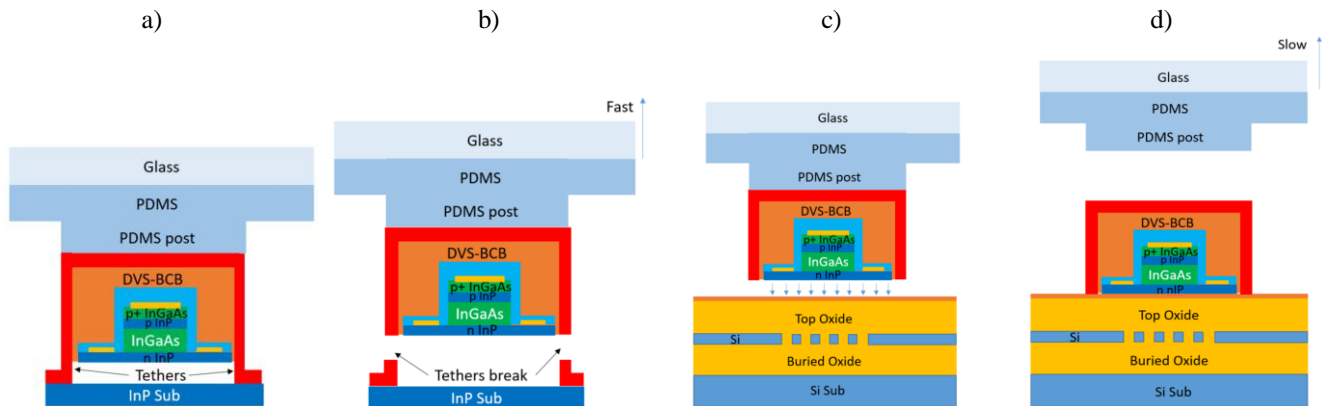


Fig. 4. Schematic sequence of the transfer printing process.

Fig. 5 shows the source substrate after the transfer printing. Arrayed transfer printing was performed in an automated mode, skipping the positions of collapsed or broken devices (marked in red in Fig. 5). 84 devices were picked using the 2x2 arrayed printing and 80/84 devices were printed. The 4 failed devices were populated on the target wafer by picking and printing using a 1x1 PDMS stamp (shown in blue in Fig. 5), as a rework procedure.

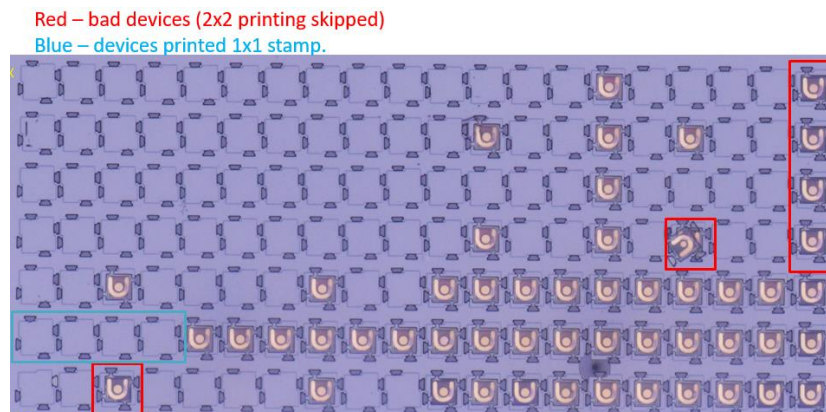


Fig. 5. Top view of the source wafer after completing the transfer printing. Collapsed or broken devices are shown in red which were skipped by the 2x2 array stamp. The blue rectangle indicates devices that were picked and printed in 1x1 mode.

2.4 Post-Processing

After transfer printing arrays of devices on the target wafer, the photoresist encapsulation was reflowed at 140°C for 10 minutes to improve III-V device adhesion and was then removed using O₂ reactive ion etching (RIE) (Fig. 6 a)). The DVS-BCB was fully cured at 280°C after which a new thick ~3 μm DVS-BCB layer was spin coated and cured at 280°C again (Fig. 6 b)). Then using RIE (SF₆/O₂ gas mixture for ~6 minutes), the DVS-BCB layer was etched back and the p- and n-electrode were opened (Fig. 6 c)). After this ~1 μm thick Au ground-signal-ground tracks were defined for electrical device characterization (Fig. 6 d)).

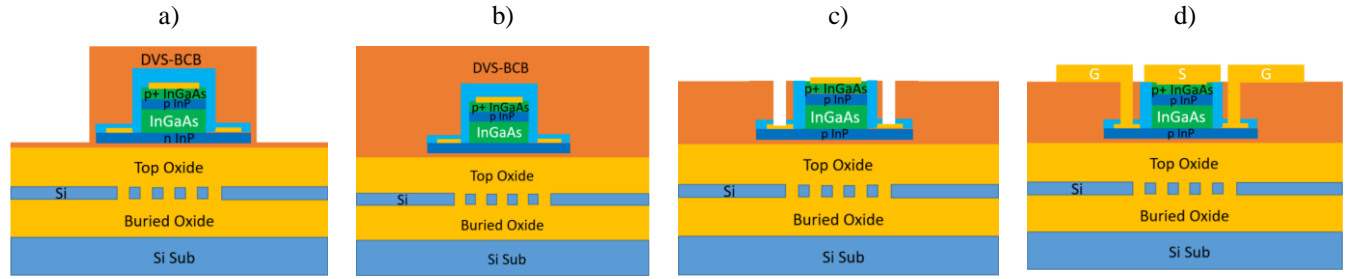


Fig. 6. Schematic illustration of the post-processing of the target wafer.

The target chip, after completing the post-processing is depicted in Fig. 7. All devices were printed and metalized. Only one device on row 13, column 2 transfer printed with the noticeable misalignment on the target (see the left inset in Fig. 7).

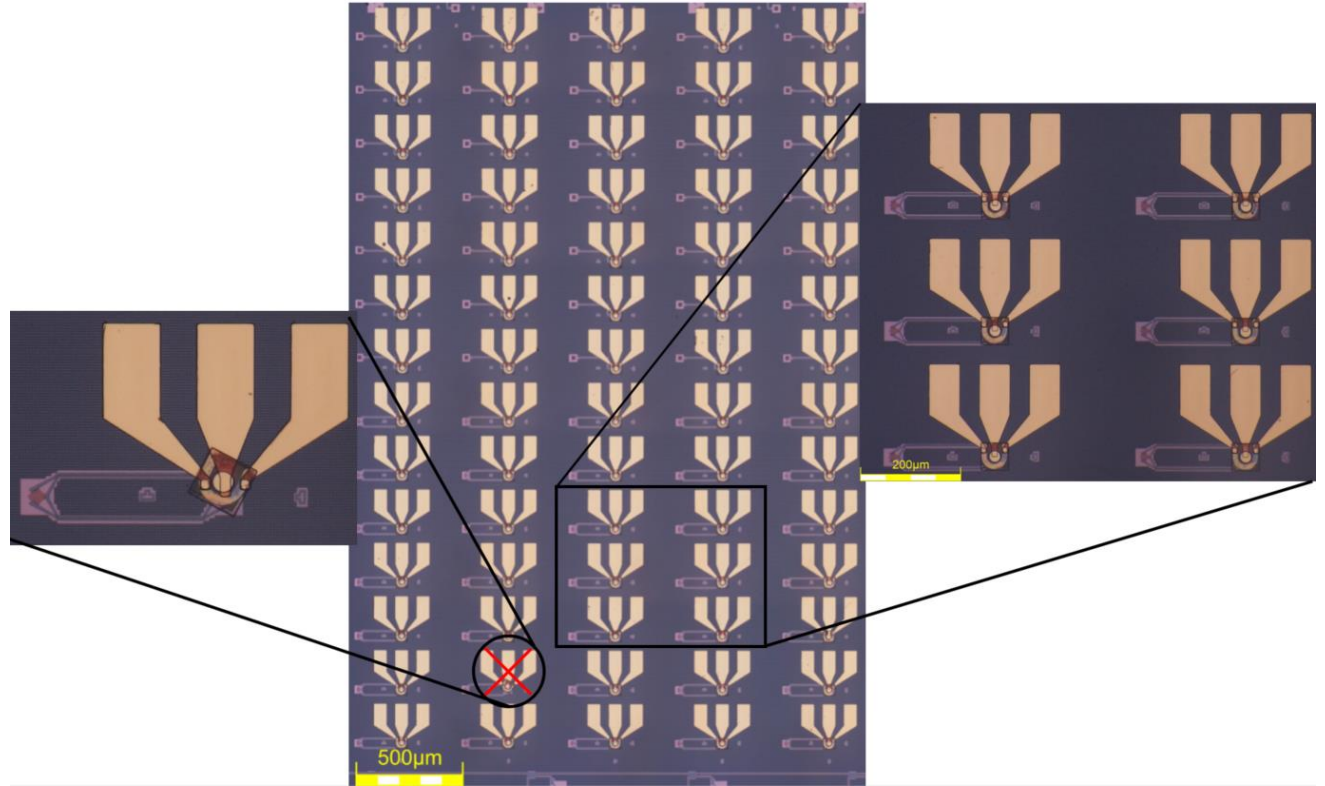


Fig. 7. Transfer printed bottom-illuminated devices after completing the post-processing. The inset on the left depicts the only device transfer printed with poor alignment accuracy.

3. DEVICE CHARACTERIZATION

3.1 IV characteristics

The IV characteristics of all 84 integrated devices were measured using DC probes. A typical IV of one device is shown in Fig. 8 a). All 84 devices show comparable IV characteristics with an average series resistance of $79\ \Omega$ (standard deviation $3\ \Omega$) and an average dark current of $0.9\ \mu\text{A}$ (standard deviation $0.3\ \mu\text{A}$). The histogram of series resistance and dark current are plotted in Fig. 8 b) and c) respectively.

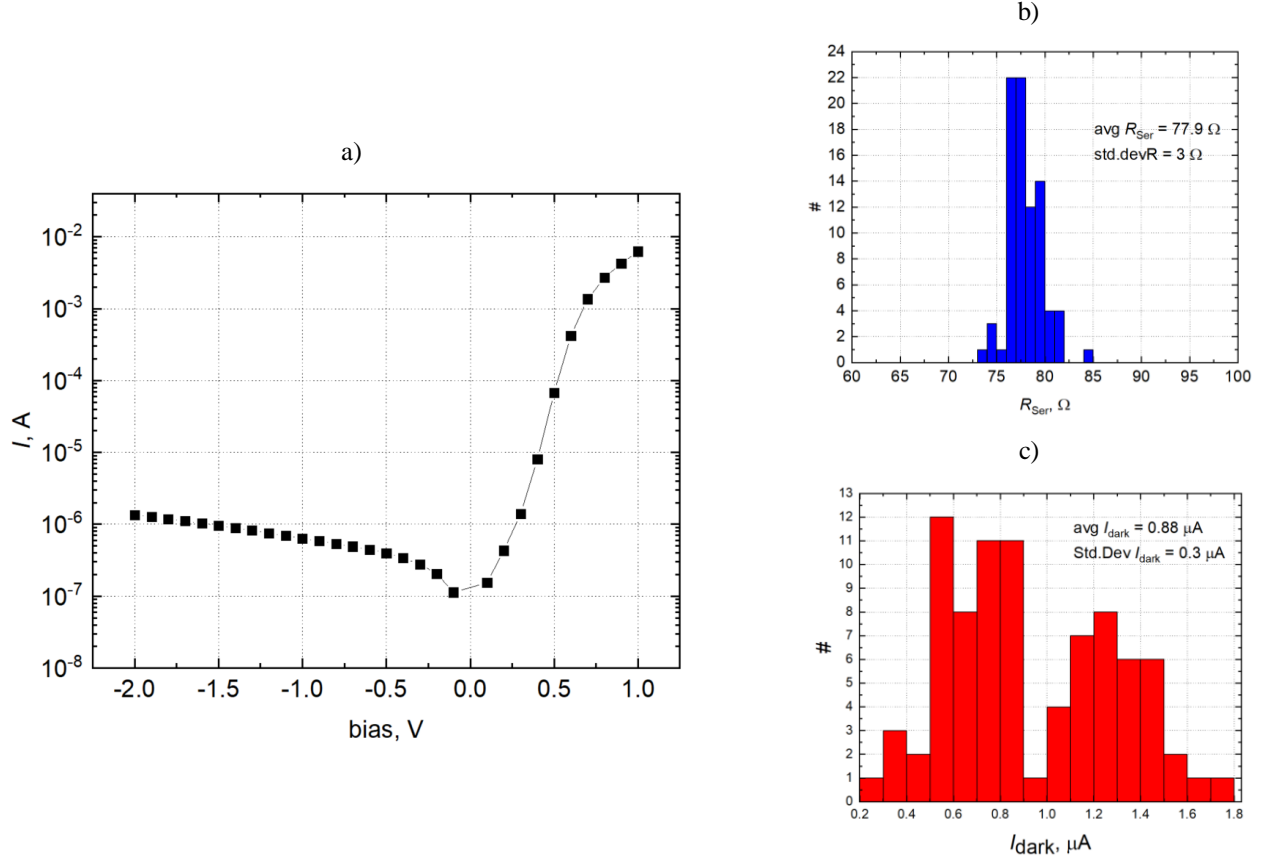


Fig. 8. a) A typical IV curve of one transfer printed photodiode; b) histogram of the series resistance of all 84 transfer printed photodiodes; c) histogram of the dark current of all 84 transfer printed photodiodes.

3.2 Responsivity

Using a Santec TSL510 tunable C-band laser and a 10 degree tilted single mode fiber, light was coupled into the silicon photonics chip (using a 1D or 2D grating coupler). The waveguide-referred responsivity of the 42 devices integrated on 1D grating couplers and its dependence on wavelength for a typical device is presented in Fig. 9 a). The responsivity increases with wavelength. This increase can be attributed to the increase of the directionality of the 1D grating coupler at longer wavelengths. Fig. 9 b) and c) display the histograms of waveguide-referred responsivities of all 42 devices integrated on a 1D grating coupler at 1550 nm and 1570 nm respectively.

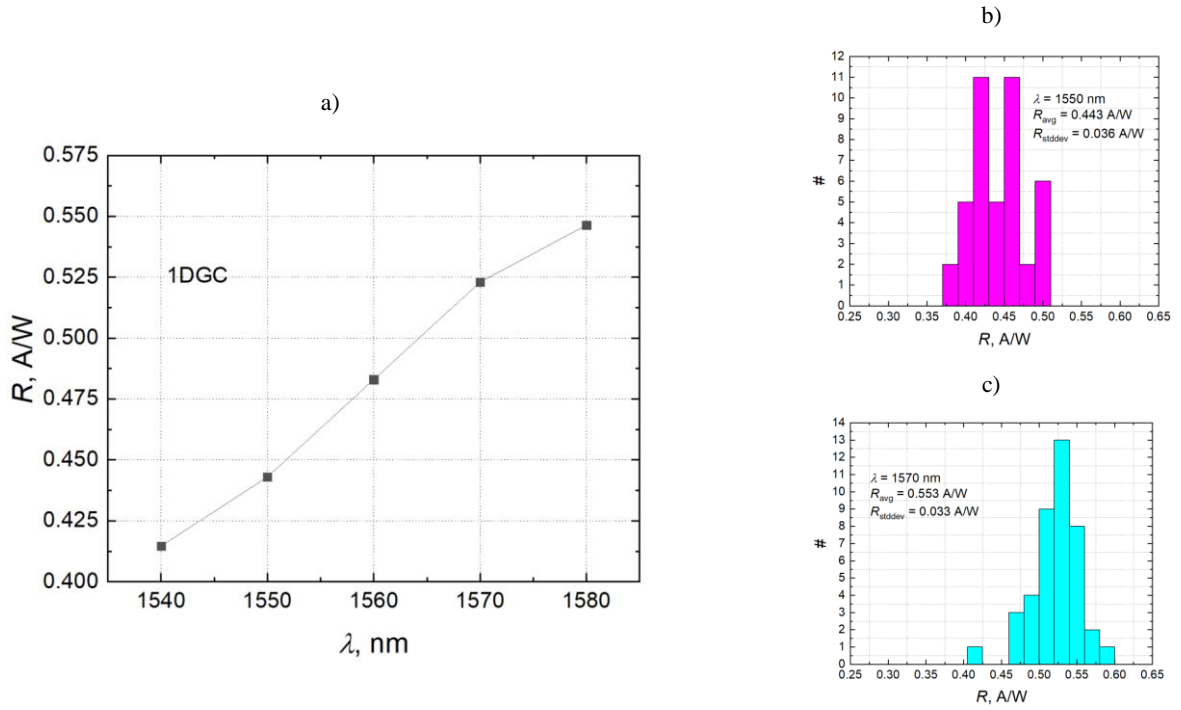


Fig. 9. a) Waveguide-referred responsivity for a typical device transfer printed on a 1D grating coupler. Histograms of the waveguide-referred responsivity at 1550 nm b) and at 1570 nm c) for the 42 photodiodes transfer printed on a 1D grating coupler.

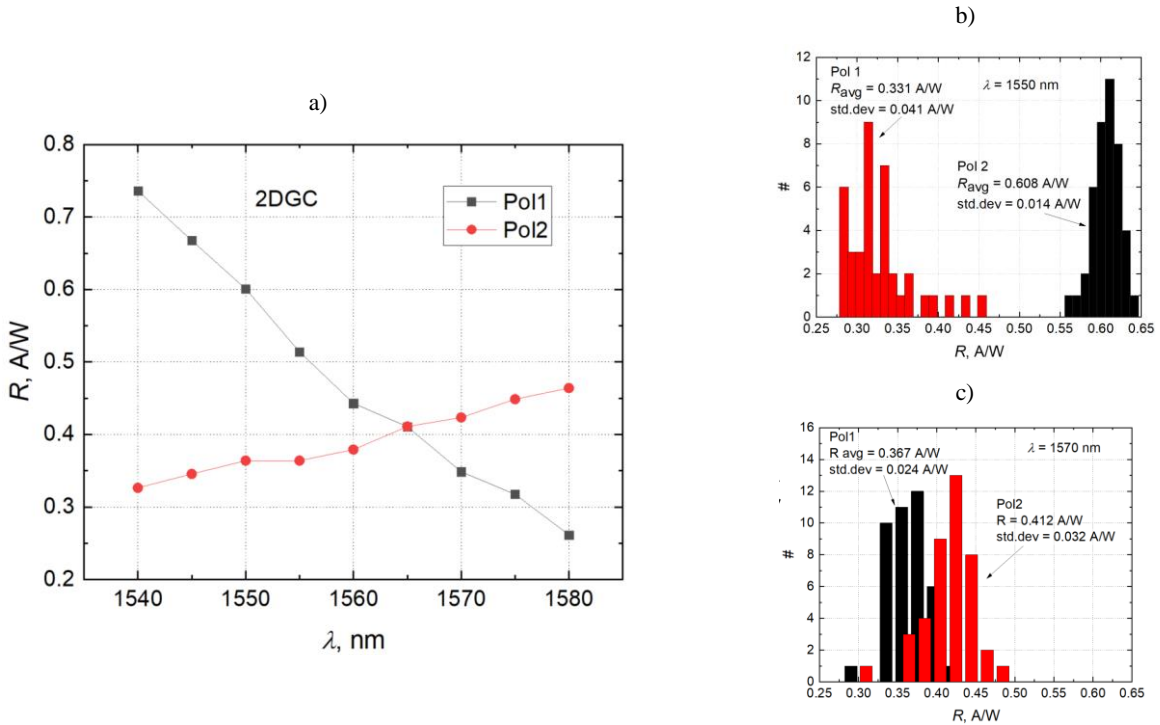


Fig. 10. a) Waveguide-referred responsivity for a typical device integrated on 2D grating coupler measured for both states of polarizations. b) histogram of responsivities at 1550 nm at polarization state 1 and 2; c) histogram of responsivities at 1570 nm at polarization state 2.

The waveguide-referred responsivity for photodiodes integrated on 2D grating couplers measured for two polarization states corresponding to the maximum and minimum response (denoted as Pol1 and Pol2) and its wavelength dependence is shown in Fig. 10.a). This behavior is not well understood at the moment and numerical simulations are necessary to understand these dependencies better. Fig. 10 b) and c) show the histogram for the waveguide-referred responsivity at 1550 nm and 1570 nm for polarization states 1 and 2 respectively for all 41 devices (the device printed with the noticeable misalignment was not taken into account).

3.3 Small Signal Measurement

The small signal response was measured using a vector network analyzer (VNA) using a Santec TSL510 tunable C-band laser and Mach-Zehnder modulator. The S_{21} parameter for different photodiode bias is displayed in Fig. 11 a). The histogram of the 3dB bandwidth of all the 83 transfer printed devices (3V reverse bias) is shown in Fig. 11 b). The 3 dB bandwidth spans between 12 and 14.4 GHz with an average value of 13.5 GHz.

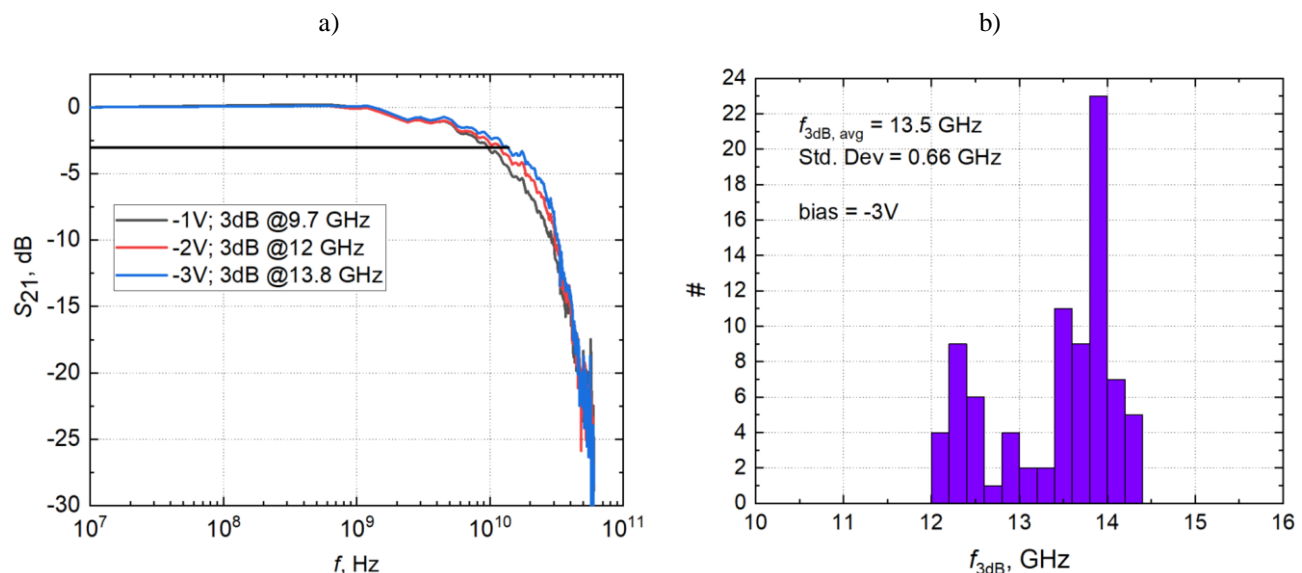


Fig. 11. a) S_{21} curve measured for one representative printed photodiode at different bias voltages. b) Histogram of 3dB bandwidths of 83 photodiodes, measured at -3V bias.

4. CONCLUSIONS

In this paper we demonstrated parallel transfer printing of substrate-illuminated III-V C-band photodetectors. We developed the photodiode fabrication and release processes, as well as the automated picking and printing of the devices. This demonstration showcases the advantages of transfer printing technology for scalable III-V-on-Si integration.

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