**Deep Levels in Metal-Oxide-Semiconductor Capacitors Fabricated on n-type In0.53Ga0.47As Lattice Matched to InP Substrates**

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**Abstract**

In this work, electron traps in n-type In0.53Ga0.47As hetero-epitaxial layers grown lattice-matched on n-type InP substrates by Molecular Beam Epitaxy have been studied by Deep-Level Transient Spectroscopy (DLTS). Metal-Oxide-Semiconductor (MOS) capacitors are employed, based on an Al2O3 gate oxide. It is shown that a single, near mid-gap electron trap dominates the DLT-spectra, whatever the surface pre- or post-gate oxide deposition treatment. At the same time, it is shown that the deep level parameters vary significantly from capacitor to capacitor and from wafer to wafer. Only after Forming Gas Annealing, a stable value for the activation energy of 0.39±0.01 eV is obtained. These results are tentatively interpreted in terms of antisite defects in the epitaxial layer, which form a family of related complexes with close deep-level parameters.

1. **Introduction**

Lattice-matched epitaxy of n-type In0.53Ga0.47As on InP substrates by liquid Phase Epitaxy (LPE) [1,2], Molecular Beam Epitaxy (MBE) [3,4] or Metal Organic Chemical Vapor Deposition (MOCVD) [4] gives rise to a number of grown-in point defects, which are determined by the growth conditions [5], i.e., the III/V ratio, the doping density, etc. These deep levels determine the non-radiative recombination and generation lifetime of the layers [6-8] and thus impact the dark current and the optical properties of photonic devices based on the InGaAs/InP materials system [9,10]. Determination of the important deep-level parameters (activation energy ET, capture cross section n,p and concentration NT) is routinely performed by Deep-Level Transient Spectroscopy (DLTS) [11-13]. One of the dominant grown-in point defects in InxGa1-xAs layers is the so-called EL2 antisite defect [4,5,14-16], also denoted as AsGa (AsIn) and giving rise to a near mid-gap donor level for a broad composition range x. Other native point defects with a low formation energy and thus a high probability for incorporation during non-equilibrium epitaxial growth are the gallium/indium vacancy (VGa/Vin) under Ga- or In-poor growth conditions [5]. Again, these defects could give rise to electron traps in the upper half of the band gap, although closer to the conduction band minimum EC.

Renewed interest on the impact of grown-in and processing-induced defects in InxGa1-xAs layers has been triggered by the potential implementation of so-called high-mobility channel materials, replacing silicon in future Complementary Metal-Oxide-Semiconductor (CMOS) technology nodes [7,17-21]. In this context, recent DLTS studies have been performed on Metal-Oxide-Semiconductor capacitors (MOScaps) fabricated on In0.53Ga0.47As/InP stacks [4,22], as it is difficult to fabricate low-leakage Schottky barriers on n-type InGaAs. Several electron traps have been detected and ascribed to bulk defects in the hetero-epitaxial layer. One particular effect which has been noted for the pronounced electron trap observed near mid-gap is that the DLTS peak position and, hence, the corresponding activation energy shifted markedly with processing and experimental conditions [5,22]. It is the aim of the present work to provide a more in-depth study to come to a better understanding and possibly an identification of the observed point defect levels. As will be shown for MBE-grown n-type material, the activation energy of the mid-gap electron trap in the range of 0.340 to 0.425 eV, narrows down to a single value of about 0.39±0.01 eV after Forming Gas Annealing (FGA). This implies first of all that the grown-in defects are sensitive to the thermal budget applied during processing and may transform into a more stable state. In addition, the wide spread in activation energy before FGA could indicate the presence of a family of near mid-gap antisite-like point defects.

1. **Experimental Details**

In a first batch of samples, MOScaps have been fabricated on 300 nm thick n-type In0.53Ga0.47As MBE layers on n-type InP substrates. In situ Si doping was applied, resulting in a doping concentration of around 1x1017 cm-3 [22]. Before gate stack formation by Atomic Layer Deposition (ALD) of 10 nm Al2O3, surface cleaning was performed using either (NH4)2S (for more details see, e.g., [23]) and abbreviated by AS or by an HCl native oxide removal only. Post-deposition FGA (10% H2+ 90% N2) was applied at 370 oC for 15 min for some of the wafers. The top gate was formed by a 50 nm Pt electrode and the back ohmic contact was prepared by a Mo metallization stack.

A second set of MBE-grown layers with a thickness of 800 nm received a net doping concentration in the range of 1×1017 cm-3, as derived from a 1/C2 (C the capacitance) versus reverse bias VR plot on the MOScaps. Surface treatment was performed by native oxide removal by HCl followed by sulfur passivation using ammonia sulfide (HCl+AS). The gate stack consisted of 10 nm ALD Al2O3 and a 100 nm nickel metal gate evaporated through a shadow mask, with a diameter of 0.5 mm.

MOScap characterization started with gate current-gate voltage (IG-VG) and gate capacitance (C) versus VG measurement at room temperature. A fixed frequency of 1 MHz of the Boonton capacitance bridge (30 mV amplitude) of the DLTS set-up was used. Cooling was performed in a liquid-nitrogen flow cryostat. Temperature-scan (T-scan) DLTS was executed during warming up from 75 K to around room temperature (RT), based on a Fourier-transformation of the measured capacitance transients (FT-DLTS). Spectra corresponding with different gate bias pulses from VR to VP were recorded in parallel, during the same temperature sweep. This enables to vary the spatial window across the In0.53Ga0.47As layer and to separate contributions from bulk traps in the depletion layer from the peaks belonging to interface states. Note that the reverse bias was chosen small enough that the depletion depth was well within the InGaAs layer, so that signals coming from the InP back interface can be ruled out. In addition, measurements have been performed for different pulse durations tp, keeping the pulse height and VR constant. This enables the study of the trap filling kinetics and to separate regular point defects in the InGaAs layer or at the interface with Al2O3, from border traps inside the gate dielectric [24-28]. Finally, the sampling period tw corresponds approximately with the period of the bias pulse and defines the electron emission rate window, together with the pulse duration tp. In first order, this corresponds approximately to tw/2, as determined more accurately by the numerical Fourier transform calculation for the b1 (sine) coefficient used to derive the DLT-spectra in this work.

1. **Results**

Figure 1 represents the spectra for the MOScaps corresponding with the four different surface pre- and post-treatments, aiming to reduce the density of interface states [6-8,23,29-32]. The same bias condition is employed, selecting a spatial window mainly in the depletion region of the InGaAs layer. The VP of -0.5 V is clearly below the flat-band voltage of the capacitor [22], so that mainly traps in the epitaxial layer will be filled with electrons during the bias pulse. At the same time, the edge of the depletion region is within the epitaxial layer, avoiding trap filling at the InP/In0.53Ga0.47As back interface. Only one electron trap is observed, however, its position is shifting between about 220 K (AS and HCl capacitors) and 205 K (AS+FGA and HCl+FGA case). This is also reflected in the corresponding Arrhenius plot of Fig. 2, showing an activation energy ET changing from 0.348 eV (AS) to 0.412 eV (HCl), similar as reported before [4,22]. Interestingly, the Arrhenius plots for the two samples after FGA overlap and yield the same ET=0.388 eV and close intercept value KT of 2.5×10-7 sK2.

One can also observe in Fig. 1 that the peaks are narrower after FGA than for their ‘as-processed’ counterparts, whereby mainly two wings at either side of the main peak are reduced or even eliminated. This has been interpreted in terms of a reduction of the density of interface states by hydrogen passivation [22], but could also point to a passivation of bulk traps in the InGaAs layer by H [8] or a thermal dissociation/transformation at 370 oC. At the same time, the trap concentrations NT, derived from the peak amplitude and the doping density of the layers is found in the range of 7×1015 cm-3 to 1.6×1016 cm-3, i.e., about 5 to10 % of the back-ground doping density [22] and is not markedly affected by FGA.

In order to further investigate whether the identical trap signature (ET,KT) for the two FGA samples is real or coincidental, DLT-spectra in Fig. 3 are compared for the HCl+FGA case for different VP values. The measurement corresponding with -1 V to 0 V should lead to a more efficient filling of interface traps close to the conduction band [12,33,34]. However, for both pulses, the same peak position and Arrhenius plot (Fig. 4) has been obtained. This strongly suggests that the electron traps for the FGA-treated samples are in the epitaxial In0.53Ga0.47As layer and not at the interface with Al2O3 [4,33]. According to Fig. 5, the peak in the HCl+FGA sample shifts as expected with the sampling period tw, showing the normal thermally activated behavior and at the same time, does not provide evidence for an anomalous trap filling kinetics. In other words, it reflects normal point defect behavior.

Further studies have been performed on the second set of samples, corresponding with the HCl+AS treatment and no FGA. According to Fig. 6, even for the same process condition, the dominant electron trap changes its maximum position and also the peak width. This can be nicely derived from the smallest peak, where the low-temperature flank overlaps with the one from the highest peak and the high-temperature side coincides with the one from the leftmost peak. Pulse conditions are again to promote bulk traps in favor of interface states. It suggests that perhaps several (similar?) near mid-gap levels are present in the as-processed capacitors, with similar yet different signatures.

The presence of interface states in the DLT-spectra is more clearly revealed in Fig. 7, corresponding with different bias pulses. It is expected that the contribution to the spectra of a broad distribution of shallow(er) interface states, close to the conduction band minimum EC will increase when VP approaches the flat-band voltage or even beyond VFB, going into accumulation of the MOScap (-0.5 V-->+0.2 V case) [33]. This is indeed what is seen in Fig. 7: besides the main electron trap, a shoulder develops at the low-temperature side (low activation energy), pointing to a high(er) density of acceptor-type interface states close to EC [29,35] (see also Fig. 1). This shoulder is absent for the other two pulses, emphasizing the fact that we are most likely probing bulk traps in the depletion region there. The corresponding Arrhenius plots are given in Fig. 8, showing rather similar activation energies for the -0.5 V-->+0.2 V and -1 V-->-0.5 V spectra, while a value of 0.51 eV is found for the ‘deepest’ bias pulse from -2 V -->-1 V. Note at the same time that the corresponding peak becomes significantly larger and more asymmetric, with a steeper decaying flank at higher temperatures.

A final experiment is represented in Fig. 9, showing spectra for a bias pulse in the depletion region and different pulse durations between 1 ms and 500 ms. Interestingly, also in this case, the peak position changes with tp, while the amplitude gently increases in the tp range between 1 ms and 500 ms. The latter could point to the contribution of the so-called slow capture phenomenon at the edge of the depletion region (so-called  region) [36-38]. Moreover, it is observed in Fig. 9 that the low-temperature side of the peaks overlaps between 10 ms and 500 ms, while this happens for the high-temperature side for the 1 ms and 10 ms spectra. Note also a significant broadening occurring for the peaks corresponding with a tp in the 10 to 500 ms range. The corresponding Arrhenius plot in Fig. 10 exhibits a slight, but not systematic variation in ET and electron capture cross section n with tp.

1. **Discussion**

Summarizing the main experimental data: in MBE-grown n-type In0.53Ga0.47As layers on n-type InP substrates a dominant electron trap is observed, with activation energy around mid-gap. Similar results have recently been reported on nominally undoped intrinsic MBE layers with residual n-type behavior, showing a dominant Eb1 peak in the 200-250 K range and exhibiting a low-temperature shoulder Eb2 [4]. The corresponding activation energy for Eb1 was found shifting from 0.38 eV to 0.46 eV when the reverse bias was changed from -0.1 V to -1.5 V, like in Figs 7 and 8 in our case. Eb2 has an activation energy of 0.37 eV, not moving with reverse bias. The Eb1/Eb2 traps were assigned to grown-in native defects, possibly EL2 antisites [4]. This interpretation is supported by previous DLTS data on MBE-grown n-type InxGa1-xAs [3,15,16] and by recent ab initio Density Functional Theory (DFT) calculations [5]. In the latter case, it has been shown that under Ga-poor growth conditions, the AsGa antisite has the lowest formation energy of the intrinsic defects and is thus likely to be introduced during epitaxial growth. Also Ga vacancies (VGa) will have a good probability to be formed during MBE.

As we believe that in our case we are also dealing with native point defects, it is logic to assign the dominant electron trap(s) to an antisite type of defect. In fact, it has been suggested in the past that the EL2 defects in GaAs consist of a family of related defects [39], involving the AsGa antisite [40] and other native point defects (VAs and/or VGa) [41-43]. The presence of multiple AsGa-related complexes with similar deep levels (or perhaps more precisely, similar electron emission rates at the same temperature) could well explain most of the atypical behavior observed here: the variation of the activation energy from sample to sample, even within the same wafer (Fig. 6) or from wafer to wafer (Fig. 1). We can add here that the surface pre-cleaning before the deposition of the Al2O3 dielectric is not playing a key role. This can be derived from the fact that after FGA, exactly the same peak can be found whether HCl or AS treatment is applied (Figs 1 and 2). Still, it is remarkable that after FGA at 370 oC, one single energy level appears (Figs 2 and 4), indicating a single trap species responsible for it. Apparently, application of a thermal budget in this temperature range singles out the more stable complex among the different family members and stabilizes the antisite configuration. Annealing studies in a broader temperature range and in inert or hydrogen containing atmospheres should further strengthen this hypothesis.

While the interpretation presented above seems to explain most of the experimental observations, a few aspects deserve further critical discussion. An alternative explanation for the broad(er) peaks observed in Figs 1, 6 and 9 could be the effect of alloy broadening on the natural width of a DLTS peak [44]. This is related to the fact that in a ternary alloy, the atomic environment around for example a simple point defect can vary with respect to the number of In versus Ga nearest and/or second nearest neighbors. This gives rise to small local potential variations and spreads the energy level of the defect, giving rise to a broader DLTS peak. However, such alloy broadening only affects the amplitude of the peak, keeping the temperature position and ‘average’ activation energy the same [44], which is clearly not observed here.

A second factor is the change in the activation energy with measurement conditions, observed for example in Fig. 7 and similar to the results reported in Fig. 15 of Ref. [4]. This can be interpreted in terms of an electric-field effect on the electron emission rate, caused by the reduction of the activation energy with more positive reverse bias [12]. Such electric field behavior is in support of a possible donor nature of the observed defects, where Poole-Frenkel barrier lowering occurs due to the attractive trap potential for electrons [45-47]. However, alternative explanations are also possible. It has for example been noted in the past that the activation energy of EL2 in GaAs depends on the Schottky barrier height. This has been ascribed to a change in the trap occupancy factor, defined by the ratio of the trap emission time constant and the trap filling rate [48,49]. This can affect the effective activation energy of the deep level derived from the slope of an Arrhenius plot, even causing a complete disappearance of EL2 from the spectrum [48,49]. The observation in Fig. 7 that the DLTS peak shifts with reverse bias in the same sample rules out the impact of for example the metal work function of the MOScap (the equivalent parameter as the barrier height for a Schottky contact) on the obtained results. In fact, the two sets of samples studied here have been processed with a different metal gate, showing similar tendencies, so that the gate stack is not an important factor in the observed shift of the DLTS peak position.

However, what certainly must be considered in the present experiments is the occurrence of the minority carrier response in a MOScap, during the relaxation of the capacitance after the bias pulse from deep depletion into accumulation [50-53]. Minority carriers (holes) generated during the transient period will be attracted by the negative gate bias, building up an inversion layer at the In0.53Ga0.47As/Al2O3 interface. This gives rise to an increase in the capacitance, similar as for electron emission from a filled trap in the depletion region and results in a positive DLTS peak, appearing like a majority carrier signal, although the physical origin is different [50,51]. It is either minority carrier diffusion from the bulk, yielding an activation energy of the band gap EG or minority carrier generation through the Shockley-Read-Hall mechanism, normally giving an activation energy of ~EG/2. Particularly for semiconductor materials with a narrow band gap, this effect may become pronounced and can occur below room temperature. Criteria to recognize the phenomenon are among others a huge amplitude, as potentially the capacitance wants to increase from the value in depletion to the one in inversion, which is similar as the oxide capacitance in accumulation. In addition, the transient is non-exponential in nature, giving rise to huge, asymmetric DLTS peaks.

While this is not the case for most of the spectra reported here, the peak in Fig. 7, corresponding with a pulse from -2 V to -1 V satisfies the above criteria and is thus a candidate minority carrier response peak. In addition, the corresponding activation energy is already quite large and falls outside the typical range observed for the other conditions (0.34 eV to 0.425 eV). In this context, it should be remarked that minority carrier generation lifetime analysis in n-type In0.53Ga0.47As (grown by Metal-Organic Vapor-Phase-Epitaxy (MOVPE) yields an activation energy of ~0.31 eV [6] at room temperature and below. Typical values for a doping density in the range of 1016 cm-3 to 1017 cm-3 are 5x10-9 s to 10-10 s at room temperature, reducing with increasing doping concentration [8]. In other words, the generation lifetime appears to be dominated by a mid-gap deep level – possibly the same as the EL2-like electron trap(s) observed by DLTS here – and, furthermore, reduces with increasing doping density. This indicates that the occurrence of minority carrier response during a typical sampling period of 51.2 ms around 200-250 K is not unlikely and in addition, should become more pronounced for increased sampling time tw (although not observed in Fig. 5) or with increased doping density.

A final fact that needs further discussion is the impact of the pulse duration on the peak shape and position in Fig. 9. While to the Authors’ best knowledge such an effect has not been reported before, it could be well explained in terms of a number of closely spaced deep levels contributing to the overall peak. At shorter tp, the one with the largest n would dominate, with saturating amplitude at 1 ms. For longer pulse times, the slower trap levels can cause a further increase in the peak amplitude and also a shift in its peak position. In addition, slow capture typically occurs at the edge of the depletion region, corresponding with a lower electric field. Hence, at longer pulse times, electron emission will occur at lower average electric field, shifting the peak maximum towards higher temperatures, like in Fig. 7. Perhaps double correlation DLTS measurements could be set up to separate the contribution of the electric field from the one determined by slow capture at the edge of the depletion region and address this question.

1. **Conclusions**

A detailed DLTS study of n-type MBE-grown In0.53Ga0.47As lattice-matched to n-type InP substrates reveals a dominant type of grown-in native point defect with near mid-gap activation energy. The variation of the deep-level parameters is explained in terms of a family of closely related AsGa-based point-defect complexes, with similar parameters and contributing to the spectra. In addition, the possible electric-field dependence of some of the deep levels further contributes to the shift of the peak position and the activation energy. It is also shown that a FGA stabilizes the trap signature to a value of 0.39±0.01 eV. It is believed that this defect(s) dominates the Shockley-Read-Hall lifetime in these epi layers. Finally, the occurrence of a minority carrier DLTS response peak under large reverse bias should be considered and can explain the variation of the activation energy to rather large values.

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**Figure Captions**

Fig. 1. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on an n-type In0.53Ga0.47As MOScap with Al2O3 gate dielectric and different surface pre-treatments (HCl or AS), with or without a post-growth FGA at 370 oC.

Fig. 2. Arrhenius plot corresponding with the spectra of Fig. 1. Measurements have been performed on an n-type In0.53Ga0.47As MOScap with Al2O3 gate dielectric and different surface pre-treatments (HCl or AS), with or without a FGA at 370 oC.

Fig. 3. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V and from -1 V to 0 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on an n-type In0.53Ga0.47As HCl+FGA MOScap .

Fig. 4. Arrhenius plot corresponding with the spectra of Fig. 3, for an n-type In0.53Ga0.47As HCl+FGA MOScap .

Fig. 5. DLT-spectra corresponding with a bias pulse from -1 V to 0 V and three different sampling periods. Measurements have been performed on an n-type In0.53Ga0.47As HCl+FGA MOScap.

Fig. 5. Arrhenius plot corresponding with the spectra of Fig. 1. Measurements have been performed on an n-type In0.53Ga0.47As MOSCAP with Al2O3 gate dielectric and different surface pre-treatments (HCL or A), with or without a FGA at 350 oC.

Fig. 6. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As on InP substrate. No FGA has been applied.

Fig. 7. DLT-spectra corresponding with a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Different bias pulses have been applied. Measurements have been performed on Al2O3 gate dielectric MOSCAPs fabricated on MBE-grown n-type In0.53Ga0.47As on InP substrate. No FGA has been applied.

Fig. 8. Arrhenius plot corresponding with the spectra of Fig. 7. Different bias pulses have been applied. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As. No FGA has been applied.

Fig. 9. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As. No FGA has been applied.

Fig. 10. Arrhenius plot corresponding with the spectra of Fig. 9. Different bias pulse durations from -1 V to -0.5 V have been applied.



Fig. 1. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on an n-type In0.53Ga0.47As MOScap with Al2O3 gate dielectric and different surface pre-treatments (HCl or AS), with or without a post-growth FGA at 370 oC.



Fig. 2. Arrhenius plot corresponding with the spectra of Fig. 1. Measurements have been performed on an n-type In0.53Ga0.47As MOScap with Al2O3 gate dielectric and different surface pre-treatments (HCl or AS), with or without a FGA at 370 oC.



Fig. 3. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V and from -1 V to 0 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on an n-type In0.53Ga0.47As HCl+FGA MOScap.



Fig. 4. Arrhenius plot corresponding with the spectra of Fig. 3, for an n-type In0.53Ga0.47As HCl+FGA MOScap .



Fig. 5. DLT-spectra corresponding with a bias pulse from -1 V to 0 V and three different sampling periods. Measurements have been performed on an n-type In0.53Ga0.47As HCl+FGA MOScap.



Fig. 6. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As on InP substrate. No FGA has been applied.



Fig. 7. DLT-spectra corresponding with a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Different bias pulses have been applied. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As on InP substrate. No FGA has been applied.



Fig. 8. Arrhenius plot corresponding with the spectra of Fig. 7. Different bias pulses have been applied. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As. No FGA has been applied.



Fig. 9. DLT-spectra corresponding with a bias pulse from -1 V to -0.5 V, a sampling period tw=51.2 ms and a pulse duration tp=1 ms. Measurements have been performed on Al2O3 gate dielectric MOScaps fabricated on MBE-grown n-type In0.53Ga0.47As. No FGA has been applied.



Fig. 10. Arrhenius plot corresponding with the spectra of Fig. 9. Different bias pulse durations from -1 V to -0.5 V have been applied.