A 21-GS/s Single-Bit Second-Order ΔΣ Modulator for FPGAs

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Abstract— **A new high-speed delta-sigma modulator (DSM) topology is proposed by cascading a bit reduction process with a multi-stage noise shaping MASH-1-1 DSM. This process converts the two-bit output sequence of the MASH-1-1 DSM to a single-bit sequence, merely compromising the DSM noise-shaping performance. Furthermore, the high clock frequency requirements are significantly relaxed by using parallel processing. This DSM topology facilitates the design of e.g. wideband software defined radio (SDR) transmitters and delta-sigma radio-over-fiber transmitters. Experimental results of the FPGA implementation show that the proposed low-pass DSM can operate at 21 GS/s, providing 520 MHz baseband bandwidth with 42.76 dB signal-to noise-and-distortion ratio (SNDR) or 1.1 GHz bandwidth with 32.04 dB SNDR (based on continuous wave measurements). An all-digital transmitter based on this topology can generate 218.75 MBd 256-QAM over 200 m OM4 multimode fiber in real-time, with 7-GS/s sampling rate and an error vector magnitude below 1.89%.**

Keywords— Delta-Sigma modulator, multi-stage noise shaping (MASH), software defined radio, quantization noise, FPGA

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