Design and Implementation of a Gate Driver Circuit for Three-Phase Grid Tide Photovoltaic Inverter Application

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***Abstract*— This paper presents and describes the design and implementation of a new gate driver circuit for a three-phase grid tide photovoltaic inverter system using SIC- MOSFET at the power stage. The proposed design consists of a 5 kW power three-phase inverter system with a new isolated gate driver related to IGBT, MOSFET and SIC-MOSFETs. The designed circuit has a dual gate driver in a single package for each leg, and each circuit has an optocoupler to provide high output peak current to turn the power transistor On or Off, and a saturation protection circuit. The control algorithm for the full system of the three-phase application runs on a TMS320F28335 DSP. The TMS320F28335 Digital Signal Processor (DSP) microcontroller is one of the Texas Instruments™ (TI) family that was used to generate the three-phase 120^{o} Bus Clamp PWM of the system, with high frequency around 25 kHz.**

Keywords—Gate Driver Circuit; SIC-MOSFET; Saturation Protection; TMS320F28335; 120^{o} Bus Clamp PWM.

I. INTRODUCTION

One of the most important parts of every electronic power system is the gate drive circuit, which connects the power transistor with the microcontroller. For this reason, the choice of gate driver circuit is closely related to the output power and reliability of the inverter/converter solution. Inadequate driver power or the wrong driver option may cause a malfunction in the driver circuit. Low power applications predominantly require a safe and low–cost, efficient driver solution for power applications. Gate driver circuits are one of the necessary links. They have to drive power transistors (IGBTs, MOSFETs and SIC transistors) and feature high output voltage and current capabilities with gate driver voltages are, typically, up to 20V.

There are different types of gate driver circuit for MOSFET, IGBT, and SIC-MOSFET. Most types of gate driver circuits are classified by configuration, with the amount of input DC power supply, the gate driver impedance, and the type of power transistor package, together determining the maximum output supply of voltage and current [1]–[8]. A bootstrap circuit is often used as the gate driver circuit for IGBT and MOSFET [9]–[12], however, it is not safe as the controller is not separated, when any faults occur.

One of the problems facing high voltage circuit designers is controlling the voltage of the power transistor's gate driver with high safety isolation [13]–[16]. In this paper, a new SIC-MOSFET gate driver circuit is shown, with the following specifications

- Provide positive output voltage to Turn-On and negative voltage to Turn-Off the power transistor to reduce the effect of the voltage induced by the parasitic source inductance (the output voltage is about 19V for On and -5V for Off).
- Full isolation between power circuit and microcontroller.
- This circuit works for each type of power transistor in the inverter.
- Reducing the parasitic capacitance to a very low value. This capacitance injects ground currents into the microcontroller that can disturb signals of DSP controllers.

The SIC-MOSFET gate driver circuit is designed to work with the majority of industrial applications, using a three-phase photovoltaic inverter, with DC link voltage up to 1000 V. Different types of PWM techniques are used to control the three-phase photovoltaic inverters, but in this paper, the SIC-MOSFET three-phase inverter system was used, with a 120º Bus Clamp PWM as a new control technique to test the full system [17]–[20]. The 120º Bus Clamp PWM signals were generated by the TMS320F28335 [21]. The silicon carbide power MOSFET CMF10120D is used in this paper [22].

The regulation of this paper is as follows: Section 2 presents the description of the driver circuit; Section 3 presents the driving control for the gate driver circuit; Section 4 presents the experimental set-up and results; and finally, Section 5 presents the conclusions.

II. Description of The Driver Circuit

In this section, we discuss the full performance of the SIC-MOSIT gate driver circuit. This circuit can be divided into two main parts: the gate driver circuit, and low side input DC power supply.

A. SIC-MOSFET gate driver circuit

The circuit diagram in Fig. 1. presents the full SIC-MOSFET gate driver circuit topology for one leg of the three-phase photovoltaic inverter used in this paper. This circuit has two gate driver circuits for two transistors (upper and lower) for each phase, and each circuit has three main parts,

1. *microcontroller isolated circuit*: In this circuit, The ACPL-P304 optocoupler chip was used as an optoisolator between the TMS320F28335 kit and the gate driver circuit.
2. *saturation protection circuit*: This circuit was designed to protect the full gate driver circuit from the AC output high voltage and current by turning off the gate driver signals when any output error occurs.
3. *low voltage isolated power supply circuit*: In this circuit, a transformer was used to achieve galvanic isolation of the low voltage side. The main properties of this circuit are:

- galvanic low DC power supply isolation;
- can obtain DC power supply for all circuit elements; and
- can obtain positive and negative voltage for On- and Off-position of the gate for high power transistors.

The transformer is the main part of this circuit and can be made with a very low primary to secondary capacitance of 2 pF, while using winding in separate rooms, together with 2 pF of the optocoupler; a total amount of 4 pF is reached.

B. Low DC power supply

The low DC power supply circuit is divided into two parts, the first part, in Fig. 2a., is designed to provide supply voltage (3.3, 5 and 9)V for the current and voltage measuring circuit. The DC input of the power supply circuit is generated by using a 220V AC to 24V DC converter.

The second part, in Fig. 2b.,, was designed as a square wave generator circuit that allows for changeable frequency and amplitude of the input DC power supply signal. This circuit is simply built of a few resistors, capacitors, a 555 timer chip, and high speed gate drivers. The square waveform output (high to low) varies approximately between +VCC and -VCC, according to the DC power supply. The required times to calculate a single cycle charge and discharge for output waveform is presented in equations 1 to 4 and the duty cycle of the square wave output signals are calculated in equation 5.

$$t_1 = 0.693 * (R_1 + R_2) * C \quad (1)$$

$$t_1 = 0.693 * R_2 * C \quad (2)$$

$$T = t_1 + t_2 \quad (3)$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) * C} \quad (4)$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)}\% \quad (5)$$

Where:

Charge Time (t1) and Discharge Time (t2)

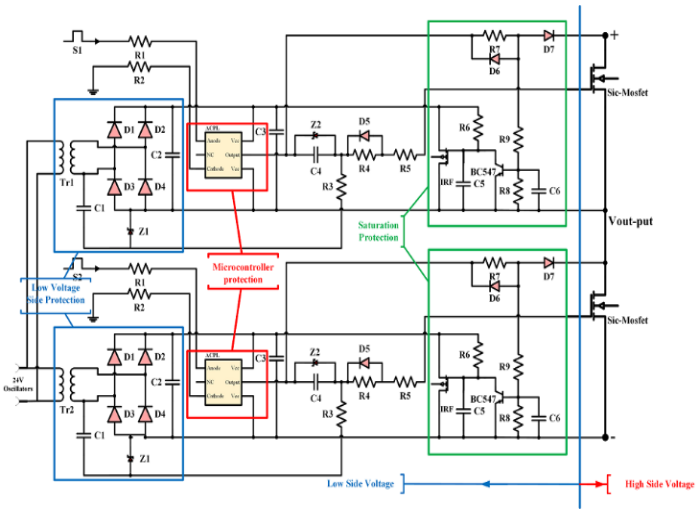
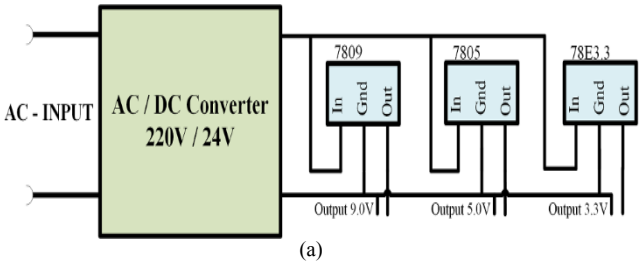
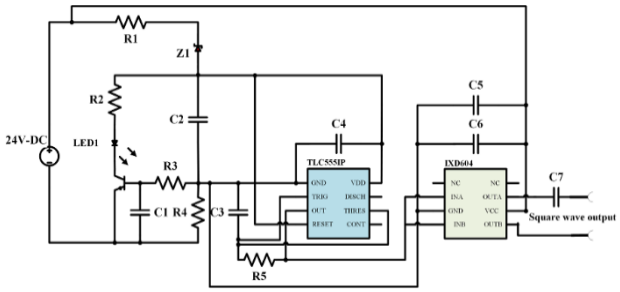


Fig. 1. One leg SIC-MOSFET gate driver circuit.



(a)



(b)

Fig. 2. DC power supply.(a) Low DC power supply circuit, (b) Square wave generator circuit.

III. DRIVING CONTROL FOR GATE DRIVER CIRCUIT

The DSP TMS320F28335 system development kit in the Fig. 3. is a complete board used to generate the 120º Bus Clamp PWM with high frequency (around 25KHz) for three-phase photovoltaic inverter gate driver circuit with SIC-MOSFET transistors. The main properties of the development microcontroller kit is presented in Table I [20].

Fig. 3. TMS320F28335 system development kit.

TABLE I. SPECIFICATIONS OF TMS320F28335

Device Frequency	Up to 150 MHz
Core Voltage	1.9-V/1.8-V
Input/output voltage	3.3V
No. of PWM Channels	18
No of ADC	12-Bit ADC, 16 Channels
No of Input/output Channels	GPIO0 to GPIO63
Temperature Options	–40°C to 125°C

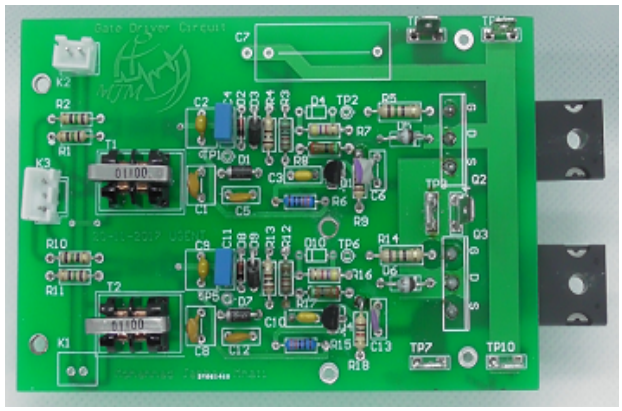
IV. EXPERIMENTAL SET-UP AND RESULTS

Fig. 4. shows the final practical circuit of the one leg circuit of the three-phase photovoltaic inverter. The SIC-MOSFET gate driver circuit is built on a two-layer PCB, using different types of components: SMT and SMD. The advantage of this circuit is that it uses only one DC voltage power supply for control and driving circuits.

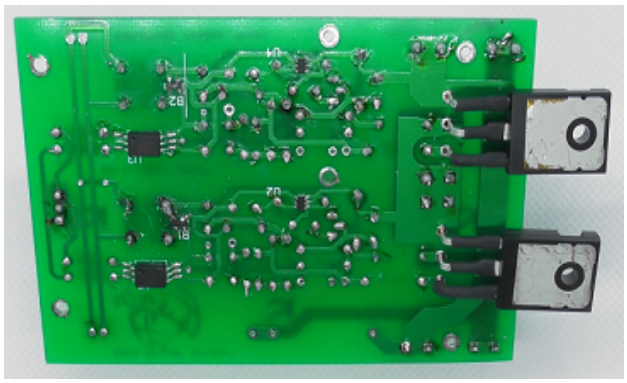
Fig. 5a. presents the DC power supply circuit. The orange box is the AC/DC converter to get the 24V DC power supply and the 9, 5, and 3.3V DC/DC converter. The final DC power supply circuit for the gate driver circuit, in Fig. 5b., has a design based on square wave power supply voltage. This circuit is used to convert the DC voltage to square wave voltage, with high frequency.

The main advantage of the circuit design in this paper is to generate negative bias during turn-off of the high power transistors (MOSFET, IGBT, and SIC-MOSFET) and full circuit isolation. The negative bias during turn-off still helps the faster turn-off and prevents false cycle even in an electrically noisy environment. The low DC voltage isolated in the gate driver circuit by using 1:1 transformer.

Table II presents the main properties of the SIC-MOSFET (CMF10120D) that was selected for this paper [21].

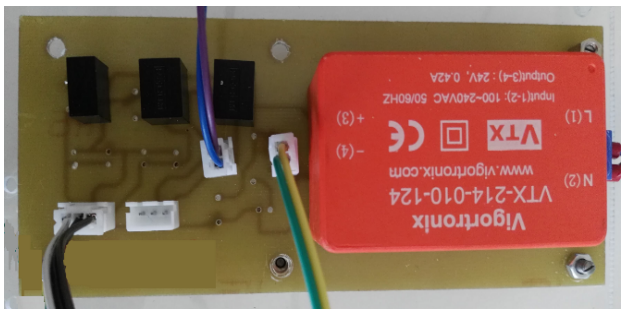


(a)

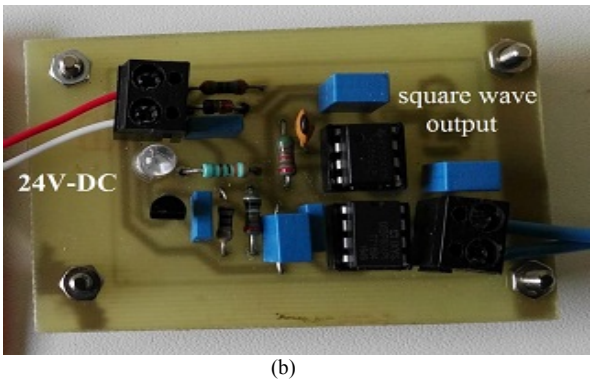


(b)

Fig. 4. Practical of one leg SIC-MOSFET gate driver circuit: (a) Upper layer , (b) Lower layer



(a)



(b)

Fig. 5. DC power supply circuit. (a) (9, 5 and 3.3)V power supply circuit, (b) Practical square wave generator circuit.

TABLE II. MAIN PROPERTIES OF SIC-MOSFET CMF10120D

Parameter	Value
Drain-Source Resistance RDS(on)	Very low
Diode Forward Voltage VSD	High voltage (about 4V),
The output (dI/dt)	Very High
The higher gate voltage	Typically –5V to 20V

Fig. 6. shows the Full system of the three-phase photovoltaic inverter with SIC-MOSFET gate driver, TMS320F28335 microcontroller, square wave voltage power supply, and three-phase current and voltage measuring circuit.

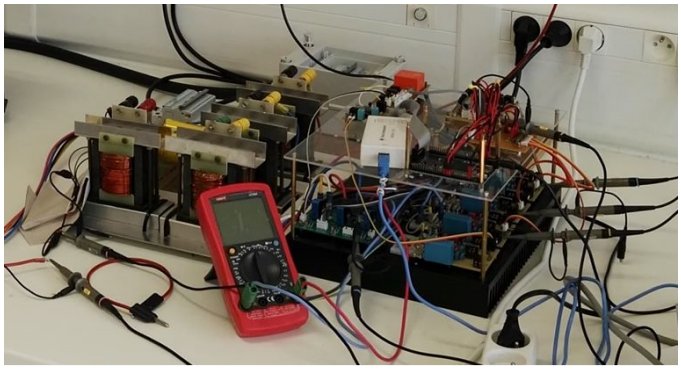
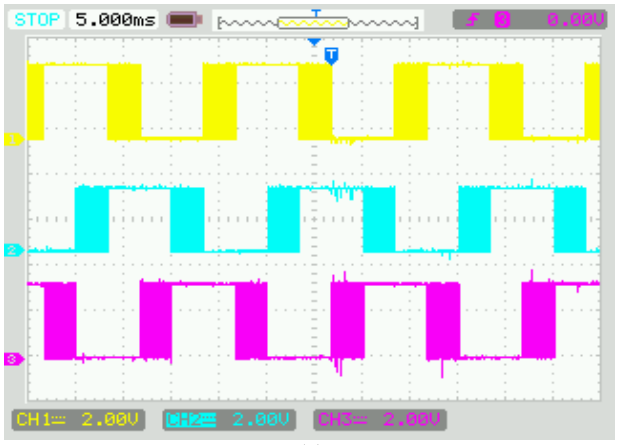


Fig. 6. Full system of three-phase inverter with SIC-MOSFET gate driver circuit

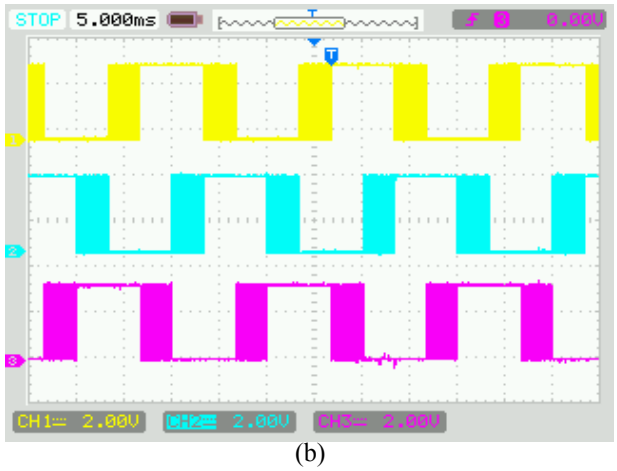
The experimental results of the three-phase inverter circuit, shown in Fig. 7. to Fig. 9., were obtained to check the performance of the power sources from the gate driver circuit, with only one DC power supply. Fig. 7. shows the 120^{o} Bus Clamp PWM switching waveforms of the three-phase inverter, under control by using TMS320F28335. The 120^{o} Bus Clamp PWM technique of the three-phase inverter means that every 60^{o}, only one phase under PWM control and the others phases are On or Off [18,20] .

The 120^{o} Bus Clamp PWM technique is shown in Fig. 7., while the output waveform of leg A gate driver circuit with negative voltage is presented in Fig. 8a. The maximum and minimum voltage of the gate driver circuit are, with negative value, (19V and -5V) respectively. Fig. 8b. presents the dead time between the upper and lower signals of leg A.

The output voltage and current of the three-phase photovoltaic inverter is shown in Fig. 9. The maximum value of the output voltage circuit is dependent on the maximum value of the DC link supply voltage.

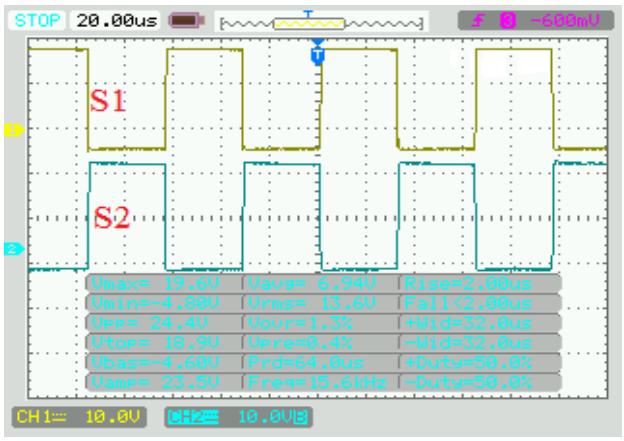


(a)



(b)

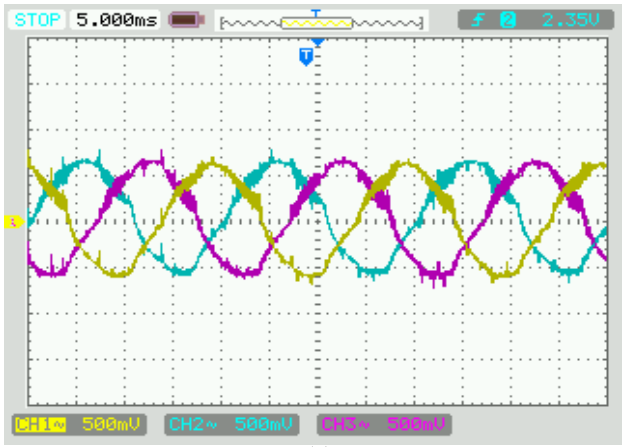
Fig. 7. Three-phase 120^{o} Bus Clamp PWM technique. (a) S1, S3 and S5 PWM; S4, S6 and S2 signals



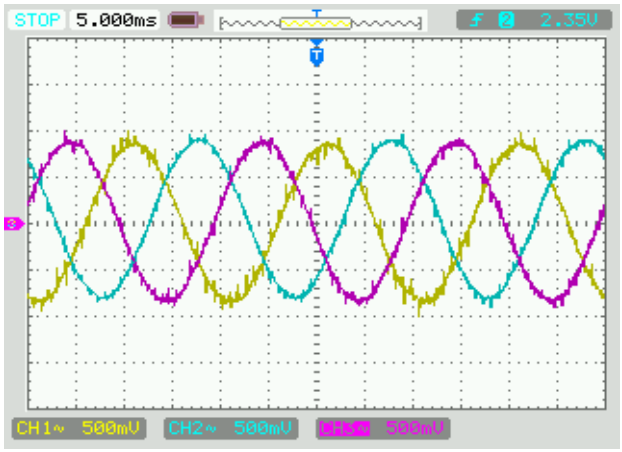
(a)

(b)

Fig. 8. The output waveform of leq A gate driver circuit. (a) S1 and S2 signals; (b) dead time between S1 and S2 signals.



(a)



(b)

Fig. 9. The output waveform: (a) three-phase voltage; (b) three-phase lines current.

V. Conclusion

The main aim of this paper is to design and implement MOSFET, IGBT, and SIC-MOSFET gate driver circuit. The circuit design is based on a three-phase photovoltaic inverter for an industrial environment and real time application. The present paper describes the full driver circuit and presents the measured output waveform of the designed gate driver circuit, and the output voltage and current of the three-phase inverter. The designed circuit of the gate driver presented in this paper can provide negative (-4V) and positive (+20V) output gate driver voltages with high frequency. The PWM for the presented three-phase inverter is a 120° Bus Clamp PWM control method and PWM singles generated by using TMS320F28335 as a microcontroller.

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