Networked sensing architecture using oversampling techniques in PROFINET IRT devices and isochronous mode processing: proof-of-principle and signal reconstruction at IO Controller side

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Abstract

The revamping of a machine manufacturer's line of high speed processing machines aims to reuse existing validated STEP 7 code. The distributed networked sensing architecture is required to pick out a single analog measurement with 50 µs resolution at specific encoder sample hits, using off-the-shelf PROFINET I/O.

A solution using an oversampling technique on a remote I/O device combined with a low-cost "streaming CPU" running in isochronous processing mode and acting as sync master in PROFINET IRT is proposed. The distributed architecture connects a main CPU to the streaming CPU, the latter configured as I-Device in a 2nd PROFINET RT network.

Overall distributed architecture, accurate reconstruction of the signal timing, network load and the signal propagation are analysed.

1. Introduction

A machine manufacturer wants to revamp its line of high speed processing machines, reusing as much as possible existing validated software code for S7-3xx PLCs, and preferably with off-the-shelf networked analog I/O.

Current machines use expensive CAM-instrumentation to sample analog signals triggered at specific encoder positions, combined with PLCs and networked I/O for other automation tasks. For continuous on-line quality control, the machine takes between 5 to 10 analog measurements per round of a turntable, triggered by different encoder positions and requiring at least 12 bit resolution. The signal itself is trapezium shaped, and the value to be measured is the top part which is only 56 µs wide at full speed.

The reused validated S7 software is to run on new S7-15xx controllers, using PN (PROFINET) [1] as industrial network. Specifications are faster than the shortest PROFINET IRT cycle (250 µs), requiring either non-standard expensive CAM-instrumentation or oversampling techniques in the PROFINET IO Device.

Oversampling inside PROFINET IO Devices is not (yet) supported by many vendors, and very rarely used. The demanding oversampling application discussed in this paper raises the questions of 1) triggered measurement on specific encoder positions 2) accurate reconstruction of the timing of the signals at the IO Controller (PLC) side and 3) determination of the overall maximum signal propagation delay.

In this paper, a low-cost off-the-shelf networked architecture is proposed and validated. The remainder of this paper is organized as follows: basic design and overall architecture is discussed in section 2, signal reconstruction delivering proof-of-principle is in section 3. Section 4 discusses the analysis of the signal timing at both analog and Ethernet level, and the signal propagation in the networks and CPUs.

2. Basic design and overall architecture

2.1. Data acquisition

Some initial trials with "off-the-shelf" alternatives quickly proved to be insufficient:

- The fastest local (mounted on a S7-15xx PLC backplane) analog card only has a minimum sample time of 62.5 µs (which is insufficient), has no oversampling nor trigger options, and there is no (practical) method to keep a sustained deterministic sample time of 62.5 µs.
- PN RT solutions do not allow oversampling, so basically stop at 500 µs (lowest update cycle).
- A S7-1512SP with HS (High-Speed) analog I/O modules on its own backplane – so a solution with remote I/O and its own local processor – does not allow for oversampling.

A Siemens ET200SP IO Device with an IM155-6 PN HF (High Feature) PN bus coupler supports oversampling when used with PROFINET IRT (Isochronous Real Time PN) and a Main CPU (Fig. 1). Combined with HS I/O modules, up to 16 (over)samples per input are possible per update cycle, with a minimum of 50 µs. The oversamples are sent one after another in the next PN IRT message (see later).

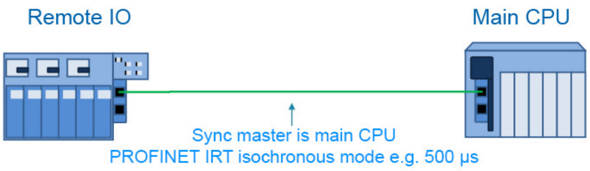


Figure 1. Basic architecture with oversampling in remote I/O, data stream directly to the "main CPU".

However, this set-up has several drawbacks:

- it does not guarantee timely processing of the continuous stream of measurement data (at 20 kHz for each individual analog input) as this depends on the cycle time of the PLC
- it puts a heavy burden on the PLC that needs to process the complete program which has an overall cycle time of more than 2 up to 3 ms, not yet including the acquisition and processing of the analog measurements.

Timely processing is solved by isochronous processing of the received IRT message in OB6x [2] (Fig. 2). In isochronous processing mode, the Send Clock (PROFINET) and the Cycle Clock (PLC) are synchronized by interrupts. Upon receiving an IRT message (e.g. every 250 µs), OB6x is called and the Process Image Partition (PIP) is updated, calculations are made and finally outputs are written to the PIP, ready to be sent in the next IRT message (in the next PN cycle).

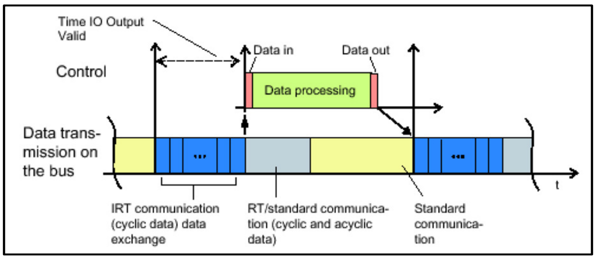

Time IO Output Valid
Control
Data in
Data out
Data processing
Data trans-mission on the bus
...
...
t
IRT communication (cyclic data) data exchange
RT/standard communica-tion (cyclic and acyclic data)
Standard communica-tion

Figure 2. Isochronous processing in OB6x

2.2. Overall architecture

Typical timing for the configuration of Fig. 1 – using one "main CPU" – leads e.g. for a S7-1516-3 CPU with PN IRT at 250 µs (with 5 oversamples to reach 50 µs) to 110 µs base CPU load every 250 µs, even without processing the data itself. Referring to Table 1 [3]: 80 µs (cyclic interrupt) + 30 µs (base load for PIP update) = 110 µs.

As this would leave not much time left for normal processing, a (very) expensive 1518 CPU is likely to be needed. This leads to the architecture with a low-cost "streaming CPU" and a "normal" main CPU (Fig. 3).

A low-cost S7-1512SP is used as sync master in a PN IRT network at 500 µs, and acts as "streaming CPU". It handles the continuous data stream of 20 kHz per analog channel, reads the encoder and calculates the sample hits: every encoder reading is minimum 250 µs with no oversampling possible, so interpolation is needed for the 50 µs resolution sample hit of the encoder position. On its 2nd PN port, the S7-1512SP acts as I-Device ("Intelligent CPU as IO-Device") in a PN RT network (Fig. 3).

Table 1. Typical timing for some CPUs.

	S7-1512SP	S7-1511-1	S71516-3	S7-1518-4
Base load for PIP update (µs)	-	35	30	5
Copy time for distributed I/O modules via PROFINET (µs)	-	0,5	0,5	0,3
Bit operations, typ. (ns)	48	60	10	1
Word operations, typ. (ns)	58	72	12	2
Cyclic Interrupt (µs)	-	90	80	12

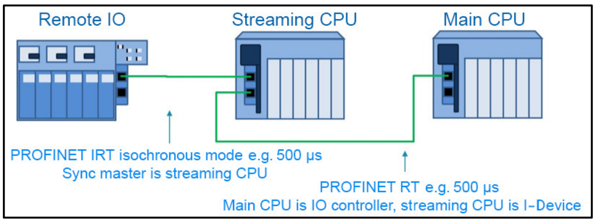

Remote IO
Streaming CPU
Main CPU
PROFINET IRT isochronous mode e.g. 500 µs
Sync master is streaming CPU
PROFINET RT e.g. 500 µs
Main CPU is IO controller, streaming CPU is I-Device

Figure 3. Suggested networked sensing architecture: low-cost "streaming CPU" reducing the workload of the main CPU.

3. Experimental analysis and signal reconstruction

The DPO 2024 oscilloscope is used to measure the 2 trapezium functions, the sine function and the pulse that simulates the encoder position hit signal (Fig. 5). These signals are generated using MATLAB generated code running on a xPC target PC using a Humusoft I/O card (Fig. 4, 5 top).

The DPO4054B measures the 2 trapezium functions and the 2 PROFINET data signals: from ET200SP to S7-1512SP and S7-1512SP to S7-1516, each time the transmitting wire set (Fig. 4 and 6).

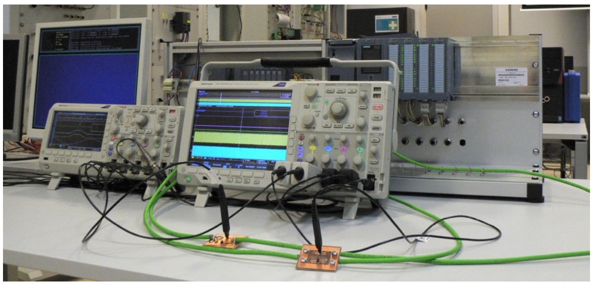


Figure 4. From left to right: xPC target screen, TEK DPO 2024 (4 analog signals), TEK DPO 4054B (2 analog and 2 Ethernet signals), (behind 4054B) S7-1512SP streaming CPU, ET200SP HF, S7-1516.

All the signals are saved into a csv file. The PROFINET messages are also saved in a csv table allowing further processing in MATLAB. Fig. 5 (bottom) shows the signal reconstruction – taking into account the signal propagation through the networks and components –tested in MATLAB: the test signals are sampled on each encoder hit (upper signal and marked in red) and plot on the original measurements.

The signal reconstruction algorithm is programmed in the streaming CPU, acting as I-Device in the PN RT network (main CPU is IO Controller). The RT network and the main CPU only get a small network load (Fig. 6) resp. processor load: the continuous 20 kHz measurement data stream is only in PN IRT, and handling and signal reconstruction is inside the streaming CPU.

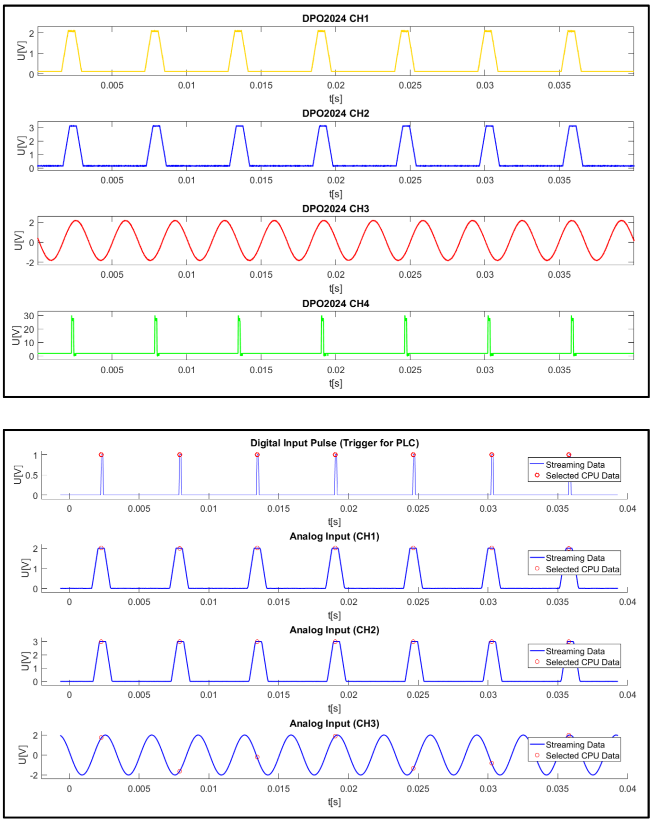
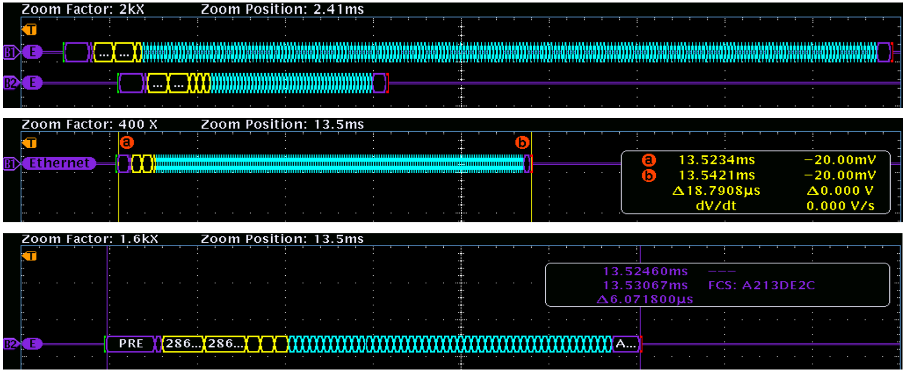


Figure 5. Top: test signals; bottom: MATLAB timing reconstruction.

4. Analysis of the signal timing and propagation

As shown earlier, signal timing reconstruction is accurate (Fig. 5). Fig. 7b shows the signal propagation in the networks and CPUs.

With a streaming CPU (Fig. 3, measurement in Fig. 7a), there is a delay of 3 update cycles before the useful data (measurements at encoder hits) is available in the main CPU: 3 x 500 µs. This is well within the above mentioned cycle time of more than 2 up to 3 ms. Data could be processed in the 4th cycle (OB1) or, if PROFINET IRT instead of RT would be used, in the 3rd cycle using OB6x.



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Zoom Factor: 2kX        Zoom Position: 2.41ms

Zoom Factor: 400 X      Zoom Position: 13.5ms
a  13.5234ms    -20.00mV
b  13.5421ms    -20.00mV
△18.7908µs      △0.000 V
dV/dt           0.000 V/s

Zoom Factor: 1.6kX      Zoom Position: 13.5ms
13.52460ms   ---
13.53067ms   FCS: A213DE2C
△6.071800µs
```

PROFINET IRT	
update cycle (µs)	500
# data bytes in test set-up	209
Bus in Fig. 6	B1
message length (µs)	18,79
% of update cycle	3,76
PROFINET RT	
update cycle (µs)	500
# data bytes in test set-up (1)	40
Bus in Fig. 6	B2
message length (µs)	6,07
% of update cycle	1,21
(1) 40 is minimum for ethernet/PROFINET	

Figure 6. Top: IRT message containing raw oversampled data, and the short RT message containing only the useful measurement data on the sample hits. Middle: measurement of IRT message length. Bottom: measurement of RT message length. Right: analysis of IRT and RT messages and timing.

Without streaming CPU (set-up of Fig. 1), data is delayed 2 update cycles, and can be immediately processed in OB6x of the (more expensive) main CPU.

5. Conclusions

A low-cost solution with fairly standard yet high-end industrial components is developed allowing the reuse of existing validated program code. The networked sensing architecture includes techniques of oversampling and isochronous processing of IRT messages.

MATLAB code has been developed to initially test the signal reconstruction algorithm, and additional MATLAB code was developed to analyze the signal timing and propagation, combining analog and Ethernet data.

The solution for this case study is robust with little extra CPU and network load, is innovative in its design, and allows for many applications involving processing of signals sampled up to 20 kHz.

Future work includes:

- Increasing acquisition bandwidth and reducing impact of signal noise, e.g. using SiPlus CMS condition monitoring hardware.
- Testing alternative solutions involving triggered measuring and time stamping using other network solutions (e.g. EtherCAT).
- Developing signal processing and control algorithms in MATLAB, to be run on the streaming CPU using code generation, allowing fast high-end applications on low cost hardware.

6. Acknowledgment

Eric De Ron of Siemens Belgium for detailed technical information. Stijn Noppe – currently at Phoenix Contact Belgium – for his contribution to this research during his working period at KU Leuven. This work was partially funded by the Interreg Va 2 Seas project 2S01-049 INCASE.

References

[1] Manfred Popp, Karl Weber, “The Rapid Way to PROFINET”, PROFIBUS Nutzorganisation, 2004, Karlsruhe, Germany.

[2] Isochronous mode with PROFINET https://support.industry.siemens.com/cs/ww/de/view/109480489

[3] Siemens AG, “S7-1500 cycle and reaction times – Function manual”, A5E03461504-02, February 2014, Nürnberg, Germany.

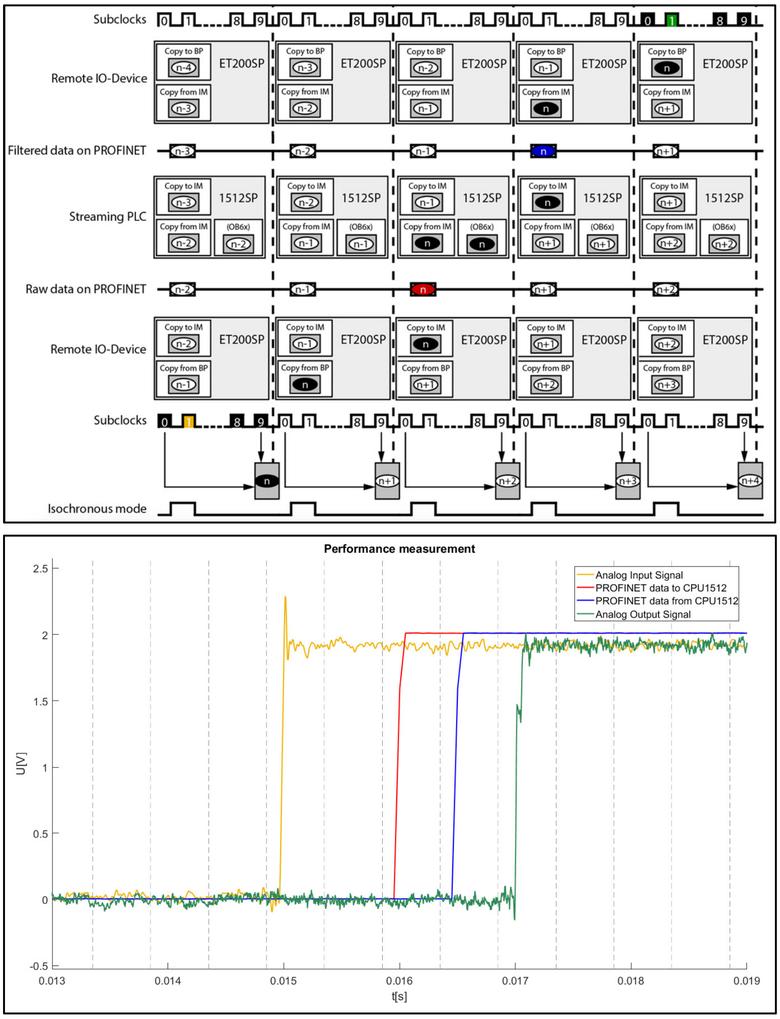

Figure 7. 7a, top: signal propagation in PROFINET and CPUs. 7b, bottom: signal propagation of analog input (yellow), reconstructed data from PROFINET messages (red is PROFINET data to S7-1512, blue is PROFINET data from S7-1512), and analog output (green).