2051.

# Scaling up Silicon Photonic Circuits: Where are the Challenges?

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***Abstract*—Silicon photonics fabrication technology allows large scaling of photonic circuits. But the scaling is limited by the design process for large interconnected circuits, and the operation of circuits with inherently imperfect and nonuniform building blocks.**

***Keywords—silicon photonics, large-scale integration, design, photonic-electronic integration***

## I. Introduction

In the past decade, silicon photonics has rapidly grown into an accepted technology: there are multiple commercial fabs and publicly accessible research foundries, the first silicon photonics products have entered the market, and silicon photonics is generally considered as the technology that will enable scaling of photonic circuits for higher-bandwidth interconnects as well as a variety of applications in sensing, spectroscopy, medical diagnostics and optical information processing. The material system and the fabrication process can enable that scaling, up to 10000-10000 optical elements on a single chip [1].

## II. Interconnectivity

However, when we look at silicon photonic circuits today, we see that the individual building blocks usually have a high performance, but the circuits are generally very simple: 'large scale integration' goes not much further than repeating an identical circuit many times over the chip. The chips can have a very high raw performance, but the functionality is generally quite limited. If we make the comparison with electronics, the functionality of the circuit has less to do with the performance of the individual transistors than with the interconnectedness of the many electronic gates. The level of interconnection in electronics is much higher than in today's electronics. True large-scale photonic integration will require this interconnectivity to fully realize the potential of silicon photonics.

Denser connectivity will also address a latent risk of today's silicon photonic circuits: reliability. As circuit complexity increases, the risk of a catastrophic failure of a single element goes up. Higher connectivity, together with configurability, can be used to implement redundancy and fault tolerant photonic circuits.

## III. Design and Control

The fabrication technology to implement such larger circuits is here. While the adapted CMOS processes are still being improved continuously, it is not limiting the integration of these many components. The challenges lie in the design and the operation of such large circuits [2]. To integrate 10000s interconnected photonic elements in a circuit, fast circuit simulators with accurate circuit models are needed. These models need to capture sufficient richness of the optical behavior: in particular the effects of small parasitic reflections can propagate throughout a circuit and become increasingly problematic in larger circuits. It is an illusion that these will be completely eliminated in fabrication, so they should be anticipated during the design phase. Similarly, the fabrication technology will never be able to guarantee uniformity at a sub-nm level between subcircuits, dies, wafers and batches. The design tools need to capture those effects and estimate circuit yield. Design techniques to mitigate the effect of variability (e.g. linewidth-tolerant designs) can help there as well.

A silicon photonic circuit should not be regarded as a standalone chip. In practice, the optical circuit will be complemented by analog electronic drivers, digital control loops and software. These elements can no longer be considered fully decoupled: the operation of a silicon chip, with its control logic, should be incorporated into the design process. This requires design automation tools that span the gap between photonics and electronics design, going to reusable 'photonic' library elements or IP blocks that comprise a complete photonic, analog, digital and software stack.

## IV. Conclusion

The scaling up of silicon photonics will rely on the ever-improving fabrication technology, but the key to scaling will be to unlock the interconnectivity. And the challenges there are situated more in the realm of design automation and control logic.

## References

[1] J. Sun, E. Timurdogan, A. Yaacobi, E.S. Hosseini, M.R. Watts. "Large-scale nanophotonic phased array." Nature 493, 7431 (2013): 195-199.

[2] W. Bogaerts, M. Fiers, P. Dumon, Design Challenges in Silicon Photonics, J. Sel. Top. Quantum Electron., 20(4) (2014), p.1-8

# W06 The 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)

W06

The 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)

**Session Type:** Workshop

**Date:** Friday, March 31, 2017

**Time:** 0830-17:30

**Location / Room:** 4A

**URL:** Homepage [1]

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Sébastien Le Beux, Lyon Institute of Nanotechnology, FR (Contact Sébastien Le Beux [4])

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Mahdi Nikdast, Polytechnique Montréal/McGill University, CA (Contact Mahdi Nikdast [5])

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Download handouts here (Handouts are available for attendees only! The password has been sent to you by email or you may ask for the password at the onsite registration desk) [21]

## Scope of the Workshop

Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering an alternative interconnect technology to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to address the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices and circuits are necessary to construct photonic interconnection networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects. OPTICS aims at discussing the most recent advances in photonic interconnect and silicon photonics for computing systems. Industry's and academia's views on the feasibility and recent progress of optical interconnect and silicon photonics will be discussed. The workshop is comprised of invited talks of the highest caliber in addition to refereed poster presentations.

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**DATE 2017 in Lausanne received over 1,500 registrations from international experts, who celebrated the 20th edition of the conference and exhibition**

2017-04-04

The DATE 2017 Conference and Exhibition closed doors last Friday, March 31, 2017, receiving more than 1,500 registrations from over 50 countries and ending with excellent feedback from both participants and exhibitors.

2017 was a special year for the world's favourite electronic systems design and test conference, as the community celebrated its 20th edition and it was held for the first time in Switzerland, at the SwissTech Convention Center on the EPFL campus in Lausanne, from March 27 to 31, 2017.

DATE 2017 received 794 paper submissions, a large share (42%) coming from authors in Europe, 32% from America, 25% from Asia, and 1% from the rest of the world. **This clearly demonstrates DATE's international character, its global reach and impact.**

For the 20th successive year, DATE presented an exciting technical programme, comprising 78 technical sessions and 11 Exhibition Theatre sessions. The DATE week started on Monday with nine in-depth tutorials and the popular PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA.

On Tuesday, the conference was opened by the **plenary keynote speakers** Dr. Arvind Krishna from IBM presenting "Design Automation in the Era of AI and IoT: Challenges and Pitfalls" and Dr. Doug Burger from Microsoft who talked about "A New Era of Hardware Microservices in the Cloud". In addition, a keynote lecture from Prof. Giovanni De Micheli (Professor at EPFL and Director of Nano-Tera.ch) was given on "Distributed Systems for Health and Environmental Monitoring" within the Nano-Tera.ch initiative. On the same day, an **Executive Panel Session** and three **Innovative Technologies & Applications (IT&A)**

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12:00 W06.5 **Lunch Break and Poster Session**

13:00 W06.6 **Afternoon Session I: Opportunities and Challenges!**

**Chair:**
Jiang Xu, Hong Kong University of Science and Technology, CN, Contact Jiang Xu [3]

13:00 W06.6.1 **Scaling Up Silicon Photonic Circuits: Where Are the Challenges?**
Wim Bogaerts, Ghent University-IMEC, BE

13:30 W06.6.2 **Impact of Planar Photonic Switch Architecture on Worse-Case Power Penalty**
Sebastien Rumley, University of Columbia, US

13:50 W06.6.3 **Towards Accurate Silicon Photonics Platform Qualification for Static and Dynamic Purposes**
Jean-Francois Carpentier, STMicroelectronics, FR

14:10 W06.6.4 **Temperature Sensitivity Analysis and Power Consumption Optimization of Optical Networks-on-Chip**
Yaoyao Ye, Shanghai Jiao Tong University, CN

14:30 W06.7 **Coffee Break and Poster Session**

15:00 W06.8 **Afternoon Session II: Design Automation and Methodologies!**

**Chair:**
Sébastien Le Beux, Lyon Institute of Nanotechnology, FR, Contact Sébastien Le Beux [4]

15:00 W06.8.1 **Towards Electronic-Photonic Design Automation for Optical Interconnect Networks**
Nikolay Karelin, VPIphotonics, BY

15:20 W06.8.2 **Challenges for mask layout for silicon photonic devices and circuits**
Marcel van der Vliet, PhoeniX, NL

15:40 W06.8.3 **From Circuit-Level to Component-Level Simulation and Back - PDK Driven Design Automation**
Jonas Flueckiger, Lumerical, CA

16:00 W06.8.4 **Design Automation Beyond its Electronic Roots: Toward a Synthesis Methodology for Wavelength-Routed Optical Networks-on-Chip**
Davide Bertozzi, University of Ferrara, IT

16:20 W06.8.5 **Silicon Photonics Scalable Design Framework: From Design Concept to Physical Verification**
Sarhan Hossam, Mentor, FR

16:40 W06.9 **Panel Discussion**

**Moderator:**
Jiang Xu, Hong Kong University of Science and Technology, CN, Contact Jiang Xu [3]

**Panelists:**
Wim Bogaerts, Ghent University-IMEC, BE, Contact Wim Bogaerts [22]
Jean-Francois Carpentier, STMicroelectronics, FR, Contact Jean-Francois Carpentier [23]
Bert Jan Offrein, IBM Zurich Research Lab., CH, Contact [24]
Nikolay Karelin, VPIphotonics, BY, Contact Nikolay Karelin [25]
Marcel van der Vliet, PhoeniX, NL, Contact Marcel van der Vliet [26]
Laurent Vivien, CNRS, FR, Contact Laurent Vivien [27]

17:20 W06.10 **Concluding Remarks and Closing Session**

**Chair:**