DEEP LEVEL INVESTIGATION OF INGAAS ON INP LAYER

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ABSTRACT

Deep level traps in lattice-matched $In_{0.47}Ga_{0.53}As$ epitaxial layers grown by MBE on InP substrates have been studied by Deep Level Transient Spectroscopy (DLTS) on Al_2O_3/InGaAs Metal-Oxide-Semiconductor (MOS) capacitors. The impact of different surface passivation steps and a post-gate-deposition Forming Gas Annealing (FGA) has been studied. It is shown that spectra are dominated by a near mid gap electron trap in the depletion region, with activation energy in the range 0.37 eV to 0.42 eV. At the same time, a broad background distribution of interface states is found as well, which is significantly reduced by the FGA. Detailed carrier trapping studies have been carried out to identify the origin of the grown-in electron traps, which are shown to be of point defect behavior.

Keywords—high-mobility channels; DLTS; deep level traps; interface states; bulk defects.

INTRODUCTION

For future high-speed low-power logic applications, III–V CMOS is of interest for its superior electron mobility [1, 2]. However, exposure of the III–V surface to air or low vacuum results in the rapid formation of low quality native oxide on the surface, leading to the near midgap Fermi-level pinning and a high D_{it} density of states present at the high-κ/III-V interface [1-7]. The origin of these interface states has been heavily debated on in the past [7] but there are clear indications that a strong relationship exists with native antisite point defects (As_{Ga} or Ga_{As}) [6], as also evidenced by scanning tunneling microscopy [8, 9]. The density D_{it} can be strongly affected by the surface treatment (cleaning, passivation), so that this will determine the degree of Fermi level pinning and dictates whether it will be possible to invert the interface or not.

Effective surface passivation is thus of great importance to obtain a high quality interface. At the same time, as epitaxial deposition is a highly non-equilibrium growth method, the presence of grown-in point and/or extended defects in the InGaAs layer is expected.

Therefore, the purpose of this work is to study the impact of different surface treatments and post-deposition FGA on the deep levels states in $Al_2O_3/In_{0.53}Ga_{0.47}As$/InPMOS capacitors by using Deep Level Transient Spectroscopy [10] which is a more complete interface-state characterization method than the traditional Capacitance-Voltage C-V and Conductance-Voltage G-V versus frequency and temperature techniques [11-13]. During DLTS Temperature-Scan, different bias pulses will be used to separate electron traps in the depletion region of the n-type InGaAs layer and at the Al_2O_3/InGaAs interface.

EXPERIMENTAL DETAILS

The 300 nm thick n-type $In_{0.47}Ga_{0.53}As$ layers have been grown by Molecular Beam Epitaxy (MBE) lattice matched on n-type InP substrates. Ammonia Sulfide ($(NH_4)_2S$) indicated by AS and HCl surface treatment before 10 nm Al_2O_3 gate oxide by Atomic Layer Deposition (ALD) have been applied, respectively. Post-deposition Forming Gas ($10\%H_2+90\%N_2$) annealing at 370°C for 15 min is also investigated. 50nm Pt is used as top metal contact and the back ohmic contact is formed by a Mo metallization stack. More detailed information of the studied samples is summarized in Table I.Top metal pads with area about 0.385mm^2 have been measured by a digital Fast Fourier Transform DLTS system, including a Boonton capacitance bridge operating at a fixed frequency of 1MHz. The gate bias is applied to the gate contact, while the substrate is kept grounded. First, I-V and C-V are measured to define an approximate bias condition for DLTS. Take C-V of AF as an example in Fig. 1. In order to distinguish the different types of defects in the InGaAs layer or at the Al_2O_3/InGaAs interface a reverse bias in depletion and a pulse bias either in depletion (-1 V-->-0.5 V) or in accumulation (-1 V-->0 V) have been applied. The doping density has been derived from the C–V characteristics in depletion. The depletion width in Table I corresponds with V_R=-1 V.

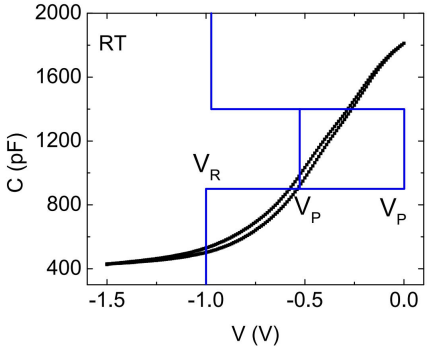

Figure 1: Capacitance-Voltage of the AF capacitor

Temperature-Scan DLTS at a fixed sampling frequency of 1 MHz has been executed to study the deep levels in the MOS system, whereby a voltage pulse from deep depletion to accumulation (V_R-V_P) was applied for a filling time t_p 1ms and with a sampling period t_w of 51.2ms. Pulse Duration Scans are also executed to examine the trap filling kinetics. This reveals information on the point- or extended-defect nature of the observed deep levels. The Arrhenius plots are obtained by using different Fourier coefficients of the numerically filtered transient signal and are used to calculate the activation energy and electron capture cross section.

TABLE I
EXPERIMENTAL DETAILS

Name	*AS treated*	*HCl treated*	*FGA*	*Ndop/cm^{-3}*	*W_R/nm*
AA	✓			7.41E15	93
AF	✓		✓	1.61E16	116
HA		✓		8.66E15	104
HF		✓	✓	7.46E15	140

*W_R is the depletion width at reverse bias -1V

RESULTS AND DISCUSSION

Figure 2 shows typical DLTS spectra in function of the sample temperature for an n-type InGaAs MOS capacitor, corresponding with different gate voltage pulses from depletion at -1V to accumulation -0.5V and 0V, respectively. It is obvious that the DLTS signal yields a broad peak between 200K-250K, which is associated with grown-in electron traps in the InGaAs epi layer. Changing the pulse bias from -0.5V to 0V, allows to fill more traps at the InGaAs/Al_2O_3 interface with electrons. However, it is observed in Fig. 2 that the DLTS signal intensity only increases and no other new defect signal from interface states appeared.

Comparing Figs 2 and 3 for the HCl-treated samples, one can clearly discern that FGA results in the removal of the broad wing features at higher and lower temperatures, which are thought to be related to the density of interface states (D_{it}), while the central peak at about 200K remains relatively unaffected. As it appears for a bias pulse in depletion, this central peak is associated with defects in the n-type InGaAs depletion region. It is concluded that an effective passivation of the interface states by FGA occurs for both pre-deposition treatments.

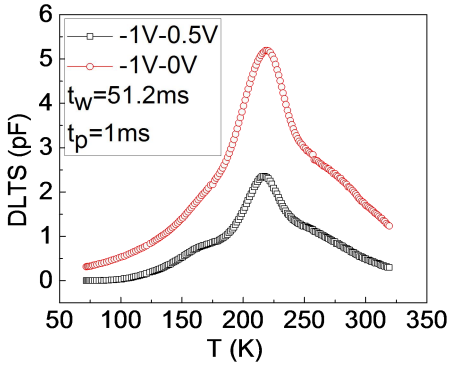

Figure 2: DLTS spectra of a HA;t_w=51.2 ms, t_P=1ms. A bias pulse from -1 V to -0.5 V (depletion) and 0 V (accumulation) has been applied to the gate of the MOS capacitor

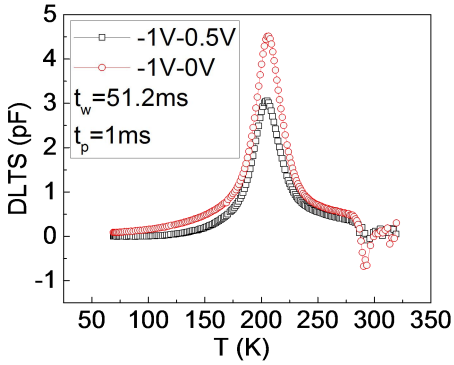

Figure 3: DLTS spectra of a HF capacitor; t_w=51.2 ms, t_P=1 ms. A bias pulse from -1 V to -0.5 V (depletion) and 0 V (accumulation) has been applied to the gate of the MOS capacitor

For the different surface pre-gate treatments Ammonia Sulfide AS and HCl, the DLTS peak is constant, as shown in Fig. 4 (FGA). Interestingly, the FGA appears to affect the bulk traps as well, showing a clear shift of the peak to a lower temperature in Fig. 5. A lower amplitude is also found, although this is mainly related with the removal (passivation) of the interface states.

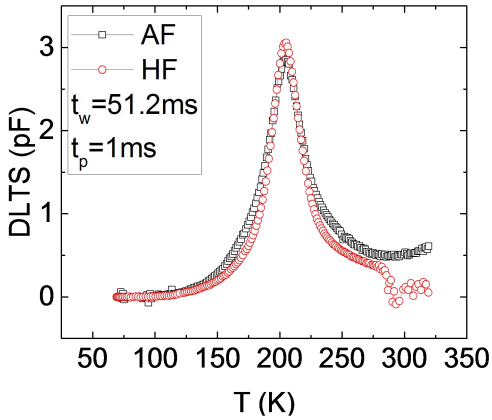

Figure 4: DLTS spectra of an AF and HF capacitor at a pulse from -1 V to -0.5 V, after FGA

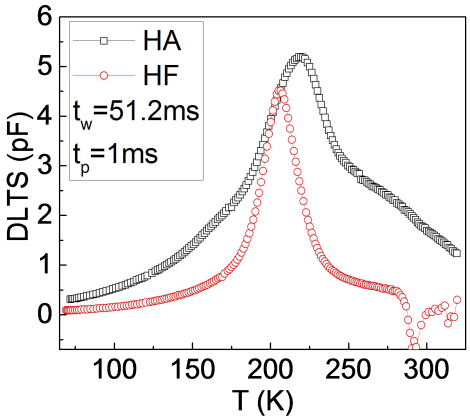

Figure 5: DLTS spectra of a HA and HF capacitor at a pulse from -1 V to 0 V

A different activation energy and electron capture cross

section are derived from the Arrhenius plot in Fig. 6. This indicates a possible reaction of the defects in the InGaAs layer with hydrogen, giving rise to a change in the parameters. A pulse duration scan is measured for AF, as shown in Fig. 7. A mostly point defect behavior is observed for the electron traps in both the InGaAs depletion region and at the Al_2O_3/InGaAs interface. The slow increase of the amplitude at longer t_p filling time could be related to long capture time constant caused by capture in the carrier tails at the end of the depletion region [14].

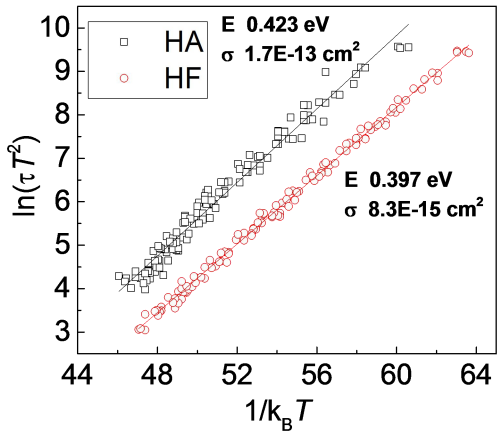

Figure 6: Arrhenius plots of the HA and HF samples

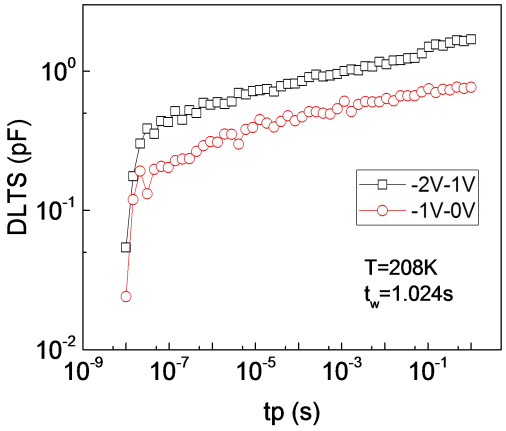

Figure 7: Pulse Duration Scan of AF at 208K;t_w=1.024s

TABLE II EXPERIMENTAL DETAILS

Name	N_{dop}/cm^{-3}	*E/eV*	σ/cm^2	N_T/cm^{-3}
AA	7.4E16	0.372±0.006	5.7E-13	7.41E15
AF	3.8E17	0.376±0.005	3.3E-15	1.61E16
HA	3.2E17	0.423±0.006	1.7E-13	8.66E15
HF	1.6E17	0.397±0.002	8.3E-15	7.46E15

CONCLUSION

It has been shown that the DLTS spectra of capacitors fabricated on lattice-matched n-type InGaAs epi layers on InP substrates exhibit a broad background distribution of interface states, which is significantly reduced by the FGA. The spectra are dominated by a near mid gap electron trap in the depletion region, with activation energy in the range 0.37 eV to 0.42 eV. The variation in activation energy can be related to the effect of the electric field on the electron emission, it is also possible that different point defect complexes are present in the InGaAs material. From the trap filling kinetics, it has been shown that this trap behaves as a point defect and should be grown-in point defects possibly related to As antisites [15].

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