A Circuit Modeling Technique for the ISO 7637-3 Capacitive Coupling Clamp Test

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***Abstract*—In this paper, we propose a transmission-line modeling technique for the ISO 7637-3 capacitive coupling clamp (CCC) test. Besides modeling the test bench, special attention is devoted to the CCC itself, for which an equivalent circuit is constructed based on the concept of surface transfer impedance and surface transfer admittance. The overall model is validated by means of measurements using a nonlinear circuit as device-under-test, as such demonstrating the appositeness to mimick the CCC test in simulations during the design phase.**

***Index Terms*—Capacitive coupling clamp (CCC), electrical fast transient (EFT) pulse, IEC 61000-4-4, ISO 7637-3, nonlinear, tansient immunity.**

I. Introduction

ELECTRICAL fast transient (EFT) disturbances represent one of the most serious threats to the operation of electronic systems. The electromagnetic (EM) energy resulting from an EFT event easily couples to cables connected to electronic equipment. Consequently, voltage pulses appear at the electronic system's ports, adversely affecting signal integrity and causing operation upsets. These effects are expected to become worse due to the continuous miniaturization trend in integrated circuits (IC) manufacturing and the resulting reduction of power supply voltages that are making electronic systems even more vulnerable.

Recognizing the importance of EFTs for designers, whose aim is to achieve electromagnetic compatibility (EMC) of equipment, international standards—such as the International Electrotechnical Commission (IEC) 61000-4-4—have been developed to provide test methods for the characterization of electronic system immunity to fast transient disturbances [1]–[3]. Such immunity tests are usually performed when the first prototype is ready or even just before production and, in case of failures, equipment reworking and redesign results in additional costs and delays. The electromagnetic compatibility (EMC) test discussed in this paper is the ISO 7637-3 capacitive coupling clamp (CCC) method [4]. The CCC test is a broadband EMC test suitable for coupling fast transient pulses, which typically occur as a result of switching processes. A first method to model the ISO 7637-3 CCC is given in [5] and [6], where its properties are measured and characterized by making use of a vector network analyzer. Another technique to model the injection clamp is via a full-wave approach [7] to allow reproducing the response of the device in the time domain. As full-wave simulators typically consume a lot of CPU time, an alternative way is to construct circuit models that mimic the behavior of the injection clamp [8]–[10]. However, these models were solely based on calculating mutual inductances and capacitances and do not fully encompass all transmission-line (TL) effects.

In this paper, we propose an efficient technique, using the TL theory and the concept of surface transfer impedance and surface transfer admittance, to model the CCC as well as the CCC test bench. The proposed circuit equivalent of the CCC test setup is validated by means of measurements, leveraging a nonlinear circuit as device-under-test (DUT). As such, the appositeness to mimick the CCC test in simulations during the design phase of susceptible equipment is demonstrated.

The remainder of this paper is organized as follows. In Section II, a thorough description of the CCC test is given. The modeling technique for the CCC is explained in Section III. The model of the CCC test bench is explained in Section IV. Section V deals with the validation of the developed circuit model, via comparison with measurements using a nonlinear active DUT. Finally, some concluding remarks are formulated in Section VI.

II. Description of the ISO 7637-3 CCC Test

The ISO 7637-3 CCC test uses an injection clamp (see Fig. 1), which is a mechanical test fixture consisting of two metallic plates connected to each other, placed above a ground plane. As is depicted in Fig. 2, the wires under test are located inside the coupling clamp, i.e., between the two plates, while the other wires of the wire harness are placed at least 100 mm away from the coupling test fixture at a height of 50 mm above the ground plane. As in other module-level automotive EMC tests, the wire harness connects the DUT (at a height of 50 mm above the ground plane) with a load simulator (load box). The test is performed with a total harness length of 1700 mm.

An EFT generator introduces a predefined disturbance via the coupling clamp. The EFT pulse is depicted in Fig. 3 and is

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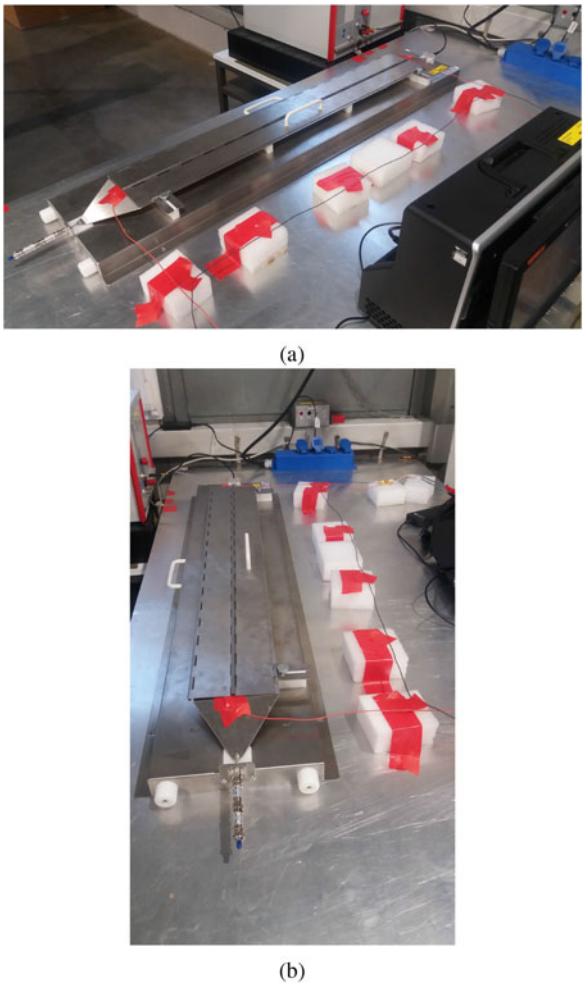

Fig. 1. ISO 7637-3 CCC test setup. (a) Top view. (b) Side view.

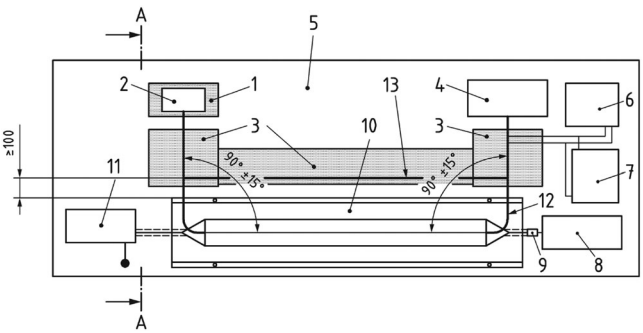

Fig. 2. Default ISO 7637-3 CCC test setup [4], where 1=insulation support, 2 = DUT, 3 = insulation support for test harness, 4 = load simulator, 5 = ground plane, 6 = power supply, 7 = battery, 8 = oscilloscope (50 Ω), 9 = 50 Ω, 10 = CCC and 11 = transient pulses generator, 12 = lines to be tested, and 13 = lines not to be tested.

described by a traditional double-exponential pulse (1), where the parameters α, β, and $U0$ determine its shape, as

$$v_s(t) = U0\left(e^{-\alpha t} - e^{-\beta t}\right). \quad (1)$$

In practice, the physical parameters such as rise time t_r, 10 % pulse width t_d and maximum amplitude U_S, indicated in Fig. 3, can be easily related to α, β, and $U0$ [11]. In [4], different

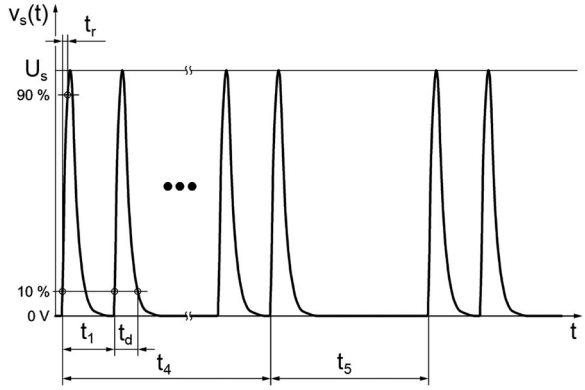

Fig. 3. Fast transient pulse 3b [4].

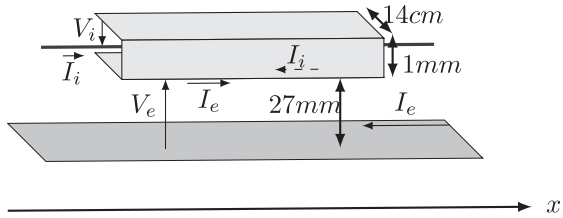

Fig. 4. Inner and external TL model of the CCC.

test levels are defined to apply in the CCC test. In this paper, we will test with the pulse 3b shown in Fig. 3 at level II. This test level corresponds to the following parameter values: U_S = 60 V, t_r = 5 ns, t_d = 0.15 μs, t_1 = 100 μs, t_4 = 10 ms, and t_5 = 90 ms. These parameters correspond to $\alpha = 5.06 \times 10^6$, $\beta = 3.806 \times 10^8$, and $U0 = 64.45$.

III. TL Model of the ISO 7637-3 CCC

In our model, we consider the injection via the coupling clamp as a shielding problem, i.e., we look at the clamp as if it is shielding the wire harness inside it. Inspired by [12], we analyze the coupling of the field that is present between the outer surface of the clamp and the ground plane to the wire harness, by describing the problem with the help of two distinct TLs, i.e., an external TL and an internal TL (see Fig. 4). Here, the external TL consists of the ground plane and the outer surface of the clamp. This *external* line has a current I_e flowing on the exterior of the clamp and the ground plane acts as return path. This external line also has a voltage difference V_e between the exterior of the clamp and the ground plane. The internal line consists of the wire harness and the interior part of the clamp. This internal line has a current I_i flowing on the wire harness, and the internal surface of the shield acts as return path. There is also a voltage difference V_i between the wire harness and the internal surface of the shield. As discussed later, the coupling between these two TLs occurs via the surface transfer impedance Z_t and the surface transfer admittance Y_t. In this paper, for notational conciseness, we consider a wire harness of two wires, where one wire runs inside the injection clamp and the other one runs next to it. The theory described in this paper can however be generalized to $N > 2$ wires.

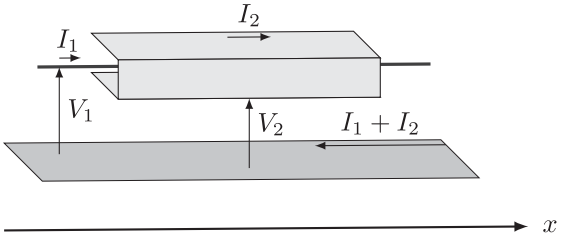

Fig. 5. MTL model of the CCC.

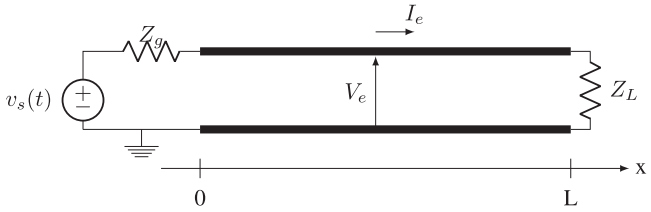

Fig. 6. Schematic of the external TL.

Although the cross section of the CCC fixture has approximately a triangular shape, in this paper, we approximate it by a rectangular cross section (see Fig. 4). As the height of the opening (1 mm) is much smaller than the width of the fixture (14 cm), this approximation will have little influence on the accuracy of the model, and it expedites the simulations.

A. Calculation of the TLs' Parameters

We start our analysis by considering the CCC as a multiconductor TL (MTL) where all voltages are defined with respect to the ground plane (see Fig. 5). This MTL is governed by the following Telegrapher's equations:

$$\frac{d}{dx}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = 0 \tag{2}$$

$$\frac{d}{dx}\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = 0. \tag{3}$$

By making use of the technique proposed in [13], we easily obtain the per-unit-length (p.u.l.) parameters, being the impedance and admittance matrices' elements Z_{ij} and Y_{ij} (i, j=1,2). Note that, given reciprocity, $Z_{12} = Z_{21}$ and $Y_{12} = Y_{21}$.

Next, we relate the MTL of Fig. 5 to the situation depicted in Fig. 4, consisting of two distinct TLs. The internal and external TL are described by the following equations [14]:

$$\frac{d}{dx}\begin{bmatrix} V_i \\ I_i \end{bmatrix} + \begin{bmatrix} 0 & Z_i \\ Y_i & 0 \end{bmatrix}\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 0 & Z_t \\ -Y_t & 0 \end{bmatrix}\begin{bmatrix} V_e \\ I_e \end{bmatrix} \tag{4}$$

$$\frac{d}{dx}\begin{bmatrix} V_e \\ I_e \end{bmatrix} + \begin{bmatrix} 0 & Z_e \\ Y_e & 0 \end{bmatrix}\begin{bmatrix} V_e \\ I_e \end{bmatrix} = \begin{bmatrix} 0 & Z_t \\ -Y_t & 0 \end{bmatrix}\begin{bmatrix} V_i \\ I_i \end{bmatrix} \tag{5}$$

and the coupling between the two is provided by the surface transfer impedance Z_t and the surface transfer admittance Y_t. As Fig. 4 on the one hand and Fig. 5 on the other hand describe the same system, the following relations are readily obtained:

$$V_1 = V_i + V_e \tag{6a}$$

$$V_2 = V_e \tag{6b}$$

$$I_1 = I_i \tag{6c}$$

$$I_2 = I_e - I_i. \tag{6d}$$

Substitution of (6) into (2) and (3) and identification with (4) and (5) yields

$$Z_t = Z_{22} - Z_{12} \tag{7a}$$

$$Y_t = Y_{11} + Y_{12} \tag{7b}$$

$$Z_i = Z_{22} + Z_{11} - 2Z_{12} \tag{7c}$$

$$Y_i = Y_{11} \tag{7d}$$

$$Z_e = Z_{22} \tag{7e}$$

$$Y_e = Y_{11} + 2Y_{21} + Y_{22}. \tag{7f}$$

Hence, by looking at the injection clamp as an MTL (see Fig. 5) and calculating its p.u.l. parameters, we can easily deduce the sought-for surface transfer impedance Z_t, the surface transfer admittance Y_t and the p.u.l. impedances Z_i and Z_e and admittances Y_i and Y_e of the internal and external TL, respectively. Note that these p.u.l. impedances and admittances can be written as $Z_i = R_i + j\omega L_i$, $Y_i = G_i + j\omega C_i$ and $Z_e = R_e + j\omega L_e$, $Y_e = G_e + j\omega C_e$, with ω the angular frequency, R_i and R_e the p.u.l. resistances, L_i and L_e the p.u.l. inductances, G_i and G_e the p.u.l. conductances and C_i and C_e the p.u.l. capacitances of the internal and external TL, respectively. For illustration, we give the p.u.l. parameters of the CCC fixture up to 100 MHz (see Table I). This frequency range is sufficient as the bandwidth of the signal is only about $\frac{1}{\pi 5ns} = 63.6$ MHz. In our model, the small dielectric losses are neglected. It is also noticed that, up to the numerical precision of the simulations, $C_{11} = -C_{12}$ and $L_{12} = L_{22}$, which is due to the fact that conductor 1 is nearly entirely enclosed by conductor 2. In what follows, we will use the "weak coupling assumption" [15], neglecting the coupling of the internal TL to the external TL. This amounts to putting Z_t and Y_t to zero in (5) while retaining the coupling terms in (4).

B. External TL

The external TL (as shown in Fig. 6) is given by the exterior of the clamp and the ground plane.

In time-harmonic regime and adopting the weak coupling assumption, we obtain the following equations:

$$\frac{dV_e(x)}{dx} = -Z_e I_e(x) \tag{8}$$

$$\frac{dI_e(x)}{dx} = -Y_e V_e(x). \tag{9}$$

TABLE I
P.U.L. PARAMETERS OF CCC FIXTURE

f [MHz]	$C_{11}\left[\frac{\text{pF}}{\text{m}}\right]$	$C_{12}\left[\frac{\text{pF}}{\text{m}}\right]$	$C_{22}\left[\frac{\text{pF}}{\text{m}}\right]$	$L_{11}\left[\frac{\text{nH}}{\text{m}}\right]$	$L_{12}\left[\frac{\text{nH}}{\text{m}}\right]$	$L_{22}\left[\frac{\text{nH}}{\text{m}}\right]$	$R_{11}\left[\frac{\text{m}\Omega}{\text{m}}\right]$	$R_{12}\left[\frac{\text{m}\Omega}{\text{m}}\right]$	$R_{22}\left[\frac{\text{m}\Omega}{\text{m}}\right]$
1	35.6	−35.6	99.3	505.2	175.1	175.1	128.1	2.9	2.9
10	35.6	−35.6	99.3	492.6	174.7	174.7	380.9	9.2	9.2
30	35.6	−35.6	99.3	490.2	174.7	174.7	651.7	15.8	15.8
60	35.6	−35.6	99.3	489.2	174.7	174.7	917.0	22.3	22.3
100	35.6	−35.6	99.3	488.6	174.6	174.6	1174.0	28.6	28.6

And hence

$$V_e(x) = Ae^{-k_e x} + Be^{k_e x} \tag{10}$$

$$I_e(x) = \frac{1}{Z_{C,e}}\left(Ae^{-k_e x} - Be^{k_e x}\right) \tag{11}$$

with

$$Z_{C,e} = \sqrt{\frac{Z_e}{Y_e}} \tag{12}$$

$$k_e = \sqrt{Z_e Y_e}. \tag{13}$$

The square roots in (12) and (13) are defined such that $\Im(k_e) > 0$ and $\Re(k_e) > 0$. The clamp, its far-end load Z_L, and the EFT source resistor Z_g are specified in the standards such that $Z_{C,e} = Z_g = Z_L = 50\ \Omega$. Hence, given this matching, $B = 0$ in (10) and (11) and $A = \frac{v_s(s)}{2}$, with $s = j\omega$, i.e., the frequency-domain equivalent of $v_s(t)$ (1).

C. Internal TL

To solve the internal TL, we use the *chain parameter matrix* (CPM) formulation [15]. This leads to the following equations:

$$\begin{bmatrix} V_i(L) \\ I_i(L) \end{bmatrix} = \mathbf{\Phi}(L)\begin{bmatrix} V_i(0) \\ I_i(0) \end{bmatrix} + \begin{bmatrix} V_{FT} \\ I_{FT} \end{bmatrix} \tag{14}$$

where $\mathbf{\Phi}(L)$ is the 2×2 chain parameter matrix (since we assume that only one wire runs into the injection clamp).

$$\mathbf{\Phi}(L) = \begin{bmatrix} \frac{1}{2}\left(e^{k_i L} + e^{-k_i L}\right) & -Z_{C,i}\frac{1}{2}\left(e^{k_i L} - e^{-k_i L}\right) \\ \frac{-1}{Z_{C,i}}\frac{1}{2}\left(e^{k_i L} - e^{-k_i L}\right) & \frac{1}{2}\left(e^{k_i L} + e^{-k_i L}\right) \end{bmatrix}. \tag{15}$$

Here, $k_i = \sqrt{Z_i Y_i}$ and $Z_{C,i} = \sqrt{\frac{Z_i}{Y_i}}$. V_{FT} and I_{FT} are the equivalent source terms at the end of the TL, given by

$$\begin{bmatrix} V_{FT} \\ I_{FT} \end{bmatrix} = \int_0^L \mathbf{\Phi}(L-\tau)\begin{bmatrix} V_d(\tau) \\ I_d(\tau) \end{bmatrix} \mathrm{d}\tau \tag{16}$$

where V_d and I_d are distributed voltage and current sources along the line. In our case, these distributed sources appear because of the coupling of the external TL to the internal TL by means of the transfer surface impedance and transfer surface admittance, as follows:

$$V_d(\tau) = Z_t I_e(\tau) \tag{17}$$

$$I_d(\tau) = -Y_t V_e(\tau). \tag{18}$$

The source terms V_{FT} and I_{FT} are expressed as

$$V_{FT} = \int_0^L \Phi_{11}(L-\tau)\frac{Z_t}{Z_{C,e}}V_e(\tau)\,\mathrm{d}\tau - \int_0^L \Phi_{12}(L-\tau)Y_t V_e(\tau)\,\mathrm{d}\tau \tag{19}$$

$$I_{FT} = \int_0^L \Phi_{21}(L-\tau)\frac{Z_t}{Z_{C,e}}V_e(\tau)\,\mathrm{d}\tau - \int_0^L \Phi_{22}(L-\tau)Y_t V_e(\tau)\,\mathrm{d}\tau. \tag{20}$$

D. Circuit Model of the Equivalent Source Terms V_{FT} and I_{FT}

In the ISO 7637-3 [4], a *transient* signal is injected and measured at the DUT end of the CCC. In (19) and (20), we obtained an expression for the source terms V_{FT} and I_{FT} in the frequency domain. Hence, using these expressions would make it necessary to take the Fourier transformation of the injected disturbance signal, apply (19) and (20) and take the inverse Fourier transform of the result. This not only causes overhead but would also result in the occurrence of the Gibbs phenomenon due to the fast pulses. Even more importantly, this would also imply that nonlinear DUTs cannot be assessed. These issues are solved by reformulating (19) and (20) in the Laplace domain and by constructing a circuit equivalent that allows rapid transient analysis in any commercial circuit solver. Transforming (19) and (20) to the Laplace domain ($s = j\omega$), neglecting the very small losses, yields

$$V_{FT}(s) = \int_0^L \frac{1}{2}\left(e^{s\beta_i(L-\tau)} + e^{-s\beta_i(L-\tau)}\right)e^{-s\beta_e\tau}\frac{Z_t}{Z_{C,e}}\,\mathrm{d}\tau - \int_0^L -Z_{C,i}\frac{1}{2}\left(e^{s\beta_i(L-\tau)} - e^{-s\beta_i(L-\tau)}\right) Y_t e^{-s\beta_e\tau}\,\mathrm{d}\tau \tag{21}$$

$$I_{FT}(s) = \int_0^L \frac{1}{2}\left(e^{s\beta_i(L-\tau)} - e^{-s\beta_i(L-\tau)}\right)\frac{Z_t}{Z_{C,e}}e^{-s\beta_e\tau}\,\mathrm{d}\tau - \int_0^L \frac{1}{2}\left(e^{s\beta_i(L-\tau)} + e^{-s\beta_i(L-\tau)}\right)Y_t e^{-s\beta_e\tau}\,\mathrm{d}\tau. \tag{22}$$

Analytically performing the integration of (21) and (22), the following closed form is obtained for $V_{FT}(s)$ and

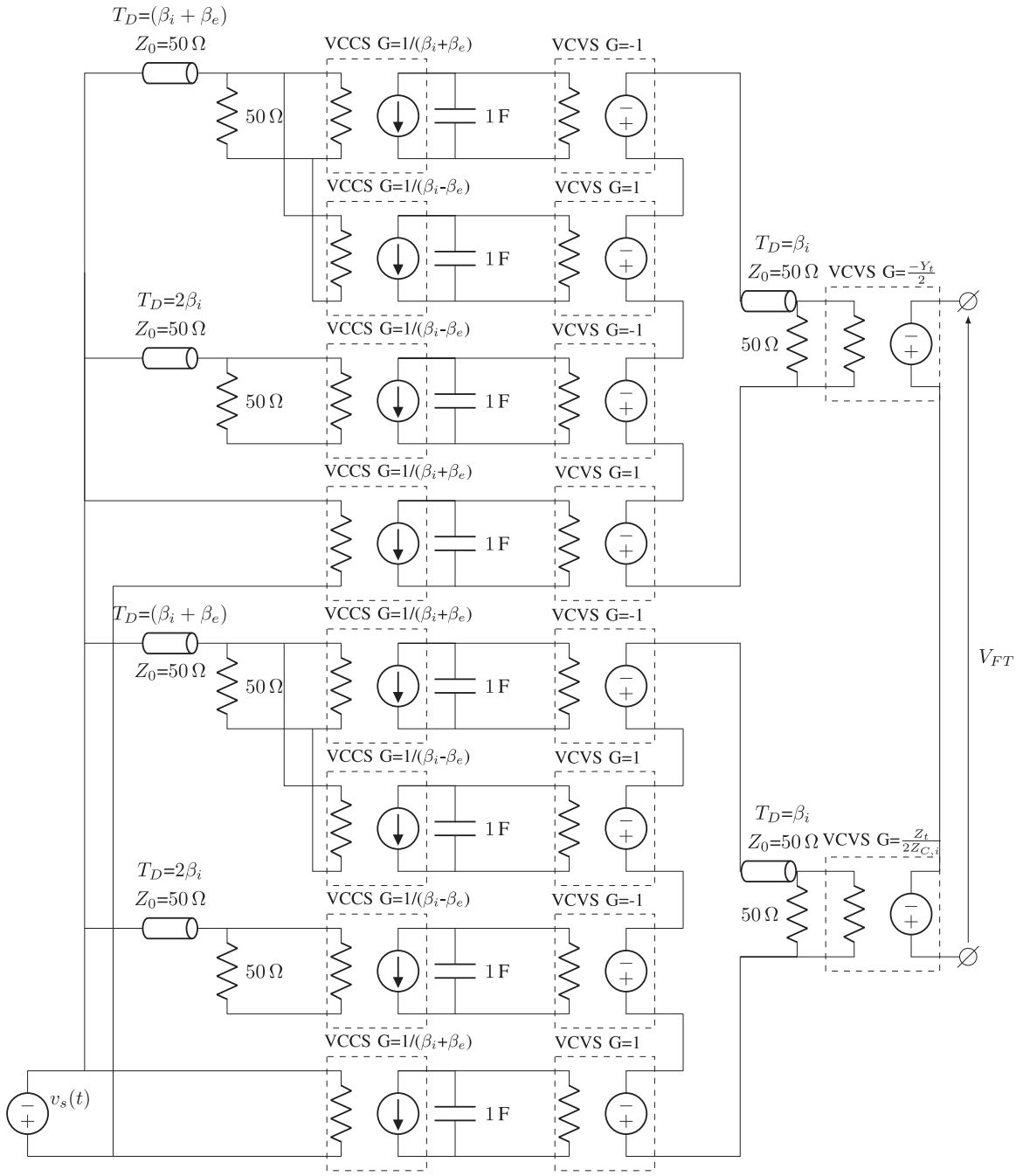

Fig. 7. Circuit model of the equivalent voltage source V_{FT} (23).

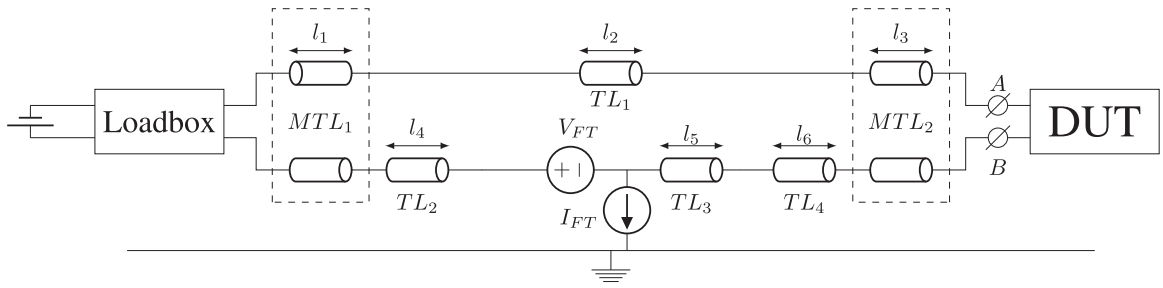

Fig. 8. TL modeling of the ISO 7637-3 CCC test bench (see Table II).

TABLE II
DIMENSIONS OF THE TL MODEL OF THE ISO 7637-3 CCC TEST BENCH

Dimension	Value	Dimension	Value
l_1	0.4 m	l_3	0.4 m
l_2	1.0 m	l_4	0.1 m
l_5	1.0 m	l_6	0.1 m

$I_{FT}(s)$:

$$V_{FT}(s)e^{-s\beta_i L} = \frac{-Z_{C,i}Y_t v_s(s)}{2}\left[\frac{e^{-s(\beta_i+\beta_e)L}-1}{s(\beta_i+\beta_e)L} + \frac{e^{-s(\beta_i+\beta_e)L}-e^{-2s\beta_i L}}{s(\beta_i-\beta_e)}\right] + \frac{Z_t v_s(s)}{2Z_{C,i}}\left[\frac{e^{-s(\beta_i+\beta_e)L}-1}{-s(\beta_i+\beta_e)} + \frac{e^{-s(\beta_i+\beta_e)L}-e^{-2s\beta_i L}}{s(\beta_i-\beta_e)}\right] \quad (23)$$

$$I_{FT}(s)e^{-s\beta_i L} = \frac{-v_s(s)Y_t}{2}\left[\frac{1-e^{-s(\beta_i+\beta_e)L}}{s(\beta_i+\beta_e)} + \frac{e^{-s(\beta_i+\beta_e)L}-e^{-2s\beta_i L}}{s(\beta_i-\beta_e)}\right] + \frac{Z_t v_s(s)}{2(Z_{C,i})^2}\left[\frac{e^{-s(\beta_i+\beta_e)L}-1}{s(\beta_i+\beta_e)} + \frac{e^{-s(\beta_i+\beta_e)L}-e^{-2s\beta_i L}}{s(\beta_i-\beta_e)}\right] \quad (24)$$

with $L = 1\,\text{m}$, $\beta_i = \sqrt{L_i C_i}$, and $\beta_e = \sqrt{L_e C_e}$. From (23) and (24), we construct an equivalent circuit using the following Laplace domain—time-domain correspondences, $V(s)e^{-sT} \Leftrightarrow v(t-T)$ and $\frac{V(s)}{s} \Leftrightarrow \int_0^t v(t)dt$. In (23) and (24), the right-hand side and left-hand side is multiplied by a retardation operator $e^{-s\beta_i L}$. This is needed to eliminate advancing time operators $e^{+s\beta_i L}$ that appear in the right-hand sides of (23) and (24) during the integration. This retardation operator can be implemented by a simple TL model to take the delay into account. The equivalent circuit model of (23) is depicted in Fig. 7, a similar circuit for I_{FT} can be deduced from (24). From Fig. 7, it can be seen that the delay factors are modeled by a TL terminated by its characteristic impedance while the scaling factors are included in the voltage-controlled current sources. The integration factor $1/s$ is modeled by taking a current source loaded with a capacitor of 1 F. The integrated voltage is then measured across this capacitor. This is done for every term in (23). Summation is obtained by placing all the voltage-controlled voltage sources in series, where an extra delay line with $T_D = \beta_i$ takes the retardation operator $e^{-s\beta_i L}$ into account.

IV. MODELING OF THE TESTBENCH

Using the circuit equivalents of (23) and (24), we can now construct an equivalent circuit model of the entire ISO 7637-3 CCC test setup (see Fig. 8). The CCC injection clamp that encompasses the victim wire is represented by TL_3 with propagation factor k_i and characteristic impedance $Z_{C,i}$ and voltage source V_{FT} and current source I_{FT}. TL_1 represents the wire that is placed (at least) 100 mm away from the coupling test fixture and at a height of 50 mm above the ground plane. TL_2 and TL_4 represent the parts of the victim wire outside the clamp and not running alongside the wire represented by TL_1. MTL_1 and MTL_2 represent the two parts of the wire harness where the wires run next to each other, connected to the load box and DUT, respectively. To model this wire harness as an MTL, we applied the same method as in [16]. The load box and the DUT are connected to the two ends of the wire harness. The load box is a passive impedance, readily characterized by means of S-parameter measurements or simulations, and it is described in the EMC test plan. At the other end of the wire harness, the DUT is connected. The two-terminal nonlinear and passive DUTs considered here, are described further in Section V.

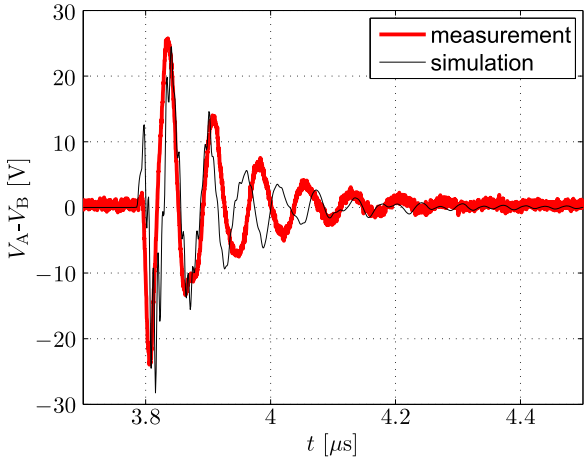

Fig. 9. Voltage across the 10-kΩ resistor DUT.

V. VALIDATION OF THE PROPOSED MODEL

To validate and illustrate the appositeness of our proposed model, we use passive and nonlinear DUTs. We measure the voltages at the DUTs and compare this with the simulation result of our model.

A. Passive DUT

As passive DUTs we use a 10-kΩ resistor and a 100-nF capacitor, representing DUTs with a high input impedance and a capacitance input stage, respectively. The purpose of these passive DUTs is to validate the proposed model of the test setup without having to deal with a potential inaccurate model of the DUT. The voltage across the resistor is depicted in Fig. 9. Fig. 10 shows the voltage across the capacitor. As can be seen, our model accurately predicts the peak amplitude of the signal waveform and its envelope. Also, there is a good correspondence concerning the ringing frequency between simulations and measurements. For example, for the 10 kΩ DUT (see Fig. 9), in measurement, we have a ringing frequency of 13.7 MHz, while in simulation 16.1 MHZ, is observed.

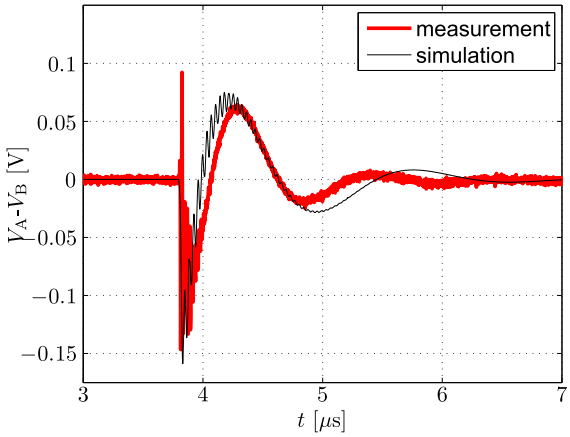

Fig. 10. Voltage across a 100-nF capacitor DUT.

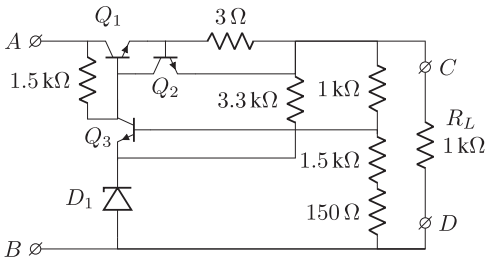

Fig. 11. Schematic of the controlled series VR.

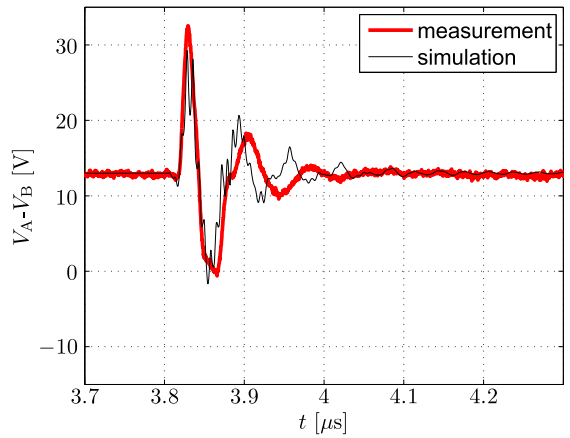

Fig. 12. Input voltage of the VR when we inject a fast transient pulse 3b level II.

B. Nonlinear DUT

As an example of a nonlinear DUT, a low drop-out voltage regulator (VR) with schematic shown in Fig. 11 is selected. This DUT was also used in [17] to validate the RI-130 test model [18]. To validate our CCC test model, we measure the voltage at the input of the VR, i.e., between nodes A and B, during the test when we inject a fast transient pulse 3b level II. The result is shown in Fig. 12. We also observe the waveform between nodes C and D, shown in Fig. 13. Similar as for the passive DUTs and owing to imperfections of the test setup, the ringing frequency is not exactly the same when comparing simulations with measurements. Additionally, we cannot expect the circuit

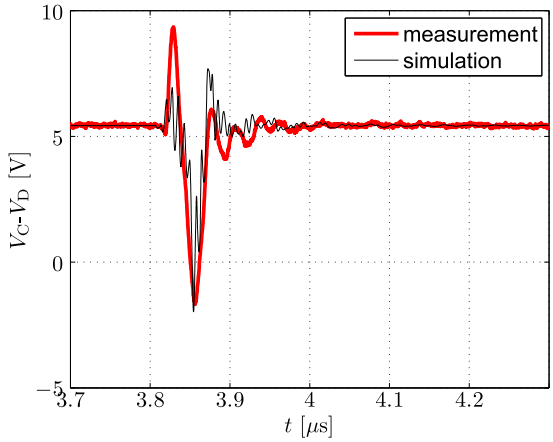

Fig. 13. Output voltage of the VR when we inject a fast transient pulse 3b level II.

model data to correspond exactly with the measurements, as the model of the DUT itself also has limited accuracy. Nonetheless, as clearly demonstrated, the proposed model predicts all salient features of the output signal and input signal of the VR, and in particular, the magnitude of the disturbance peaks and the duration of the disturbance is accurately modeled. This is of critical importance and it allows the circuit designer to analyze the immunity of his/her circuit during the design phase. It is important to mention that the CPU time to run the simulation is only 4.83 s on a workstation equipped with a i7-4770 CPU at 3.40 GHz with 32 GB RAM, which demonstrates the efficiency of the circuit modeling approach.

VI. Conclusion

In this paper, we have proposed a circuit modeling technique for the ISO 7637-3 CCC test. Special attention has been devoted to the modeling of the CCC where the concept of the surface transfer impedance and surface transfer admittance was leveraged. The overall model was validated by means of measurements using a nonlinear VR as DUT. Good accuracy and efficiency was demonstrated. Consequently, the equivalent model can be used to assess the immunity of novel circuits and devices in their design phase.

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