Transceivers for 400G based on hybrid integrated thick SOI and III/V chips

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Abstract *We present results from 400G transceiver development based on the hybrid integration of vertical-cavity surface emitting lasers and photodiode arrays on 3 and 12 µm silicon-on-insulator (SOI) chips. The integration of waveguide circuits, amplifiers and modulators on SOI is also reported.*

Introduction

New transceiver technologies are needed in both datacom and telecom applications where the relative importance of aggregate bandwidth, spectral efficiency, power efficiency, footprint and cost varies depending on the communication distance. Telecom transceivers have been traditionally based on discrete components, while short optical interconnects in data centers and high-performance computing (HPC) have been based on the combination of short-wavelength vertical-cavity surface-emitting lasers (VCSELs) and multi-mode fibers (MMFs). Communication distance with MMF is, however, limited by modal dispersion. For example, 71 Gb/s NRZ link has been demonstrated with 850 nm VCSELs, but only for a 7 m long MMF link[1]. For large data centers and access networks the communication distance should reach from 1 km up to ~40 km.

For >1 km distances standard single-mode fibers (SSMFs) are preferred. Long-wavelength VCSELs at ~1.5 µm have been used to demonstrate up to 56 Gb/s links[2-3], but there the chromatic dispersion of the SSMF and the directly-modulated laser chirp have limited the transmission distance to <1 km at 40 Gb/s.

VCSEL technology is being challenged by silicon photonic transceivers[4]. There light is generated in III-V lasers that are either edge emitting dies or heterogeneously integrated on top of silicon-on-insulator (SOI) wafers. Light modulation and detection can be achieved with monolithically integrated components that are typically realized in a 220–400 nm thick SOI layer where also wavelength (de)multiplexing and other passive functions can be integrated. This technology has already entered the datacom market. However, small waveguide dimensions induce several challenges, such as high sensitivity to fabrication tolerances, high input/output coupling losses and single-polarization operation.

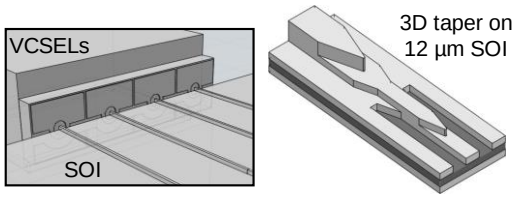

Fig. 1: VCSEL coupling to Thick-SOI waveguides (left). Spot-size conversion with tapers on 12 µm SOI (right).

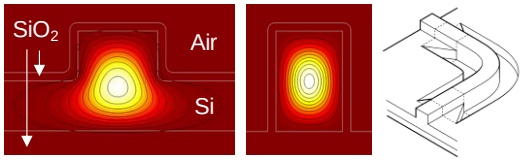

Fig. 2: Cross-sections and fundamental modes of rib and strip waveguides on 3 µm SOI (left). Rib-strip converters and Euler bends (right).

In this paper we describe our progress towards 400G transceivers for 1–40 km SSMF reach using the hybrid integration of directly modulated ~1.3 µm VCSELs, discrete photodiodes (PDs) and silicon photonics[5] (Fig. 1).

Thick-SOI silicon photonics

Using either 3 or 12 µm thick SOI avoids most of the problems that are associated with submicron SOI waveguides. In this "Thick-SOI" technology light is almost completely confined into the waveguide core (Fig. 2), so that the effective index is very close to the bulk refractive index of Si (~3.5). This makes the waveguide components and circuits insensitive to polarization, dimensional variations and surface roughness. Typical propagation loss is 0.1 dB/cm and the large cross-section area allows to transmit also high optical powers (>1 W) without nonlinear absorption. Single-mode (SM) operation over an ultra-wide wavelength range (from <1.2 to >2 µm) is achieved with rib waveguides[6] that can be adiabatically coupled to strip waveguides without the excitation of higher order modes (Fig. 2).

Thick SOI waveguides used to be associated with large footprint and large bending radii. Now they achieve integration densities that are close to submicron SOI technology. Total internal reflection (TIR) mirrors can be used in both 3 and 12 µm SOI to turn light abruptly and with <0.1 dB/90° loss. Even lower losses below 0.01 dB/90° can be achieved with a few micron bending radius using Euler bends[7] on 3 µm SOI.
A library of compact and low-loss passive components, such as wavelength multiplexers and filters, has been already developed on the 3 µm SOI platform. Polarization independent operation is achieved with symmetrical strip waveguides. Athermal wavelength multiplexing has been demonstrated using successive polymer and SOI waveguides that cancel each other's temperature dependency (Fig. 3).
Thermo-optic tuning and switching has been demonstrated with both metallic and implanted (all-Si) heaters reaching <1 µm response time and 24 mW/π efficiency. High-speed (>25 GHz) SiGe modulators and Ge PDs have also been demonstrated on 3 µm SOI.
The development of a similar passive component library is now being developed on the 12 µm SOI platform where high topography is a great challenge for lithography.

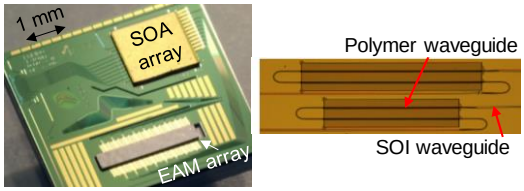

Fig. 3: Passive components on 3 µm SOI with hybrid-integrated amplifier and modulator arrays on top (left). Athermal polymer-Si waveguide combination (right).

Long-wavelength (1.3 µm) VCSELs

The single-mode VCSELs reported here are based on Vertilas' unique InP Buried Tunnel Junction (BTJ) design. These fixed-polarization VCSELs have ~1.3 µm wavelength to minimize chromatic dispersion in SSMF. They have been optimized for high bandwidth using a very short optical cavity surrounded by dielectric mirrors, as well as a small mesa surrounded by benzo cyclobutene (Fig. 4). Measured side mode suppression ratio (SMSR) is > 40 dB and maximum optical output power is 3.8 mW at a roll-over current of 16 mA (Fig. 5). The operating voltage is <1.8 V and the measured 3-dB modulation bandwidth is 17 GHz at room temperature (Fig. 6). This is the highest bandwidth reported for a SM 1.3 µm VCSEL.

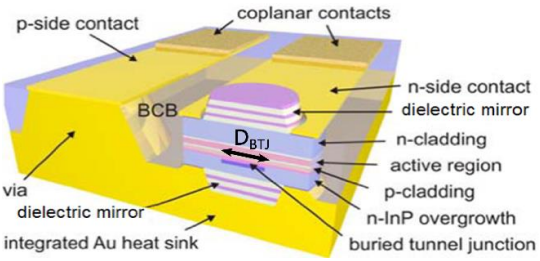

Fig. 4: Cross section of a 1.3 µm VCSEL.

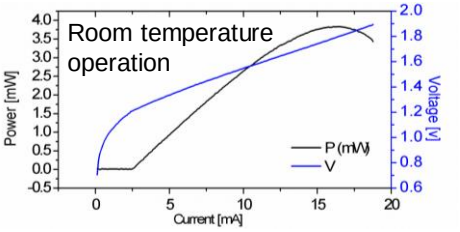

Fig. 5: Output power and diode voltage versus diode current showing threshold current of 2.5 mA and maximum optical power of 3.8 mW with voltage < 1.8 V.

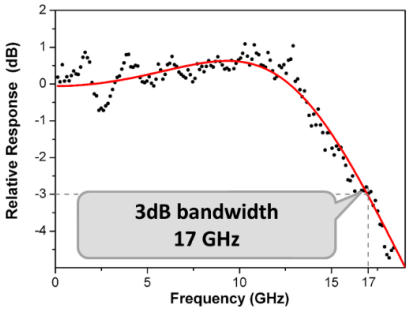

Fig. 6: VCSEL bandwidth measurement.

VCSEL-based transmission experiments

The suitability of the 1.3 µm VCSELs for 400G transceiver integration was studied by coupling light from a directly modulated VCSEL to SSMF, and then to a commercial 40G photoreceiver[9]. The VCSEL was modulated with a 0.13 µm SiGe BiCMOS 4-channel driver circuit that was wire bonded to a 2-ch 1325 nm VCSEL array (Fig. 7). Transmission measurements were made without active cooling and the free-running temperature of the VCSEL was measured with a thermistor to be ~30°C. The measured 3-dB bandwidth of the VCSEL was 15.6 GHz. The maximum received optical power was 1 dBm in back-to-back configuration with an extinction ratio (ER) of 5.2 dB at 28 Gb/s. At 40 Gb/s the ER dropped to 2.8 dB due to limitations in generating the electrical input signal. Eye diagrams with 220 acquired waveforms and the corresponding bit error rate (BER) curves were measured for both 28 Gb/s and 40 Gb/s data rates, and for different SSMF lengths[9] (Fig. 7).
Error-free operation (BER < 10^{-11}) was achieved with sensitivity of -10.6 dBm at 28 Gb/s, with 3.3 dB power penalty after 20 km of SSMF and residual power budget of 1.6 dB. At 40 Gb/s this

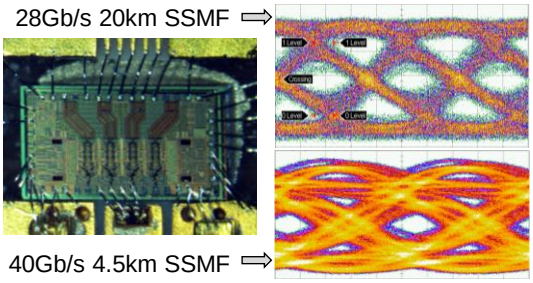

Fig. 7: Wire-bonded driver-VCSEL assembly and measured eye diagrams at 28 and 40 Gb/s.

was achieved with -4.9 dBm sensitivity, 1.5 dB penalty after 4.5 km of SSMF and residual power budget of 3.2 dB. The measured power consumption of the transmitter assembly was ~190 mW, of which 170 mW was consumed by the driver and feed forward equalization (FFE) and ~20 mW was required for VCSEL biasing. This translates into an energy efficiency of 4.75 pJ/bit at 40 Gb/s. With error-free transmission without any digital signal processing (DSP) this leads to 29 fJ/bit/km at 28 Gb/s over 20 km of SSMF. These results make the directly modulated 1.3 µm VCSELs a very attractive choice for realizing 400G transceivers.

Hybrid integration on SOI

For realizing 400G transceivers the VCSELs can be integrated with SOI chips where Mach-Zehnder interferometers or Echelle gratings can be used for wavelength multiplexing in a very small footprint (<1 mm^2). With 25–56 Gb/s VCSELs and 4–16 channels the transceiver bandwidth can be anything from 100G to 800G. The original goal was to integrate VCSELs with 12 µm SOI chips that offer perfect matching to SSMF. This work is still underway due to challenges with 12 µm SOI processing and test board electronics. Some intermediate results are shown in Fig. 7. Integrating VCSELs and PDs on 12 µm SOI could offer the most compact and low-loss transceivers.

However, the VCSEL mode field was found to be better matched to much thinner SOI waveguides and coupling experiments were then carried out between VCSELs and 3 µm thick SOI waveguides. The measured coupling loss to 2.6 µm wide SM rib waveguides was only 3.2 dB, which matches well with mode coupling simulations. By adjusting the waveguide width the coupling loss should drop below 2 dB. Maximum VCSEL power coupled to a 3 µm SOI waveguide was 1.8 mW. VCSEL integration on 3 µm SOI offers the possibility for using semiconductor optical amplifiers (SOAs) and electro-absorption modulators (EAMs) on 3 µm for even higher bandwidths and longer communication distances.

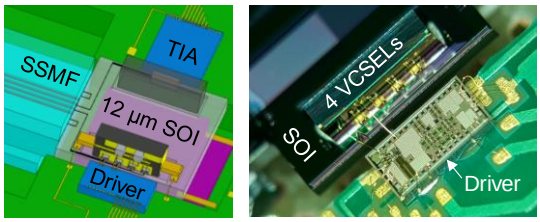

Fig. 7: Designed 4-ch transceiver assembly (left). Test assembly with 28 Gb/s VCSELs (right).

Conclusions and outlook

The combination of directly modulated 1.3 µm VCSELs, PDs and Thick-SOI technology is a promising path towards 400G transceivers with 1–40 km reach. The individual building blocks have already been demonstrated. The main technological barrier is now the high topography on 12 µm SOI wafers, which requires some layout redesign and process optimization. Even with VCSEL coupling to 3 µm SOI the 12 µm SOI chips with spot-size converters (Fig. 1) would be the ideal choice for efficient coupling to SSMF.

Acknowledgements

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