Segmented Optical Transmitter comprising a CMOS Driver Array and an InP IQ-MZM for Advanced Modulation Formats

Michael Vanhoecke, Alessandro Aimone, Nikos Argyris, Stefanos Dris, Renato Vaernewyck, Koen Verheyen, Marko Gruner, Gerrit Fiol, Dimitris Apostolopoulos, Hercules Avramopoulos, Guy Torfs, Xin Yin and Johan Bauwelinck

***Abstract*—Segmented Mach-Zehnder modulators are a promising solution to generate complex modulation schemes in the migration towards optical links with a higher-spectral efficiency. We present an optical transmitter comprising a segmented-electrode InP IQ-MZM, capable of multi-level optical signal generation (5-bit per I/Q arm) by employing direct digital drive from integrated, low-power (1 W) CMOS binary drivers. We discuss the advantages and design trade-offs of the segmented driver structure and the implementation in a 40 nm CMOS technology. Multi-level operation with combined phase and amplitude modulation is demonstrated experimentally on a single MZM of the device for 2-ASK-2PSK and 4-ASK-2-PSK, showing potential for respectively 16-QAM and 64-QAM modulation in future assemblies.**

***Index Terms*—CMOS integrated circuits, optoelectronic devices, optical transmitters, electrooptic modulation**

I. Introduction

THE past decade has seen a tremendous increase in internet traffic fueled by popular video services and the rapid expansion of mobile data traffic. This exponential increase has been stressing the capacity of optical networks since it becomes increasingly difficult to overcome optical impairments as optical channel speeds increase. With the introduction of the long-haul OIF 100G standard, the transition was made from a simple On-off keying (OOK) modulation format to the higher spectral efficient DP-QPSK. As such, coherent technology has emerged as the backbone of optical networks allowing advanced phase modulation as well as leveraging the capabilities of digital signal processing (DSP). As the demand for data traffic keeps on rising, higher-order modulation will provide the path to further exploitation of the inherent capacity of optical fiber links [1]. Moreover, not only the increase in data traffic, but also the rate of this traffic is determining technology choices. The volatility of internet traffic requires novel flexible network architectures and feeds the need for components capable of introducing flexibility in the modulation format and spectral utilization [2].

In recent years, segmented transmitter architectures implementing an electro-optical digital-to-analog conversion (DAC) functionality have shown to be a promising candidate for the efficient generation of high-speed multi-level optical signals. A segmented electrode Mach-Zehnder Modulator (SEMZM) is paired with a dedicated driver IC to generate multi-level optical signals from multiple binary electrical drive signals. The concept already dates back to 1980 [3], but due to the advancements in OOK signaling it was not until recent that segmented transmitters regained attention. In the light of 100 GbE development several PAM-4 transmitters using two binary weigthed segments were demonstrated [4]–[6]. 10 Gbit/s PAM-8 intensity modulation was shown with a hybrid configuration of a 3-bit SEMZM and an electrical DAC [7]. IQ-modulation for coherent communication was demonstrated using two 2-bit SEMZMs for 16-QAM at 28 GBd [8] and for 64-QAM at 32 GBd using two 4-bit SEMZMs [9]. Only the driver in [8] is benefiting from the potential of the small lumped capacitances of a segmented electrode with a low-power CMOS logic driver. No retiming circuitry is present however, making it not readily extendable to a higher resolution and speed, as timing matching is the most challenging aspect. The state-of-the-art SEMZM in [9] is driven with a BiCMOS SiGe driver and has fixed passive delay lines to match the timing. As a result, two different versions of the driver chip are required for the IQ-implementation which is undesirable in a cost-effective solution. Moreover, the passive delay lines result in a rather large die size of 7.5 mm^2.

In this work, we present a prototype optical transmitter based on an Indium Phosphide (InP) IQ-MZM with a 5-bit segmented electrode. The SEMZM is driven by novel, low power 40 nm CMOS electronics that consume only 1 W per I/Q arm. The array of output driving stages utilizes

M. Vanhoecke, R. Vaernewyck, K. Verheyen, G. Torfs, X. Yin and J. Bauwelinck are with the Department of Information Technology, Ghent University - IMEC - iMinds, 9052 Ghent, Belgium (e-mail: michael.vanhoecke@intec.ugent.be; renato.vaernewyck@intec.ugent.be; koen.verheyen@intec.ugent.be; guy.torfs@intec.ugent.be; xin.yin@intec.ugent.be; johan.bauwelinck@intec.ugent.be).

A. Aimone is with the Technische Universitat Berlin, Berlin 10623, Germany, and also with the Department of Photonic Components , Fraunhofer Heinrich-Hertz-Institute, Berlin 10587, Germany (e-mail: alessandro.aimone@hhi.fraunhofer.de).

N. Argyris, D. Apostolopoulos, H. Avramopoulos are with the Photonics Communications Research Laboratory, National Technical University of Athens, Zografou 15780, Greece (e-mail: nargyris@mail.ntua.gr; apostold@mail.ntua.gr; hav@mail.ntua.gr).

S. Dris was with the Photonics Communications Research Laboratory, National Technical University of Athens, and is now with VPIphotonics GmbH, 10587 Berlin, Germany (email: stefanos.dris@vpiphotonics.com).

M. Gruner and G. Fiol are with the Department of Photonic Components , Fraunhofer Heinrich-Hertz-Institute, Berlin 10587, Germany (e-mail: marko.gruner@hhi.fraunhofer.de; gerrit.fiol@hhi.fraunhofer.de).

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voltage mode CMOS inverters to maximize the swing and to minimize the power consumption. A tunable bidirectional timing architecture is proposed to match the optical velocity in the electrical chip. The structure allows for the creation of multi-level optical signals using only binary signals from the driver array. An encoder circuit is included to match the input binary word to the segment configuration so the transmitter can be effectively used as an electro-optical DAC. The device is demonstrated and evaluated with proof-of-concept experiments on a single SEMZM, showing high potential for the generation of multiple, higher-order modulation formats in future assemblies. It constitutes a promising approach towards addressing future flexible network needs for high capacity and low power consumption.

II. Segmented Transmitter Configuration

A. Advantages of the Segmented Approach

The segmentation of the electrodes of an MZM has several advantages. A first asset is the inherent DAC functionality by splitting up the electrode. Traditional solutions for multi-level optical signal generation include multiple nested MZMs or a single MZM driven by an electrical DAC with a linear driver. The former solution is bulky and difficult to scale whereas the latter uses expensive and power-hungry electronics. By using the DAC capabilities of the segmented structure, a compact and power-efficient solution can be implemented. It was already shown in [3] for a low-speed design that an MZM with a binary weighted segmented electrode, directly driven by digital signals can be used to generate a multi-level optical output. In [10] it is illustrated that in theory it is possible to generate arbitrary QAM-signals using a single MZM device and binary drive signals. However, the presented concept lacks a practical demonstrator.

A second benefit of the segmented transmitter is that it can resolve the trade-off between the electro-optical bandwidth and a low V_π voltage. In a common MZM, an RF signal is propagation on a traveling wave (TW) electrode alongside the modulator. However, there is an inherent mismatch in the velocity of the optical and electrical signal propagation. The technology dependent $V_\pi L$ constant dictates that a longer interaction length L is needed to reduce the drive voltage V_π. In the common TW MZM, the elongation of the electrode is limited by a reduction in the bandwidth due to the velocity mismatch between the electrical and optical signal and by RF losses alongside the TW electrode. To break this limit, the task of the velocity matching is shifted from the TW electrode to the electronic driver chip. In the presented transmitter, the drive signals are applied sequentially to the segments with precision tunable timing circuits to match the correct optical signal delay between segments. As a result, the interaction length can be elongated without suffering from velocity mismatch and therefore the driving voltage can be lowered. This paves the way to use electronics with low voltage swings from a low-power deep submicron CMOS technology. Moreover, since at each segment the signal is resampled and there is a dedicated driver stage, the transmitter is also not limited by RF losses as in regular TW modulators.

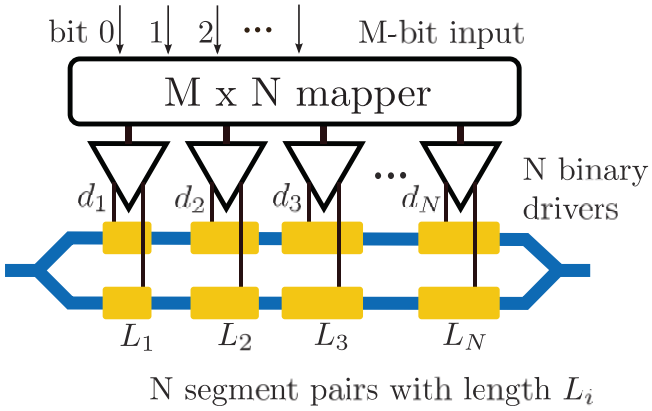


Fig. 1. DAC principle in a segmented transmitter

Lastly, since the electrode is split into short segments, a segment can be considered as a lumped capacitance and there is no longer a need for a power-hungry 50 Ohm interface. As noted in [11], a separate independent low-voltage transmission line driver can be used, whereas the segment driver can be high voltage and it is not loaded with 50 Ohm. In an advanced CMOS technology this allows using an efficient CMOS inverter topology as a driving stage rather than a current mode logic (CML) output stage.

B. Optical DAC functionality

A general single-arm configuration is depicted in Fig. 1. For IQ-modulation, there is one driver array in each arm of an IQ-MZM so that multi-level signals can be generated in quadrature. The electronic chip takes a binary input word of M bits and encodes it to an array of N output drivers. The electrodes are split in segment pairs of length L_i The modulator is driven differentially in a push-pull configuration as is also the case in common traveling-wave MZMs. The binary output signals d_i determine if the respective segment pair is contributing to the optical output:

$$\Delta\phi \sim \sum_{i=1}^{N} d_i L_i \tag{1}$$

It can be seen that the effective interaction length is altered to change the modulation level. There are several possibilities to choose the number of segments and their respective lengths. The two most straightforward methods are a binary weighted and a thermometer code implementation. When the segment lengths are binary weighted, a binary input word can be directly applied without the need for a mapper circuit. The number of segments and output channels is minimized which benefits integration complexity and power consumption. Although the total output capacitance to be driven remains equal, the power consumption of dedicated circuits, e.g. retiming cells, is fixed per channel. Hence, minimizing the number of output channels also minimizes power consumption. A disadvantage in the binary weighted approach is the large difference in the segment lengths, making it more difficult to drive each segment with equal output channels. Eventually

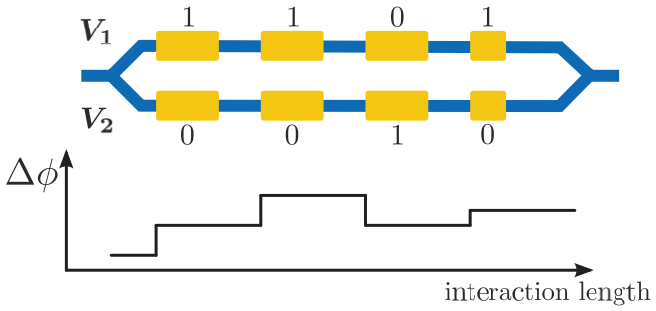


Fig. 2. Example drive state in which the phase difference between the arms gets a net contribution of 1.5 segment pairs. Two segments and a half-length segment are contributing with positive polarity, while one segment is contributing with negative polarity.

the number of segments is limited by the maximum length for which the most significant bit (MSB) segment can still considered to be a lumped capacitance, larger segment lengths will limit the bandwidth of the opto-electrical conversion. A thermometer code implementation on the other hand, has the advantage that all segment lengths are equal. The drawback of this configuration is that the number of segments increases exponentially ($N = 2^M - 1$). The power consumption rises accordingly and the integration becomes impractical due to the many RF connections from the driver to the modulator.

Additional attention is required when using a CMOS inverter topology rather than the common differential pair output. When considering the transfer function of a MZM, in which V_1 and V_2 are the sum of the various weighted segment voltage contributions, applied to respectively the upper and lower arm of the MZM, one can see that the difference between the voltages controls the amplitude of the optical signal, while the sum of the voltages determines the phase of the output:

$$\frac{E_{out}}{E_{in}} = exp\left(j\frac{V_1+V_2}{2V_\pi}\pi\right) cos\left(\frac{V_1-V_2}{2V_{pi}}\right) \quad (2)$$

With a differential pair output, the sum of the contributions to both arms is always constant. So when switching a segment pair on or off, only the amplitude changes. When using the CMOS inverter topology, there is no real differential signal and the sum of the voltages differs when altering the numbers of segments contributing to the modulation. Therefore, there is an undesired phase shift, causing problems in an IQ configuration. As a solution, rather than just switching segment pairs on or off, segments pairs with different polarities are combined to create an output level. In the differential pair case, the polarity would only be used to switch between the negative and positive phase output. The polarities of the segments are switched using a pseudo-differential CMOS output, hence keeping V_1+V_2 constant and only influencing the amplitude. Note that a regular thermometer coding with all equal segments is not readily applicable anymore. E.g. whereas 4 equal segments would be sufficient to implement a 3 bit functionality (4 positive and 4 negative levels) when segments can be switched off, only a 2 bit resolution would remain with the proposed driving scheme. To preserve the resolution, we propose to half the length of one the segments. An example drive state is shown in Fig. 2. Two and a half segment pairs are contributing with a positive polarity and one with a negative polarity resulting in a positive net contribution of one and a half segment. This 4-segment configuration can implement a 3 bit functionality.

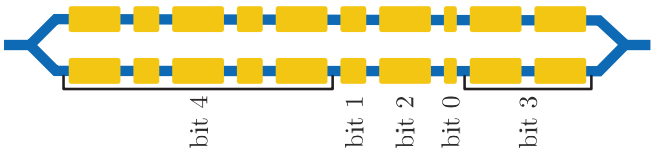


Fig. 3. 5-bit segment configuration.

The proposed principle is used to implement a 5-bit crossover solution between full binary weighted and thermometer coding. The final configuration is depicted in Fig. 3. Three different binary weighted lengths of segments are used. For the two most significant bits, a combination of these segment lengths are grouped and jointly driven. The position of longer and shorter segments are altered so they can be connected to a bond pad array with a fixed pitch. While the segments are implemented with a 5-bit resolution, the actual resolution will be lower due to the non-linear cosine dependency in the MZM transfer function. It is the goal of the 5-bit configuration to add redundancy and compensate for the non-linearity in the transfer function, rather than just driving the MZM in its linear region and hence sacrificing too much extinction ratio.

III. CMOS Electronics and SEMZM

The driver IC was developed in a 40 nm CMOS LP (low-power) technology with a 3.3 mm × 1.65 mm footprint, with 3.3 mm also being the active length of the MZM. The chip features a 10-channel differential output array, matching the segment configuration proposed in Fig. 3. A 5 × 10 mapper circuit is included on chip to map the 5 input bits to the 10 output channels. The core of the chip is a timing architecture with tunable delay cells to match the optical signal propagation in the electronics. The designed timing control implementation is shown in Fig. 4 and can be programmed through an SPI interface. A clock signal is propagating alongside the optical signal and is tapped in each output channel where it is fed to a flip-flop to retime the incoming data signals. A first demonstration of a driver chip with resampled data was shown in [12]. The implementation we propose in this paper shows several refinements to the concept. The transmission line is designed to match the interchannel delay in the modulator. However, since deviations in the velocity of either the electrical or optical signal propagation in the fabricated devices can cause accumulating delay differences, the transmission line delay is made tunable by loading it with digitally controlled capacitors in between channels. A second level of tunability is added as an in-channel independent delay control to compensate for process variations and load differences. This control is implemented by including a precision delay control circuit before feeding the tapped clock to the retiming cell. Finally,

a coarse delay circuit is included in the data path before the retiming cell in each channel. The purpose of this delay is to ensure that the data signal falls within the valid retiming window of the flip-flop, which is crucial since the timing difference between the first and the last channel can be close to a symbol period for high bit rates. The coarse delay cells also allow to switch around the propagation direction of the electrical drive signals, so that the driver chip can be used in multiple orientations. This bidirectionality is typically important in an assembly with an IQ-modulator, since it allows using an identical driver for both I and Q branches. The drivers need to be placed a opposite sides of an IQ MZM chip, so one of them nees to be rotated with respect to the other. It also relaxes the assembly constraints as both a flip chip approach and a wirebond approach can be taken. As stated in the introduction, the lack of this flexibility causes the state-of-the-art transmitter in [9] to use two different versions of the driver chip.

The output driver consists of a pseudo-differential tapered CMOS inverter chain. The first few stages are CMOS trans-impedance amplifier (TIA) stages to amplify the data signal to full swing. The preceding circuit block is a CML-to-CMOS conversion circuit to convert the CML logic, which is used from the input stage until the retiming flip-flop, but does not yet deliver full swing output. The last couple of inverter stages in the output include cross-coupled inverters to minimize timing offsets in the pseudo-differential paths. The CMOS inverter is an interesting topology as an output driver because it delivers a rail-to-rail output which is essential when working with a low supply voltage (1.1 V) technology. It also consumes negligible static power consumption and is very suited to drive capacitive loads. The interaction length is made sufficiently long to be able to drive the modulator with the 2.2 V differential output from the CMOS chip. The output drivers are designed to drive a capacitive segment ranging from 85 fF to 240 fF depending on the segment length. Due to a sub-optimal operation of the retiming cells, the speed in this first version of the driver chip is limited to 15 GBaud. However, the output stages already showed their capability to drive loads up to 28 GBaud. In Fig. 5 it can be seen that the horizontal eye opening is wide open and the rise and fall times have margin for higher speed. The vertical opening could even benefit from increased data rates as the effect of the overshoot will be less. The total power consumption of a single driver chip is around 1 W, the output drivers contributing 10×40 mW (i.e. without taking into account the timing and mapping circuitry which consumes around 0.6 W). The IQ-drivers in [8] and [9] consume respectively 0.5 W and 0.75 W per arm, without the retiming capability though. As a comparison, a solution with an electrical DAC functionality easily consumes 2 W [13] clearly illustrating the potential of a segmented transmitter.

The fabricated IQ InP segmented modulator (IQ-SEMZM) footprint is 10 mm $\times$ 0.82 mm. It includes spot-size converters at the optical input and output, deeply-etched ridge wave guides, and multi-mode interferometers as splitters and couplers [14]. Each of the two SEMZMs has an active length, $L_a = 2945\,\mu m$, divided in 10 segments in a configuration as depicted in Fig. 3. These segments match the driver IC outputs

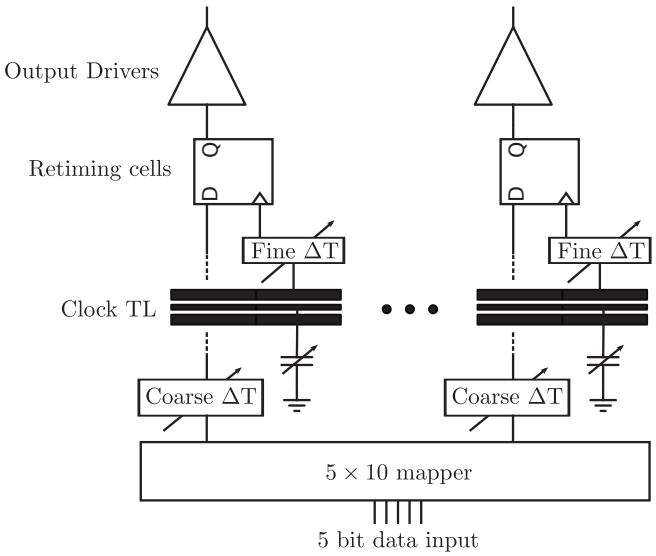
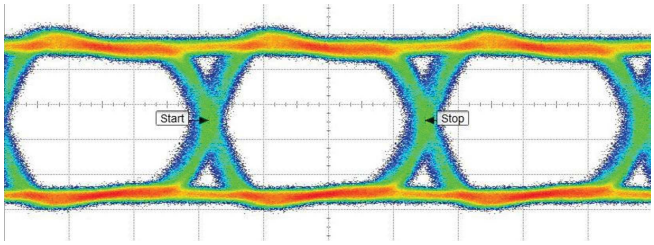
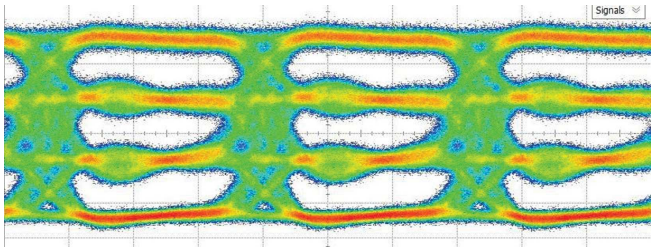


Fig. 4. Timing architecture with the different levels of tunability indicated.



(a)



(b)

Fig. 5. Optical eye diagrams for (a)NRZ and (b)PAM4 modulation at 15 Gbaud (20 ps/div). The rise time of the eyes indicates that the speed is not limited at the output stage.

in both number and pitch. The fiber-to-fiber insertion loss is 10 dB at 1550 nm. The measured DC switching voltage V_π is equal to 1 V when a bias voltage of 7 V is applied, leading to a modulation efficiency of 0.29 V cm. Since the IC driving voltage is well above $2.V_\pi$ full modulation depth is ensured.

In the final assembly, two driver chips (I & Q) and the IQ-SEMZM will be mounted on opposite sides of a ceramic interposer. To enable early testing however, a 4-layer PCB was designed to host the IQ-modulator and a single CMOS driver (i.e. driving a single branch of the IQ structure). The distance between the two dies was minimized to keep parasitics low, to allow to directly wire bond the outputs of the driver. The driver inputs, as well as the bias and SPI connections, were wire bonded to the board. A detail of the PCB with the two

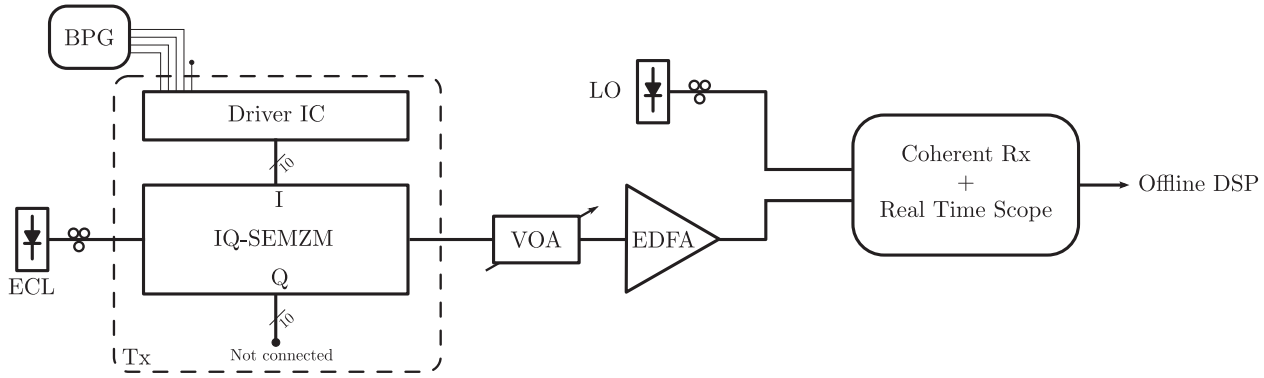


Fig. 6. Experimental setup for the evaluation of the driver IC and the MZM for coherent modulation formats in back-to-back configuration.

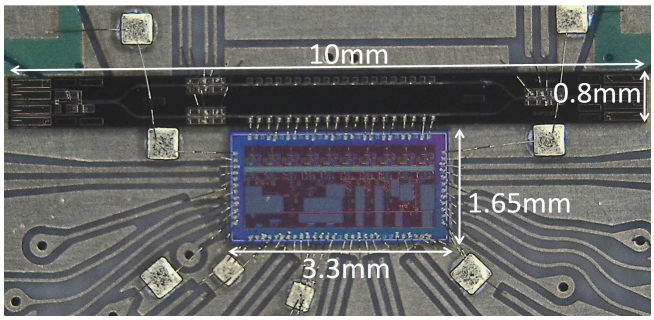
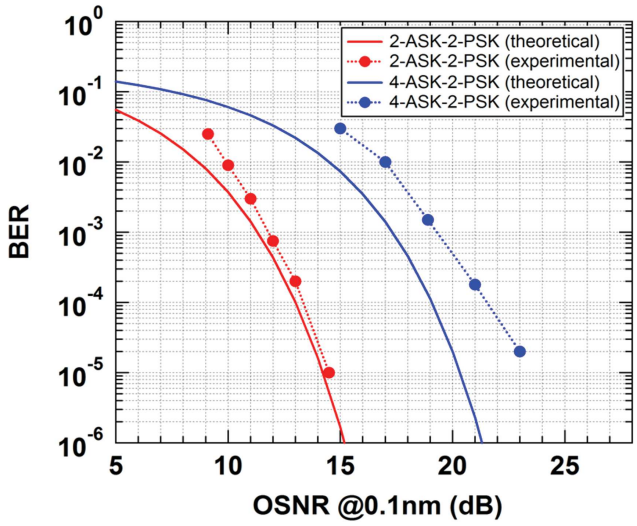


Fig. 7. The driver and the MZM integrated circuits are bonded directly on a test PCB for quick verification.

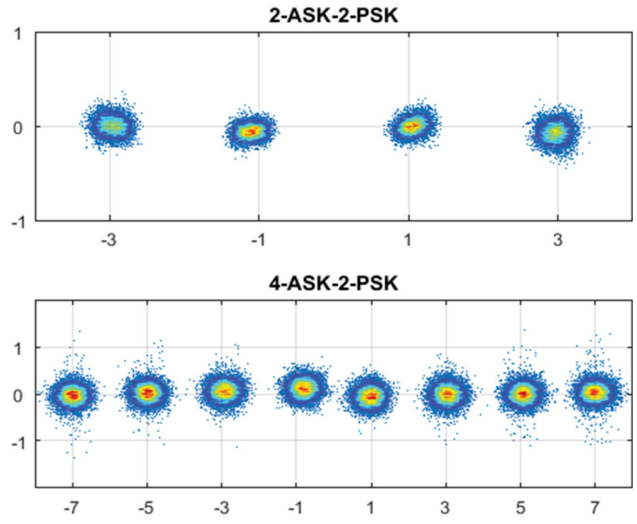
bonded dies is shown in Fig. 7. The limited minimal trace width and spacing on a PCB allows connection of only 4 out of the 5 available input bits. Nonetheless, the operational concept and the designed architectures can be verified and optical amplitude/phase modulation can be evaluated.

IV. Performance Evaluation

The experimental setup shown in Fig. 6 was employed to evaluate the operation principle of the single SEMZM. The four input streams of the driver were provided by a 4-channel Bit Pattern Generator (BPG) operating at 15 Gb/s, allowing the SEMZM to generate multi-level signals with 4-bit resolution. The timing of the different output stages is optimized manually by inspecting the optical OOK eye resulting from driving individual outputs. Biasing the modulator at the zero transmission point, combined amplitude and phase modulation was realized generating 4 and 8 point constellations in the form of 2-ASK-2-PSK (2 bits/symbol) and 4-ASK-2-PSK (3 bits/symbol). These formats were selected to show the potential for 16- and 64-QAM generation, assuming that the second MZM of the device is driven in the same way in future assemblies. The modulated signal output was then launched into a Variable Optical Attenuator (VOA) followed by an EDFA, in order to vary the optical signal to noise ratio (OSNR) and obtain back-to-back BER curves. The signal was received with a polarization-diversity coherent receiver and the resulting photocurrents were captured by a digital real time oscilloscope (33 GHz & 80 GSa/s) for further offline



(a)



(b)

Fig. 8. (a) BER vs. OSNR for the two modulation formats and a comparison with the theoretical curve for an AWGN channel.(b) Constellation diagrams at the highest OSNR values

DSP. In the DSP, the signal was resampled at $4\,\mathrm{Sa/s}$ and after the Square Timing algorithm the resynchronized signal had $1\,\mathrm{Sa/s}$. The phase-entropy frequency offset estimation algorithm [15] was applied to compensate for the residual frequency difference between transmitter and local oscillator (LO) lasers, whereas the blind phase search algorithm (BPS) was used to recover and track the phase of the signal [16]. Prior to symbol detection, the signal was fed to a 31 tap symbol spaced linear equalizer. Fig. 8(a) depicts the measured BER of the two modulation formats as a function of OSNR (dotted lines). In order to roughly estimate the implementation penalties, the theoretical curves that would be obtained in an ideal AWGN channel are included in the plot. To extract the theoretical curves of the Error Probability versus OSNR, the theoretical OSNR was correlated to the E_b/N_0, based on the fact that the signal bandwidth is twice the symbol rate as is approximately the case in unshaped NRZ signaling. The SNR-OSNR conversion was done using the relationship stated for a single polarization channel given in [17]. The 2-ASK-2-PSK signal exhibits negligible penalty ($< 1\,\mathrm{dB}$) for a BER equal to a hard-decision (HD)-FEC limit of $3.8 \cdot 10^{-3}$, whereas for the 8-level signal (4-ASK-2-PSK) the penalty is $1.95\,\mathrm{dB}$. Fig. 8(b) shows the constellation points generated by the single SEMZM. In an IQ implementation (i.e. 2 SEMZM branches), two of these 4- and 8 level signals can be combined in quadrature to generate 16- and 64 QAM formats.

V. Conclusion

Advantages and trade-offs in the design of a segmented transmitter were discussed and the implementation of a driver IC in a $40\,\mathrm{nm}$ CMOS process was shown. The transmitter utilizes an efficient CMOS inverter topology in the output stage and features a novel tunable timing architecture to match the optical signal velocity. A 10-segment configuration is proposed to implement a 5-bit DAC functionality. By avoiding a purely electrical DAC, a power consumption of less than $1\,\mathrm{W}$ is achieved. A first optical transmitter prototype using a segmented-electrode InP IQ-MZM driven by the low power CMOS drivers has been demonstrated. Negligible implementation penalties for 2-ASK-2-PSK and 4-ASK-2-PSK formats are achieved, showing potential for generating formats up to 64 QAM in future assemblies, using only binary driving signals.

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