MIMO Pre-Equalization and DFE for High-Speed Off-Chip Communication

Lennert Jacobs *, Mamoun Guenach [†] and Marc Moeneclaey *

 * Department of Telecommunications and Information Processing Ghent University, Ghent, Belgium
 Email: {lennert.jacobs,marc.moeneclaey}@telin.ugent.be
 † Nokia Bell Labs, Antwerp, Belgium
 Email: guenach@ieee.org

Abstract—In this contribution, we present a multipleinput multiple-output (MIMO) transceiver scheme for high-speed chip-to-chip communication over low-cost electrical interconnects. Linear MIMO pre-equalization at the transmitter is combined with decision feedback equalization (DFE) at the receiver to counteract the adverse effect of inter symbol interference (ISI) and crosstalk (XT). Considering an energy constraint at the transmit side, we derive elegant closed-form expressions for the equalization filters under a minimum mean square error (MMSE) criterion. Numerical analysis shows that the combination of linear MIMO pre-equalization and MIMO DFE allows to significantly improve the reliability of future high-speed off-chip communication.

I. INTRODUCTION

Due to the ever increasing bit rates that are required on low-cost dispersive electrical chip-to-chip interconnects, severe signal integrity issues are currently being dealt with. High-frequency attenuation of the transmitted signal, caused by skin effect and dielectric loss, gives rise to inter symbol interference (ISI), whereas crosstalk (XT) originating from mutual coupling between neighboring wires further degrades the signal quality. In order to combat ISI, most state-of-the-art transceivers apply non-linear decision feedback equalization (DFE) at the receiver or Tomlinson-Hirashima precoding (THP) at the transmitter [1]-[4]. In addition, numerous XT cancellation techniques have been proposed, such as [5]-[8]. Since XT is expected to dramatically increase because of growing bit rates and reduced circuit dimensions, attempting to exploit the useful information in the XT signals seems to be more advantageous and effective than XT cancellation. In [9], multiple-input multiple-output (MIMO) pre-equalization using THP was proposed to improve the reliability of 10 Gbps Ethernet over UTP cables, also known as 10GBASE-T. However, also on electrical chip-to-chip interconnects, XT can be put to good use by applying linear MIMO equalization at the receiver side, as shown in [10]. These results were further improved in [11] by applying DFE. In the latter scheme, however, both the feedforward and the feedback equalization filters are situated at the receiver side, which demands additional chip area and increases the power consumption. In order to distribute the required chip area and power consumption among the transmitter and the receiver chip, we propose in this paper to move the MIMO feedforward filter from the receiver to the transmitter side. The resulting combination of linear MIMO pre-equalization at the transmitter, also called pre-emphasis, and MIMO DFE at the receiver is shown to significantly improve the reliability of future highspeed chip-to-chip communication over low-cost electrical interconnects. Given a transmit energy constraint, we derive an elegant closed-form matrix expression for the finite impulse response (FIR) pre-equalization and feedback filters under a minimum mean square error (MMSE) criterion.

II. SYSTEM MODEL

Fig. 1 displays a baseband communication scheme transmitting L real-valued data streams $\{a^{(l)}(k)\}$, with $1 \leq l \leq L$, at a symbol rate 1/T; the symbol streams are assumed to be spatially and temporally independent, i.e., $E\left[a^{(l_1)}(k_1) a^{(l_2)}(k_2)\right] = \sigma_a^2 \delta_{l_1-l_2} \delta_{k_1-k_2}$. Before being applied to the MIMO pre-equalization matrix $\mathbf{H}_{\rm pr}$, the data symbols are upsampled by a factor $N_{\rm pr}$, i.e., $(N_{\rm pr} - 1)$ zeroes are inserted between every two symbols. Hence, the $L \times L$ pre-equalization filters operate at (a multiple of) the symbol rate $1/T_{\rm pr} = N_{\rm pr}/T$; the



Figure 1: MIMO DFE scheme.

impulse response $h_{\rm pr}^{(r,p)}(m)$ of the pre-equalizer filter linking the *p*-th input of the equalization matrix with the *r*-th output is assumed to be the (r, p)-th entry of $\mathbf{H}_{\rm pr}$. In this way, the *l*-th output of $\mathbf{H}_{\rm pr}$ is obtained as the sum of the outputs of the *L* pre-equalization filters $h_{\rm pr}^{(l,p)}(m)$, with $1 \leq p \leq L$. The *L* outputs of the preequalization matrix are each applied to a pulse shaping filter $H_{\rm tr}(f)$ and transmitted on a typical electrical chipto-chip interconnect consisting of *L* parallel lanes. The continuous-time signal at the outputs of the transmitter can be written as

$$s(t) = \sum_{q=1}^{L} \sum_{k} s_{k}^{(q)}(t), \qquad (1)$$

where $s_k^{(q)}(t)$ is the signal transmitted on the q-th output of the transmitter corresponding to the symbol vector $\mathbf{a}(k) = (a^{(1)}(k), \dots, a^{(L)}(k))^{\mathrm{T}}$, with the superscript T denoting matrix transpose:

$$s_{k}^{(q)}(t) = \sum_{p=1}^{L} \sum_{n} a^{(p)}(k) h_{\rm pr}^{(q,p)}(n) h_{\rm tr}(t - kT - nT_{\rm pr}).$$
⁽²⁾

The L direct channels between the transmitter and the receiver along with the XT channels are captured by the channel matrix $\mathbf{H}_{ch}(f)$; the (r,p)-th entry $H_{ch}^{(r,p)}(f)$ denotes the frequency response between the p-th transmitter and the r-th receiver, with $1 \leq r, p \leq L$. At the receiver, the L signals affected by channel dispersion and XT, are each filtered by an analog receiver filter $H_{rec}(f)$ and sampled at the symbol rate 1/T; note that the sampling instants $\{kT + \varepsilon T\}$ depend on the sampling phase ε . The stationary noise at the receiver is represented

by the additive noise samples $n^{(1)}(k), \ldots, n^{(L)}(k)$. The variables $u^{(l)}(k)$ based on which the symbol decisions are taken, are obtained by subtracting from the received samples the outputs of the MIMO equalizer matrix \mathbf{H}_{FB} representing the $L \times L$ symbol-spaced feedback equalizer filters and scaling the result with a factor $1/\alpha$. Note that the pre-equalization filters operate at the rate $N_{\rm pr}/T$, whereas the feedback filters operate at the symbol rate 1/T. Furthermore, the feedback filters are strictly causal, since only past symbol decisions can be applied to the inputs of \mathbf{H}_{FB} . If the off-diagonal equalizer filters $h_{\rm pr}^{(r,p)}(m) = 0$ and $h_{\rm FB}^{(r,p)}(m) = 0$, $\forall m$ and with $r \neq p$, the MIMO system from Fig. 1 degenerates to a SISO preequalization scheme with DFE at the receiver. When all feedback filters have zero coefficients only, the MIMO DFE scheme reduces to a linear MIMO pre-equalization scheme.

III. MMSE MIMO DFE

Assuming that the past symbol decisions which are applied to the feedback filter are correct, the outputs $\{u^{(l)}(k)\}$ of the MIMO DFE equalization scheme, with $1 \le l \le L$, are given by

$$u^{(l)}(k) = \frac{1}{\alpha} \left[\sum_{p=1}^{L} \sum_{m} h^{(l,p)}(m) a^{(p)}(k-m) + n^{(l)}(k) - \sum_{p=1}^{L} \sum_{m>0} h^{(l,p)}_{\text{FB}}(m) a^{(p)}(k-m) \right],$$
(3)

where $h^{(l,p)}(m)$ is defined as

$$h^{(l,p)}(m) = \sum_{q=1}^{L} \sum_{m_1} h_{\rm pr}^{(q,p)}(m_1) g^{(l,q)}(mN_{\rm pr} - m_1)$$
(4)

and the sequences $\{g^{(l,q)}(m)\}$, with $1 \leq l,q \leq L$, are obtained by sampling at instants $\{mT_{\rm pr} + \varepsilon T\}$ the impulse responses of the corresponding cascades $H_{\rm tr}(f)H_{\rm ch}^{(q,p)}(f)H_{\rm rec}(f)$. Ideally, in the absence of noise, ISI and XT, we should have $u^{(l)}(k) = a^{(l)}(k)$.

In practice, the pre-equalization and feedback filters are finite impulse response (FIR) filters with a limited number of filter taps; we assume $h_{\rm pr}^{(r,q)}(m) = 0$ for $m \notin$ $[-L_{\rm pr,min}, L_{\rm pr,max}]$, yielding $L_{\rm pr} = L_{\rm pr,min} + L_{\rm pr,max} +$ 1 taps per pre-equalization filter, and $h_{\rm FB}^{(r,q)}(m) = 0$ for $m \notin [1, L_{\rm FB}]$, yielding $L_{\rm FB}$ taps per feedback filter. In order to enable convenient matrix notation, we introduce the $(LL_{\rm pr}) \times L$ block matrix $\overline{\mathbf{H}}_{\rm pr}$ comprising all preequalizer coefficients:

$$\overline{\mathbf{H}}_{\mathrm{pr}} = \begin{bmatrix} \mathbf{\breve{H}}_{\mathrm{pr}}(-L_{\mathrm{pr,min}}) \\ \vdots \\ \mathbf{\breve{H}}_{\mathrm{pr}}(L_{\mathrm{pr,max}}) \end{bmatrix}, \quad (5)$$

where the (l, q)-th entry of the $L \times L$ matrix $\check{\mathbf{H}}_{\mathrm{pr}}(m)$ is given by $h_{\mathrm{pr}}^{(l,q)}(m)$. Similarly, the (l, q)-th entry of the $L \times L$ matrix $\check{\mathbf{H}}_{\mathrm{FB}}(m)$ is given by $h_{\mathrm{FB}}^{(l,q)}(m)$, with $m = 1, \ldots, L_{\mathrm{FB}}$. The samples $\{g^{(q,p)}(m)\}$ are included in the $L \times (LL_{\mathrm{pr}})$ block matrix $\overline{\mathbf{G}}(m)$ as follows

$$\overline{\mathbf{G}}(m) = \begin{bmatrix} \mathbf{\breve{G}} (mN_{\rm pr} + L_{\rm pr,min})^{\rm T} \\ \vdots \\ \mathbf{\breve{G}} (mN_{\rm pr} - L_{\rm pr,max})^{\rm T} \end{bmatrix}^{\rm T}, \quad (6)$$

where the (q, p)-th entry of the $L \times L$ matrix $\mathbf{\check{G}}(m)$ is given by $g^{(q,p)}(m)$. The sequences $\{g^{(q,p)}(m)\}$ are assumed to have limited time duration, i.e., $g^{(q,p)}(m) =$ 0 for $m \notin [-L_{g,\min}, L_{g,\max}]$, such that the number of non-zero matrices $\overline{\mathbf{G}}(m)$ is limited to the interval $[-L_{G,\min}, L_{G,\max}]$, where

$$\begin{cases} L_{\rm G,min} = \left\lfloor \frac{L_{g,\min} + L_{\rm pr,min}}{N_{\rm pr}} \right\rfloor \\ L_{\rm G,max} = \left\lfloor \frac{L_{g,\max} + L_{\rm pr,max}}{N_{\rm pr}} \right\rfloor , \tag{7}$$

with $\lfloor x \rfloor$ denoting the floor function. By introducing the *L*-dimensional column vectors $\mathbf{n}(k)$ and $\mathbf{u}(k)$, the *l*-th elements of which are given by $n^{(l)}(k)$ and $u^{(l)}(k)$, respectively, the vector of decision variables $\mathbf{u}(k)$ can be written as

$$\mathbf{u}(k) = \frac{1}{\alpha} \left[\sum_{m \in \Psi_{\mathrm{G}}} \mathbf{H}(m) \, \mathbf{a}(k-m) + \mathbf{n}(k) - \sum_{m \in \Psi_{\mathrm{FB}}} \breve{\mathbf{H}}_{\mathrm{FB}}(m) \, \mathbf{a}(k-m) \right], \quad (8)$$

where $\Psi_{\rm G} = [-L_{\rm G,min}, L_{\rm G,max}]$, $\Psi_{\rm FB} = [1, L_{\rm FB}]$, and

$$\mathbf{H}(\mathbf{m}) = \overline{\mathbf{G}}(m)\overline{\mathbf{H}}_{\mathrm{pr}}.$$
(9)

Taking (8) and (9) into account, the error vector $\mathbf{e}(k) = \mathbf{u}(k) - \mathbf{a}(k)$ between the actual output $\mathbf{u}(k)$ and the target output $\mathbf{a}(k)$ can be written as

$$\mathbf{e}(k) = \frac{1}{\alpha} \left[\sum_{m \in \Psi_{\mathrm{FB}}} \left(\mathbf{H}(m) - \breve{\mathbf{H}}_{\mathrm{FB}}(m) \right) \mathbf{a}(k-m) + \mathbf{n}(k) + \sum_{m \in \Psi_{\mathrm{Pr}}} \left(\mathbf{H}(m) - \alpha \delta_m \mathbf{I}_L \right) \mathbf{a}(k-m) \right],$$
(10)

where $\Psi_{\rm pr} = \Psi_{\rm G} \setminus \Psi_{\rm FB}$. As a performance measure for the proposed equalization scheme, we introduce the normalized mean square error (MSE) caused by noise, ISI, and XT:

$$MSE \triangleq \frac{E\left[\|\mathbf{e}(k)\|^2\right]}{E\left[\|\mathbf{a}(k)\|^2\right]}.$$
(11)

The equalization filters are selected so as to minimize the MSE under the restriction that the average transmit energy per symbol interval is limited to LE_s , i.e.,

$$E\left[\int_{-\infty}^{+\infty} \left|\sum_{q=1}^{L} s_k^{(q)}(t)\right|^2 dt\right] = LE_{\rm s}.$$
 (12)

It is readily verified that (2) and (12) yield the following energy constraint:

$$\sigma_a^2 \operatorname{tr}\left(\overline{\mathbf{H}}_{\mathrm{pr}}^{\mathrm{T}} \mathbf{G}_{\mathrm{tr}} \overline{\mathbf{H}}_{\mathrm{pr}}\right) = L E_{\mathrm{s}},\tag{13}$$

where the elements of the $(LL_{\rm pr}) \times (LL_{\rm pr})$ matrix $\mathbf{G}_{\rm tr}$ are given by

$$(\mathbf{G}_{\rm tr})_{n_1,n_2} = \int_{-\infty}^{+\infty} h_{\rm tr}(t) h_{\rm tr}(t + (n_1 - n_2) T_{\rm pr}) dt.$$
(14)

Taking (10) into account and using Lagrange multipliers to obtain the equalization filters that minimize the MSE (11) under the energy constraint (13), the Lagrangian is given by

$$\Lambda = \frac{1}{L\sigma_a^2 \alpha^2} \left[\sigma_a^2 \sum_{m \in \Psi_{\rm FB}} \left\| \overline{\mathbf{G}}(m) \overline{\mathbf{H}}_{\rm pr} - \breve{\mathbf{H}}_{\rm FB}(m) \right\|^2 + \sigma_a^2 \sum_{m \in \Psi_{\rm pr}} \left\| \overline{\mathbf{G}}(m) \overline{\mathbf{H}}_{\rm pr} - \alpha \delta_m \mathbf{I}_L \right\|^2 + \operatorname{tr}(\mathbf{R}_n) \right] + \lambda \left(\sigma_a^2 \operatorname{tr}\left(\overline{\mathbf{H}}_{\rm pr}^{\rm T} \mathbf{G}_{\rm tr} \overline{\mathbf{H}}_{\rm pr} \right) - LE_{\rm s} \right),$$
(15)

where λ is the Lagrange multiplier and the $L \times L$ autocorrelation matrix $\mathbf{R_n}$ is defined as

$$\mathbf{R}_{\mathbf{n}} \triangleq E\left[\overline{\mathbf{n}}(k)\,\overline{\mathbf{n}}(k)^{\mathrm{T}}\right].\tag{16}$$

Obviously, for any given pre-equalization matrix $\overline{\mathbf{H}}_{\mathrm{pr}}$, the Lagrangian (15) is minimized by selecting the feedback filters for $m \in \Psi_{\mathrm{FB}}$ as

$$\mathbf{\check{H}}_{\mathrm{FB}}(m) = \overline{\mathbf{G}}(m)\overline{\mathbf{H}}_{\mathrm{pr}}.$$
(17)

From (17) it follows that minimizing (15) with respect to the pre-equalization matrix $\overline{\mathbf{H}}_{\mathrm{pr}}$ results in the following MMSE pre-equalizer:

$$\overline{\mathbf{H}}_{\mathrm{pr,MMSE}} = \alpha \mathbf{A}^{-1} \overline{\mathbf{G}}(0)^{\mathrm{T}}, \qquad (18)$$

where

$$\mathbf{A} \triangleq \sum_{m \in \Psi_{\mathrm{pr}}} \overline{\mathbf{G}}(m)^{\mathrm{T}} \overline{\mathbf{G}}(m) + \lambda \mathbf{G}_{\mathrm{tr}}.$$
 (19)

Finally, the optimal values for λ and α can be obtained from the energy constraint (13) and the derivative of the Lagrangian (15) with respect to α , which yields

$$\lambda = \frac{\operatorname{tr}\left(\overline{\mathbf{H}}_{\operatorname{pr}}^{\mathrm{T}}\mathbf{G}_{\operatorname{tr}}\overline{\mathbf{H}}_{\operatorname{pr}}\right)}{LE_{\mathrm{s}}}$$
(20)

and

6

$$\alpha = \sqrt{\frac{\sigma_a^2}{LE_s}} \operatorname{tr}\left(\overline{\mathbf{G}}(0)\mathbf{A}\mathbf{G}_{\mathrm{tr}}\mathbf{A}^{-1}\overline{\mathbf{G}}(0)^{\mathrm{T}}\right).$$
(21)

IV. NUMERICAL RESULTS

In this section, the performance of the proposed MMSE MIMO pre-equalization scheme with DFE at the receiver is illustrated on a 4×4 MIMO channel with strong XT, obtained from simulating an electrical chipto-chip interconnect consisting of 4 adjacent stripline traces or lanes on a multilayer PCB. The transmit filters are assumed to generate unit-energy rectangular pulses

with length T whereas the receiver filters are unit-energy square-root raised-cosine filters with a 3 dB bandwidth of 1/(2T) and a roll-off factor $\beta = 0.3$. Furthermore, we use a 2-PAM constellation and assume that the noise samples $n^{(l)}(k)$ are spatially and temporally independent real-valued zero-mean Gaussian random variables with variance $N_0/2$:

$$E\left[n^{(p_1)}(k_1) n^{(p_2)}(k_2)\right] = N_0/2 \,\delta_{p_1-p_2} \delta_{k_1-k_2}.$$

When the sampling phase $\varepsilon = 0$, it is assumed that the impulse response corresponding to the frequency response $H_{\rm tr}(f)H_{\rm ch}^{(1,1)}(f)H_{\rm rec}(f)$ is sampled at the instant it reaches its maximum value. Since the filter coefficients can be computed offline, the complexity of the proposed equalization systems is mainly determined by the discrete-time filter operations. Hence, the total number of filter taps can be considered a valid complexity measure for both MIMO and SISO equalization systems.

Assuming $E_{\rm s}/N_0 = 20 \,\mathrm{dB}$ and a bit rate of $R_{\rm b} = 30$ Gbit/s per lane, we display in Fig. 2 the 1/MSE curves as a function of the sampling phase ε for several equalization schemes, for $N_{\rm pr} = 1$ and $N_{\rm pr} = 2$. We consider both the proposed pre-equalization scheme combined with DFE at the receiver side as well as a linear preequalization scheme without DFE ($L_{\rm FB} = 0$). In addition, we show the MSE performance resulting from the linear MIMO post-equalization scheme at the receiver (Rx) side from [10] and the DFE scheme at the receiver side from [11]; in the latter two schemes, upsampling at the transmitter $(N_{\rm pr} = 2)$ is replaced by oversampling at the receiver $(N_{po} = 2)$. It is observed from Fig. 2a that moving the feedforward filters from the receiver to the transmitter side does not affect the MSE performance of the linear and DFE MIMO equalization schemes when $N_{\rm pr}=1$. However, when $N_{\rm pr}=2$, Fig. 2b shows that the MIMO pre-equalization schemes slightly outperform the MIMO post-equalization schemes. It also follows from Fig. 2a that the proposed MIMO DFE scheme with $L_{\rm pr}=7$ (i.e., $L_{\rm pr,min}=L_{\rm pr,max}=3$) and $L_{\rm FB} = 4$ achieves a performance improvement of about 1 dB as compared to an equivalent SISO DFE scheme with $L_{\rm pr} = 7$ and $L_{\rm FB} = 0$, at the cost of increased complexity. However, even by increasing the number of filter taps of the SISO DFE scheme ($L_{\rm pr} = 28$, $L_{\rm FB} = 16$) such that both schemes have the same total number of filter taps, the SISO DFE scheme cannot compete with the MIMO DFE scheme. Furthermore,







Figure 2: MSE for SISO and MIMO equalization schemes with and without DFE ($R_{\rm b} = 30$ Gbit/s).

note that the equalization schemes with DFE are less susceptible to variations of the sampling phase ε than the linear schemes. From Fig. 2b, it follows that upsampling at the transmitter with a factor $N_{\rm pr} = 2$ improves the MSE performance for both the linear and the DFE schemes and further reduces the dependency of the MSE on the sampling phase. For the MIMO DFE scheme, the performance gain due to upsampling amounts to about 1 dB. However, the difference in MSE performance as compared to the other equalization schemes becomes much smaller than when $N_{\rm pr} = 1$.

In Fig. 3, we show the MSE performance of the equalization schemes from Fig. 2 for a bit rate of $R_{\rm b} = 60$ Gbit/s. It is readily observed that increasing the bit rate deteriorates the MSE performance for all

Figure 3: MSE for SISO and MIMO equalization schemes with and without DFE ($R_{\rm b} = 60$ Gbit/s).

equalization schemes. However, for the MIMO DFE scheme, the degradation is limited to about 3 dB for both $N_{\rm pr} = 1$ and $N_{\rm pr} = 2$, whereas it is much larger for the linear schemes and the SISO DFE schemes. For instance, when $N_{\rm pr} = 1$, the MIMO DFE schemes outperform the SISO DFE schemes by about 3 dB and the linear MIMO schemes by about 5 dB; when $N_{\rm pr} = 2$, the MIMO DFE schemes outperform their SISO DFE counterparts and the linear MIMO equalization scheme at the receiver side by more than 3 dB, whereas the difference with the linear MIMO pre-equalization scheme amounts to more than 4 dB. Hence, MIMO pre-equalization with DFE at the receiver side is clearly shown to be a promising technique to help facilitate future high-speed communication over low-cost electrical interconnects.



Figure 4: MSE for SISO and MIMO pre-equalization schemes with DFE at the receiver.

In Fig. 4, we show the BER versus E_s/N_0 for the SISO and MIMO pre-equalization schemes with DFE from Figs. 2 and 3. The BER values are anlytically obtained by averaging the conditional BER over the 10 highest-energy ISI terms and treating the remaining ISI as additive white Gaussian noise (AWGN). Note that we consider the SISO DFE scheme with $L_{\rm pr}=28$ such that all schemes have the same complexity in terms of total number of filter taps. For each scheme and for each value of $E_{\rm s}/N_0$, we obtain the optimal sampling phase from the corresponding 1/MSE curves before computing the BER. Considering a target BER of 10^{-12} , MIMO DFE outperforms SISO DFE by more than 1 dB at a bit rate of $R_{\rm b} = 30$ Gbit/s for both $N_{\rm pr} = 1$ and $N_{\rm pr} = 2$. In line with the results from Fig. 2, upsampling by a factor 2 clearly results in an improvement of the BER. At a bit rate of $R_{\rm b} = 60$ Gbit/s, the SISO DFE schemes do not achieve the target BER due to an error floor, whereas the MIMO pre-equalization schemes with DFE still perform very well. At the target BER, the degradation of the MIMO DFE scheme with $N_{\rm pr} = 2$ is limited to about 4.5 dB when doubling the bit rate from 30 Gbit/s to 60 Gbit/s per lane.

V. CONCLUSIONS

In this contribution, we derived elegant closed-form expressions for the FIR filters of an MMSE MIMO equalization scheme using linear pre-equalization at the transmitter and DFE at the receiver. We demonstrated how the proposed MIMO equalization scheme greatly outperforms its SISO counterpart, even given a total number of filter taps, when high bit rates are targeted. Therefore, the proposed scheme can be considered a promising technique to help facilitate future high-speed communication over low-cost electrical interconnects.

VI. ACKNOWLEDGEMENTS

Part of this research has been funded by the Interuniversity Attraction Poles Programme initiated by the Belgian Science Policy Office.

REFERENCES

- M. Kossel, T. Toifl, P. Francese, M. Brandli, C. Menolfi, P. Buchmann, L. Kull, T. Andersen, and T. Morf, "A 10 Gb/s 8-Tap 6b 2-PAM/4-PAM Tomlinson-Harashima Precoding Transmitter for Future Memory-Link Applications in 22-nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3268–3284, Dec. 2013.
- [2] H. Kimura, P. Aziz, T. Jing, A. Sinha, S. Kotagiri, R. Narayan, H. Gao, P. Jing, G. Hom, A. Liang, E. Zhang, A. Kadkol, R. Kothari, G. Chan, Y. Sun, B. Ge, J. Zeng, K. Ling, M. Wang, A. Malipatil, L. Li, C. Abel, and F. Zhong, "A 28 Gb/s 560 mW Multi-Standard SerDes With Single-Stage Analog Front-End and 14-Tap Decision Feedback Equalizer in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3091–3103, Dec 2014.
- [3] J. Bulzacchelli, T. Beukema, D. Storaska, P. Hsieh, S. Rylov, D. Furrer, D. Gardellini, A. Prati, C. Menolfi, D. Hanson, J. Hertle, T. Morf, V. Sharma, R. Kelkar, H. Ainspan, W. Kelly, G. Ritter, J. Garlett, R. Callan, T. Toifl, and D. Friedman, "A 28Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32nm SOI CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers (ISSCC)*, Feb 2012, pp. 324–326.
- [4] M. Nazari and A. Emami-Neyestanak, "A 15-Gb/s 0.5-mW/Gbps Two-Tap DFE Receiver With Far-End Crosstalk Cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2420–2432, Oct. 2012.
- [5] K.-D. Hwang and L.-S. Kim, "A 6.5-Gb/s 1-mW/Gb/s/CH Simple Capacitive Crosstalk Compensator in a 130-nm Process," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 60, no. 6, pp. 302–306, June 2013.
- [6] P. Amleshi and C. Gao, "NEXT and FEXT characteristics and suppressions in dense 25Gbps+ backplane vias," in *IEEE Int. Symp. on Electromagnetic Compatibility (EMC)*, Aug 2014, pp. 979–985.
- [7] D. Shilpa and B. Uma, "A wavelet technique to minimize offchip interconnect crosstalk," in *Int. Conf. on Emerging Trends in Communication, Control, Signal Processing Computing Applications (C2SPCA)*, Oct 2013, pp. 1–5.
- [8] T. Oh and R. Harjani, "A 12-Gb/s Multichannel I/O Using MIMO Crosstalk Cancellation and Signal Reutilization in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1383–1397, Jun. 2013.
- [9] J. Chen, Y. Gu, and K. Parhi, "Novel FEXT Cancellation and Equalization for High Speed Ethernet Transmission," *IEEE Trans. Circuits Syst.*, vol. 56, no. 6, pp. 1272–1285, June 2009.
- [10] L. Jacobs, M. Guenach, and M. Moeneclaey, "Linear MIMO equalization for high-speed chip-to-chip communication," in *Proc. IEEE Int. Conf. Commun. (ICC)*, 8-12 Jun. 2015.
- [11] —, "Application of MIMO DF equalization to high-speed offchip communication," in *Proc. IEEE Region 8 Int. Conf. on Computer as a Tool (EUROCON)*, 8-11 Sep. 2015.