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References

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In this letter, an improved bang-bang phase detector (PD) for multi Gb/s clock and data recovery (CDR) circuits is presented. The proposed PD is based on inverting the Alexander PD. In a typical subsampled CDR circuit, this Inverse Alexander PD results in a 10 times better bit error rate (BER) compared to the conventional Alexander PD. Additionally, in the case of duty-cycle distorted input data, this Inverse Alexander PD can even reach 20 times better BER compared to the conventional Alexander PD.

Introduction: Clock and data recovery (CDR) circuits are key building blocks in all high speed serial communication systems. This makes the performance of the CDR crucial to ensure the reliability of the entire communication system [1]. An important aspect to take into account in the design of a CDR is duty-cycle distortion (DCD) of the received data, because it degrades the performance. This duty-cycle distortion is caused by non-ideal driver and receiver characteristics [2].

The block diagram of a generic CDR circuit is shown in Fig. 1. The purpose of the bang-bang (BB) phase detector (PD) is to determine the phase error between the incoming data (D_{in}) and the recovered clock (Clk) signal. The BBPD only outputs whether the clock is leading or lagging the data signal. The corresponding 'Early' and 'Late' signals are sent to the loop filter (LF), which adjusts the control signal of the voltage controlled oscillator (VCO) in order to reduce the phase error. If no data transition occurs, the BBPD does not generate any signal and the VCO is not adjusted.

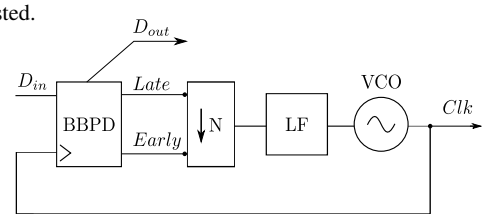


Fig. 1. A general bang-bang CDR circuit with subsampling.

Such BBPDs are typically used in high speed CDR circuits because they provide simplicity in design, good phase adjustment and can work at high speeds [3]. In recent years some new BBPD topologies have come up [4, 5]. However, either the complexity in these topologies is increased or the data retiming and the phase detection operation are not performed in the same circuit. The latter requires an explicit decision circuit and intrinsically introduces skew between both circuits. This is unfavorable for high speed data communication applications [6]. Therefore, the Alexander PD topology [7], including variations such as the half-rate, the quarter-rate, the multilevel, and the majority-voting variant, is the most commonly used PD in high speed designs with data rates larger than 10 Gb/s.

Furthermore, the high data rates make it inevitable to use subsampling in the bang-bang phase detector in order to alleviate the speed and hardware requirements [1]. This means that the BBPD will only generate an output signal once out of every N clock cycles. This is needed to reduce the speed in the LF and the circuitry driving it to a practical level. In Fig. 1, the subsampling is modeled by the decimation block N.

This letter introduces an Inverse Alexander phase detector. The BER performance of this improved PD is compared with the conventional Alexander PD for multiple cases of duty-cycle distortion and subsampling factors. It is found that in a typical subsampled CDR system, the use of our newly proposed Inverse Alexander PD improves the BER 10 to 20 times compared to the conventional Alexander PD.

The Alexander PD: The block diagram of the Alexander PD is shown in Fig. 2. Utilizing three data samples taken by three consecutive clock edges, the PD can determine whether a data transition is present and whether the clock leads or lags the data. The CDR with an Alexander PD will try to align the falling edge of the clock signal with an edge of the data, resulting in a 0.5 unit interval (UI) phase difference $\Delta\phi$ between the data and the clock. This is illustrated by Fig. 3(a). If the falling edge of the clock leads (is 'Early'), the last sample, S_3, is unequal to the first two and the clock frequency must be decreased (Fig. 3(b)). Vice versa, if the

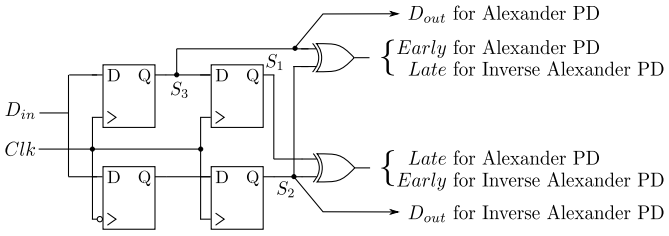


Fig. 2. The conventional Alexander PD and Inverse Alexander PD.

falling edge of the clock lags (is 'Late'), the first sample, S_1 is unequal to the last two and the clock frequency must be increased (Fig. 3(c)). In absence of data transitions, all three samples are equal and no action is taken. These relations are summarized by [6]:

$$\text{Early}: S_1 \oplus S_2 = 0, \quad S_2 \oplus S_3 = 1 \quad \rightarrow \quad \text{Clk frequency} \downarrow \tag{1}$$

$$\text{Late}: S_1 \oplus S_2 = 1, \quad S_2 \oplus S_3 = 0 \quad \rightarrow \quad \text{Clk frequency} \uparrow \tag{2}$$

$$\text{Others}: S_1 \oplus S_2 = S_2 \oplus S_3 \quad \rightarrow \quad \text{Do not adjust clk} \tag{3}$$

Note that the definition used here for 'Early/Late' is similar to [6] and different from [7], because the definition of 'Early/Late' and the corresponding frequency adjustment is more intuitive in [6].

Fig. 3(a) shows that once the CDR has settled, either the first or last sample, S_1 or S_3 can correspond with the data output D_{out} while the other sample moment S_2 occurs at the transition of the data.

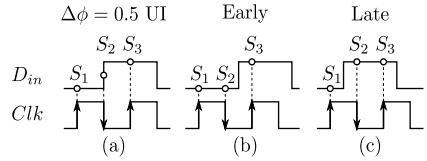


Fig. 3 *Waveforms for the locking behavior of the Alexander PD: (a) Ideal locking condition with phase difference $\Delta\phi = 0.5$ UI; (b) 'Early' condition; (c) 'Late' condition.*

The Inverse Alexander PD: The proposed PD is also shown in Fig. 2. It has the same schematic as the Alexander PD, however the 'Early/Late' signal is inverted:

$$\text{Early}: S_1 \oplus S_2 = 1, \quad S_2 \oplus S_3 = 0 \quad \rightarrow \quad \text{Clk frequency} \downarrow \tag{4}$$

$$\text{Late}: S_1 \oplus S_2 = 0, \quad S_2 \oplus S_3 = 1 \quad \rightarrow \quad \text{Clk frequency} \uparrow \tag{5}$$

$$\text{Others}: S_1 \oplus S_2 = S_2 \oplus S_3 \quad \rightarrow \quad \text{Do not adjust clk} \tag{6}$$

The inversion of the sign of the CDR loop causes the CDR to settle at a different operating point. As shown in Fig. 4(a), the Inverse Alexander PD will try to align the rising edge of the clock signal with an edge of the data. If the rising edge of the clock leads (is 'Early'), the first sample, S_1, is unequal to the last two and the clock frequency must be decreased (Fig. 4(b)). Vice versa, if the rising edge of the clock lags (is 'Late'), the last sample, S_3 is unequal to the first two and the clock frequency must be increased (Fig. 4(c)). In lock, the middle sample, S_2 now corresponds with the data sample D_{out} while the other sample moments S_1 and S_3 occur at the data transitions.

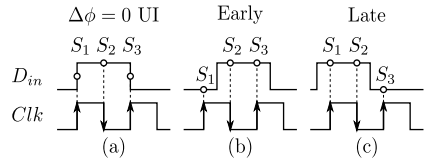


Fig. 4 *Waveforms for the locking behavior of the Inverse Alexander PD: (a) Ideal locking condition with phase difference $\Delta\phi = 0$ UI; (b) 'Early' condition; (c) 'Late' condition.*

Influence of duty-cycle distortion: Duty-cycle distortion (DCD) means that the duration of a logic-0 will be be different from the duration of a logic-1 [2]. The notations T_0 and T_1 are used to represent respectively the duration of an occurrence of a single logic-0 and a single logic-1 affected by DCD; where the sum of T_0 and T_1 always equals 2 UI. Note when T_1 equals 1 UI, there is no DCD and when $T_1 < 0.5$ UI, the DCD is too large to have any useful operation of the CDR. The dual case when $T_1 > T_0$, is analogue and is therefore covered by our discussion as well.

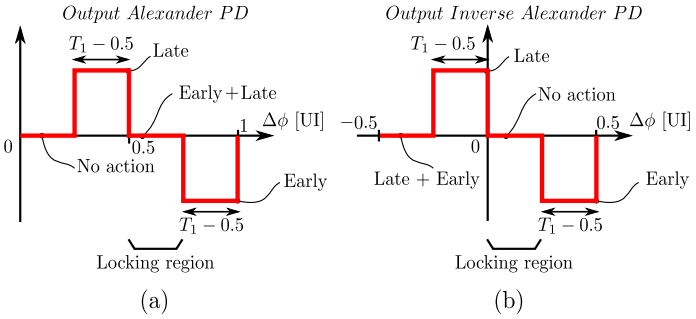


Fig. 5 *Output characteristic of the PDs without subsampling:* ***(a)*** *the Alexander PD; and* ***(b)*** *the Inverse Alexander PD.*

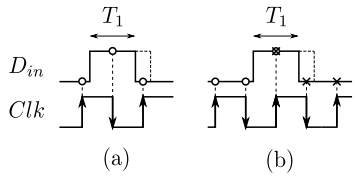
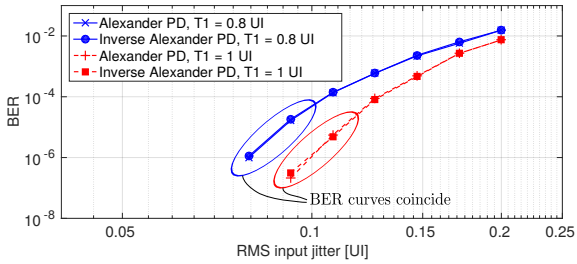


Fig. 6 *Waveforms of dead-zones:* ***(a)*** *'No action'-zone; and* ***(b)*** *'Early+late'-zone or 'Late+Early'-zone.*



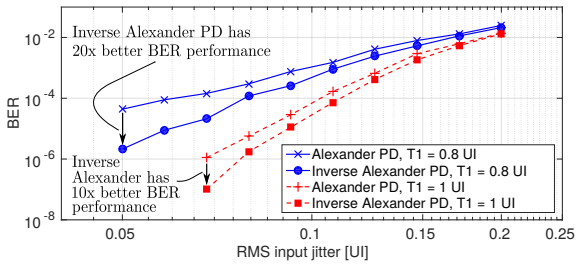


Fig. 7. BER performance: **(a)** No subsampling; **(b)** Subsample factor = 4.

To examine the influence of DCD, the output characteristics of both PDs are determined. This is calculated by sweeping the phase difference $\Delta\phi$ between a DCD data stream with a single logic-1 bit and the recovered clock. Therefore, the characteristics in Fig. 5 are derived for the case that two consecutive data transitions occur. Note that no subsampling is applied here. Fig. 5 illustrates that both output characteristics are the inverted versions of each other, and that next to the expected 'Early' and 'Late' zones, two new zones with zero output (dead-zones) are present. Due to the characteristic of the Alexander PD (Fig. 5(a)), the CDR loop will lock such that the phase difference $\Delta\phi$ lies between [0.5, 1.5-T_1] UI. This is also indicated on the figure as the 'Locking region' and contains the 'Early+Late'-zone. This is different from the locking region of the Inverse Alexander PD, as shown in Fig. 5(b), which is located between [0, 1-T_1] UI. This region corresponds with the 'No-action'-zone.

The two cases where a dead-zone can occur, are displayed in Fig. 6. In the 'No action'-zone, the first and last sample are equal and different from the middle sample. The PD outputs simultaneously a 'Late' and an 'Early' signal and therefore the frequency of the VCO will not change. In the 'Early+Late'-zone or the 'Late+Early'-zone, the PD outputs first an 'Early' and outputs the subsequent clock period a 'Late' signal or vice versa. Due to the loop filtering this results in a net zero action. This can be extended to the more general case where we have multiple consecutive identical bits: As long as the number of consecutive identical bits is limited due to bit scrambling and the loop filter has a low enough cut off frequency, the 'Early' signal generated at the first data transition will be canceled out by the 'Late' signal generated at the second data transition. This also results in a net zero action.

Performance: To study the performance, simulations were performed. A CDR with an Alexander PD is compared with a CDR containing an Inverse Alexander PD. For both CDRs the loop parameters are equal and the BER performance for different input jitter levels, DCD and subsample factors is discussed.

In the case that no subsampling is present in the system, we expect that the BER curves for both systems are equal, because the characteristics of both PDs (Fig. 5) are identical apart from the phase shift in $\Delta\phi$. Hence the system will react in a similar way and this results in the coincidence of the BER curves. This is confirmed by the simulations as shown in Fig. 7(a). Additionally, Fig. 7(a) illustrates that the BER becomes worse when the DCD increases. This is because the shorter logic-1 levels become more susceptible to jitter. As mentioned above, the cases for $T_1 = 0.8$ UI and $T_1 = 1.2$ UI are analogue and result in the same BER curves. These curves are omitted from the figures.

Fig. 7(b) illustrates the BER for a 4-times subsampled CDR. In this case the Inverse Alexander PD performs better than the Alexander PD. This is because subsampling causes the output characteristic of the PDs to change: especially the 'Early+Late'-zone which resulted in a net zero action when no subsampling was present. Due to the subsampling only one signal of the two subsequent 'Early' and 'Late' signals is sampled. In this way, the 'Early' and 'Late' signal will not cancel out rapidly as was the case without subsampling. This will undesirably lead to an adjustment of the frequency and cause fluctuations in the phase difference. For the Alexander PD this results in a worse BER, because its locking region is located in the 'Early+Late'-zone. For the Inverse Alexander PD, the BER will also degrade due to the lower update rate of the error signal. However, this degradation is less severe because the output characteristic in the locking region for the Inverse Alexander PD (i.e. 'No action'-zone) remains the same when subsampling is applied. Fig. 7(b) shows that the inverse Alexander PD is consistently better than the conventional Alexander PD and the difference becomes more pronounced for high levels of DCD and/or low levels of jitter, e.g.: for a typical case with 0.05 UI RMS input jitter and a subsample factor of 4, the Inverse Alexander PD reaches a BER which is 20 times better than the BER for the Alexander PD.

Conclusion: In this letter, an improved BBPD was proposed by inverting the sign of the Alexander PD. We can conclude that with this minimal effort, the Inverse Alexander PD has all the advantages of an Alexander phase detector while improving the BER with a factor 10 to 20 in the typical situation that the CDR system uses subsampling in the PD.

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