

Flip-Chip Bonding of VCSELs to Silicon Grating Couplers via SU8 Prisms Fabricated using Laser Ablation

K.S.Kaur⁽¹⁾, A.Z.Subramanian^(2,3), R. Verplancke⁽¹⁾, P. Cardile⁽¹⁾, J. Van Kerrebrouck⁽⁴⁾, S. Spiga⁽⁵⁾,
R. Meyer⁽⁵⁾, J. Bauwelinck⁽⁴⁾, R. Baets^(2,3), G. Van Steenberge⁽¹⁾

⁽¹⁾ Centre for Microsystems Technology, imec/Ghent University, B-9052 Gent, Belgium
(Kaur.Kamalpreet@elis.ugent.be)

⁽²⁾ Photonics Research Group, INTEC Department, Ghent University-imec, Ghent 9000, Belgium

⁽³⁾ Centre for Nano- and Biophotonics, Ghent University, Ghent 9000, Belgium

⁽⁴⁾ Department of Information Technology, Ghent University-iMinds-imec, B-9000 Ghent, Belgium

⁽⁵⁾ Walter Schottky Institut, Technische Universität München, D-85748 Garching, Germany

Abstract *We successfully demonstrate for the first time, VCSEL-to-silicon grating coupler flip-chip assembly using SU8 prism fabricated by non-uniform laser ablation. Excess loss of < 1 dB and data transmission up to 20 Gb/s @ 1550 nm was achieved.*

Introduction

In silicon photonics, the use of grating couplers (GCs) is a standard solution to connect on-chip circuitry to the outside world. However, the conventional GC designs require off-normal (typically 8-10 degrees) coupling angle so as to avoid second order Bragg reflections. This off-normal incidence condition makes the integration of light sources especially vertical-cavity surface-emitting lasers (VCSELs) to silicon-on-insulator (SOI) chips a challenging task, as the back reflections not only lead to poor coupling efficiencies but are also detrimental for the VCSEL performance. Although complex designs of GCs adapted for perfect vertical coupling have been reported¹, they are hard to implement. Another approach could be to use the standard GCs and flip-chip bond the VCSELs on top at an angle but that again is a non-trivial and non-standard technology. An alternative solution to this problem is by incorporating micro-optical elements on top of GCs as reported in [2]. In this paper, fiber-to-fiber transmission was demonstrated using a polymer (SU8 and PAK) wedge fabricated using focused-ion-beam (FIB) and imprinting lithography on top of the GCs to translate the vertical incidence into an off-normal incidence. However, FIB is inherently a time-intensive, expensive and non-flexible process. Finally, as the polymer wedge is protruding out on the SOI chip² patterning the bonding pads and realizing VCSEL-to-SOI chip assembly using this approach can be quite challenging.

In order to circumvent the above mentioned issues, we present a laser-based, contactless and single-step process to fabricate polymer prisms on top of the GCs. It is a simple, fast, flexible and wafer-scalable process. In this paper, we demonstrate for the first time the

integration of VCSEL chips to silicon GCs using SU8 prisms. The VCSELs were flip-chipped onto the SOI chips employing the laser-induced forward transfer (LIFT) - assisted thermocompression bonding³. We describe in this paper the technological approach and the measurement of coupling efficiency. We also report on the high speed data transmission experiments performed on the bonded assemblies.

Flip-chip bonding of VCSEL to SOI

The waveguides and GCs used for the experiments were fabricated using deep UV lithography in a CMOS environment via ePIXfab⁴. The waveguides were completely etched and were 220 nm x 500 nm in dimensions. The GCs were shallow etched by 70 nm at the input and output end of the waveguide. The entire structure was cladded by SiO₂ on top for reduced losses.

The various steps involved in the process flow to realize the VCSEL to SOI assembly are depicted in Fig. 1. First of all the insertion loss of the SOI chips (GC-WG-GC) was measured prior to the prism fabrication to get the reference loss value. The GCs used for the experiments were designed for 10° operation in the C-band for TE polarization mode. For the measurements light from a tunable laser source was coupled into the input GC at an angle of 10° using a SMF (single mode fiber) and was collected after propagation in the SOI waveguide from the output GC using another SMF at an angle of 10°. A 25 μm thick blanket layer of SU8 was then spin coated on top of the SOI chip, followed by soft bake (1 min @ 65 deg, 10 min @ 95 deg), flood exposure (> 300 mJ/cm²) and hard bake (1hr @ 150 deg) steps to fully cure the SU8 layer. Next, the VCSEL bonding pads (Ti/Ni/Au) were defined on

top of the SU8 layer using image reversal lithography.

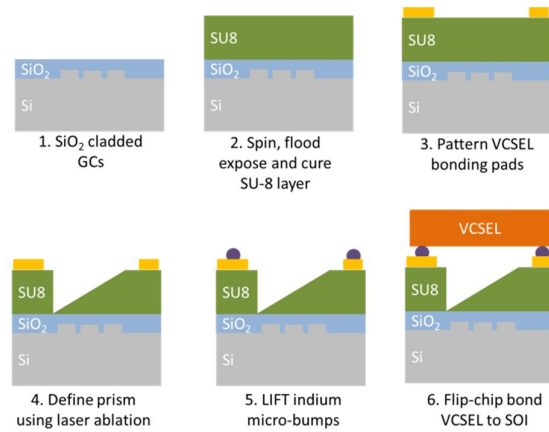


Fig. 1: Schematic depicting the process flow for VCSEL-to-SOI integration (not drawn to scale).

The next step was the fabrication of SU8 prisms with an angle of 24° on top of the GCs using non-uniform laser ablation⁵. The optimum value for the prism angle was calculated using Snell's law for a normal incidence on prism face such that it resulted into a 10° incidence angle onto the GCs. Laser pulses from an excimer laser (KrF, operating wavelength 248 nm, pulse duration 5-8 ns, pulse energy 570 μ J) were first passed through a triangular mask (1000 x 610 μ m) and a demagnified image (factor of 12) of the mask was projected onto the SU8 coated sample. The sample was then scanned in a direction perpendicular to the incoming laser beam at a speed of 157 μ m/s at 100 Hz repetition rate to ablate a ~ 22 μ m deep prism with 24° angle. The simplicity of this technique lies in the fact that the prism angle can be tuned just by adjusting the laser energy and sample scan speed. Micro-bumps of indium metal with ~ 20 μ m diameter and 7 μ m thickness were then printed on the bonding pads employing the LIFT technique. The details about this technique can be found in [3]. A Timebandwidth Duetto laser source (355 nm, 12 ps) and a transfer fluence of 300 mJ/cm² was used for the LIFT experiments. The final step in the assembly was to flip-chip bond the VCSEL chips onto the GCs with SU8 prism fabricated on top. The 1550 nm *n*-InP VCSELs used in these experiments were based upon a short-cavity design and had three compressively strained AlGaInAs quantum wells⁶. A semiautomatic flip-chip bonder from Tresky was used for thermocompression bonding of the VCSELs to the SOI chips. A mechanical and electrical interconnection between the VCSEL and the SOI chip was established via molten indium bumps³.

Characterization of the bonded assembly

The samples were measured after each processing step (1-6 in Fig. 1) to evaluate the excess loss (if any) introduced by the processing to ensure an optimum coupling efficiency from the GCs. The loss values measured at various stages are listed in Tab. 1. Prior to VCSEL bonding fiber to fiber transmission measurements were performed. Till step 3 both the input and output fibers were tilted at 10° angle from the normal to GC, while from step 4 onwards, the input fiber was positioned along the normal (0°) and the prism refracted the incident light to an optimum 10° onto the GCs. No significant shift in the GC efficiency was recorded at any stage of process flow indicating there was no excess loss due to any step and the process was optimum. The fiber transmission curves recorded before and after prism fabrication for one of the samples is shown in Fig. 2.

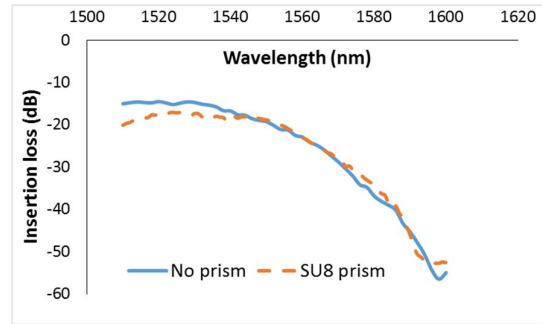


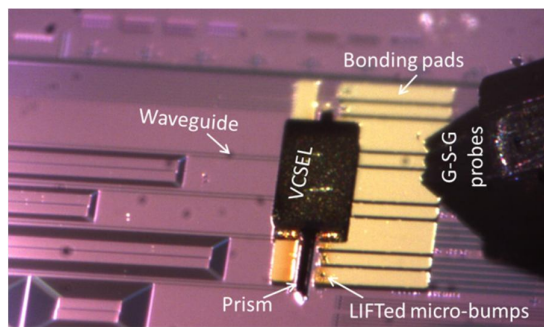
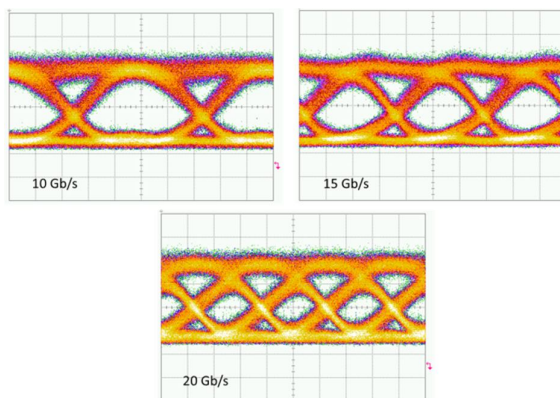
Fig. 2: Transmission curves recorded before and after prism fabrication onto GCs.

A typical bonded assembly comprising of bonding pads, prism, SOI and VCSEL is shown in Fig. 3. Before bonding, the VCSEL chips were characterized and they typically emitted -4 dBm @ 5 mA. For the DC measurements a driving current of 5 mA was applied to the bonded VCSELs. The emitted power was coupled into the SOI waveguide via SU8 prism and GC combination. After propagating in the waveguide the power was collected at the output GC by a SMF at 10° and was recorded by a power meter. Few devices were tested and for the best case the transmitted power collected at the output was up to -21.7 dBm @ 1547 nm (peak wavelength of VCSEL) for a driving current of 5 mA. This resulted in a total excess loss of < 1 dB introduced by the whole assembly process as shown in Tab. 1. The main contributing factor for the excess loss is attributed to the misalignment during bonding as the flip-chip process involved passive alignment of the VCSEL and SOI chip.

Tab. 1: Loss values measured at various stages of the VCSEL-to-SOI integration process.

Sample ID	Fiber-to-waveguide coupling efficiency without prism (10°, 1550 nm) (dB)	Fiber-to-waveguide coupling efficiency with prism (0°, 1550 nm) (dB)	VCSEL-to-waveguide coupling efficiency (@ 5 mA) (dB)	Total excess loss (prism+bonding) (dB)
S1	-18.5	-19	-20	-1.5
S2	-17	-17.5	-17.7	-0.7

To further check the reliability and the performance of the process, non-return-to-zero (NRZ) transmission experiments till 20 Gb/s were performed on the bonded assemblies by direct modulation of the VCSELS. Clear and wide open eye patterns for 10 and 15 Gb/s were recorded representing an error free transmission as shown in Fig. 4. At 20 Gb/s, the bandwidth limitation of the set-up started to appear.

**Fig. 3:** Typical bonded assembly of VCSEL on top of SOI chip.**Fig. 4:** Eye diagrams recorded for the bonded VCSEL assemblies at 10, 15 and 20 Gb/s.

Conclusions

To conclude, flip-chip bonding of VCSEL chips to SOI GCs using SU8 prisms was successfully demonstrated in this paper. The step-by-step

process for the SU8 prism fabrication on top of GCs employing non-uniform laser ablation followed by LIFT assisted thermocompression flip-chip bonding of VCSEL chips was presented. An excess loss of < 1 dB @ 1550 nm was measured for the bonded assemblies. NRZ measurements showed clear open eyes recorded till 20 Gb/s for the bonded samples thereby confirming the suitability of this approach for high speed data transmissions. The simplicity, cost-effectiveness, flexibility and wafer scalability makes this method an attractive solution for VCSEL-to-SOI integration.

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