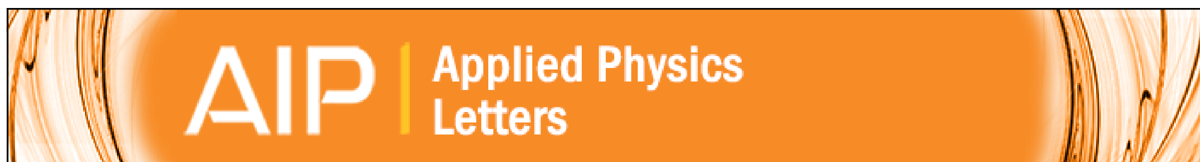

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Correlation of interface states/border traps and threshold voltage shift on AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors

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In this paper, three electrical techniques (frequency dependent conductance analysis, AC transconductance (AC-g_m), and positive gate bias stress) were used to evaluate three different gate dielectrics (Plasma-Enhanced Atomic Layer Deposition Si_3N_4, Rapid Thermal Chemical Vapor Deposition Si_3N_4, and Atomic Layer Deposition (ALD) Al_2O_3) for AlGaN/GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors. From these measurements, the interface state density (D_{it}), the amount of border traps, and the threshold voltage (V_{TH}) shift during a positive gate bias stress can be obtained. The results show that the V_{TH} shift during a positive gate bias stress is highly correlated to not only interface states but also border traps in the dielectric. A physical model is proposed describing that electrons can be trapped by both interface states and border traps. Therefore, in order to minimize the V_{TH} shift during a positive gate bias stress, the gate dielectric needs to have a lower interface state density and less border traps. However, the results also show that the commonly used frequency dependent conductance analysis technique to extract D_{it} needs to be cautiously used since the resulting value might be influenced by the border traps and, vice versa, i.e., the g_m dispersion commonly attributed to border traps might be influenced by interface states. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4930076]

Gallium Nitride (GaN) based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) are highly promising for power switching applications.[1] However, the threshold voltage (V_{TH}) instability of MIS-HEMTs remains a critical issue. Especially, V_{TH} hysteresis after a positive gate voltage sweep and V_{TH} shift during a positive bias gate stress[2–5] are important reliability challenges. Therefore, it is important to understand the origin of V_{TH} shift in order to provide technology solutions to minimize these instability issues. We can distinguish two main types of papers in literature. A first type focuses on the analysis of the V_{TH} drift during stress.[3–5] In contrast, a second type focuses on the characterization of the quality of the gate dielectrics in terms of interface states and border traps on the fresh devices[6–9] without discussing the implications on V_{TH} instability during operations. The link between these two type of analyses is still unclear. In this work, we compare three different gate dielectrics: Rapid Thermal Chemical Vapor Deposition (RTCVD) Si_3N_4, Atomic Layer Deposition (ALD) Al_2O_3, and Plasma-Enhanced Atomic Layer Deposition (PEALD) Si_3N_4, by means of (1) a conventional frequency dependent conductance analysis, (2) an AC transconductance (AC-g_m) technique, and (3) a study of the V_{TH} shift after a positive gate bias. By correlating the results of the electrical analyses, the physical mechanism behind the V_{TH} instability is proposed.

All wafers were fabricated with a Au-free CMOS-compatible process on 200 mm Czochralski-grown ⟨111⟩ Si wafers with a resistivity of 10 Ω·cm, starting with an AlN nucleation layer, a 2.3 μm AlGaN buffer, a 150 nm GaN channel, a 15 nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 3 nm GaN cap layer, which is used to avoid the oxidation of the AlGaN barrier. The epitaxy of the GaN cap/AlGaN/GaN stack was grown by means of metalorganic chemical vapor deposition (MOCVD) at a temperature of 1010 °C with Trimethylgallium (TMGa), trimethylaluminum (TMAl), and Ammonia as precursors for Ga, Al, and N, respectively. The 2DEG resistivity is approximately 450 Ω/sq. Atomic Layer Etching (ALE) process was used to recess the AlGaN barrier by means of cycles of oxidation and lower power BCl_3 etching. Unlike fully recessed gate Metal-Insulator-Semiconductor Field-Effect Transistors (MIS-FETs), where the channel is touching the gate dielectric, several device properties could be easily influenced by the proximity of the dielectric, e.g., electron mobility and subthreshold swing. The partial recessed gate structure focuses on trapping phenomena without these influences since the channel between AlGaN barrier and GaN buffer is not touching the gate dielectric. Therefore, this study was performed on recessed gate devices with 3.7 nm AlGaN barrier thickness remaining under the gate dielectric (Fig. 1) and with three different gate dielectrics: 15 nm PEALD Si_3N_4 deposited in an ASM system, 15 nm ALD Al_2O_3, and a 15 nm RTCVD Si_3N_4. PEALD Si_3N_4 film (N-rich) was deposited at 300 °C with SiH_4 and N_2 alternating cycles of SiH_4 and N_2 as precursors,[10]

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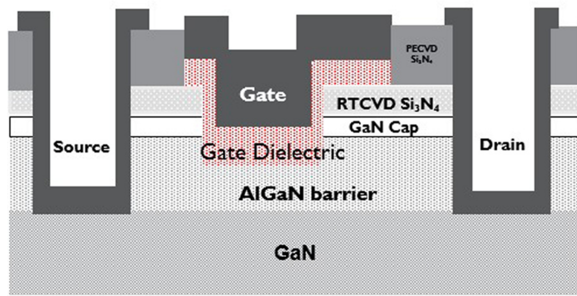

FIG. 1. Cross-section of a recessed gate AlGaN/GaN MIS-HEMT.

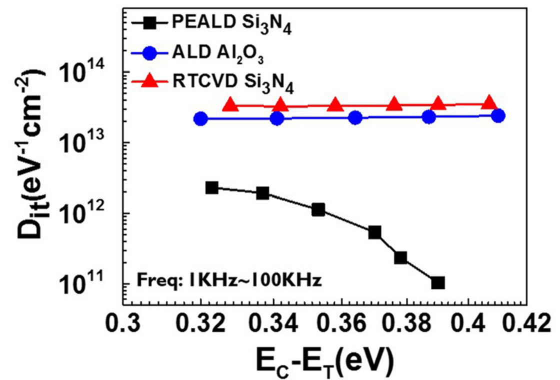

FIG. 4. D_{it} values extracted from the frequency dependent conductance technique for MIS-HEMTs with different gate dielectrics. The trap state energy was estimated based on the Shockley–Read–Hall statistical model with a capture cross-section of 1×10^{-15} cm^2.

RTCVD Si_3N_4 film (Si-rich) was deposited under 700 °C with SiH_4 and NH_3 as precursors, and ALD Al_2O_3 film was deposited at 300 °C with TMA and H_2O as precursors. The gate dielectric is annealed at 700 °C for 1 min in forming gas (10% H_2, 90% N_2). The CMOS compatible gate metal stack consists of 30/20/250 nm W/Ti/Al, and the ohmic metal stack used consists of 5/100/60 nm Ti/Al/TiN, resulting in a contact resistance of 0.65 Ω mm.[11]

Fig. 2 shows typical I_D-V_G characteristics of devices with the three different gate dielectrics. The different V_{TH} values are most probably due to the different fixed charges brought by different gate dielectrics.[12]

The frequency-dependent conductance technique was proposed by Nicollian and Goetzberger[13] and has been successfully applied to characterize the interface states for depletion-mode (D-mode) AlGaN/GaN MIS-HEMTs.[6,7] Considering the case in AlGaN/GaN MIS-HEMTs, a positive gate bias is needed to transfer the electrons from the channel to the interface between the AlGaN barrier and the gate dielectric where electrons might be trapped at interface states.

The following conditions were measured on the capacitor structures: $V_G = 2.4$ V–3.4 V (RTCVD Si_3N_4), $V_G = 2.6$–3.6 V (ALD Al_2O_3), and $V_G = 3$ V–4 V (PEALD Si_3N_4). The slightly different measuring conditions were chosen depending on $V_{G,spill\text{-}over}$ where the electrons start accumulating below the interface[3] as schematically shown in Fig. 3.

However, one of the most critical assumptions in this technique is that electrons only interact with the interface states without considering the influence of border traps in the gate dielectric.[13] Fig. 4 shows the extracted D_{it} values at the interface between the gate dielectric and the AlGaN barrier. The D_{it} is significantly lower for the device with a PEALD Si_3N_4 ($D_{it} \sim 1 \times 10^{11}$–$2.3 \times 10^{12}$ cm^{-2} eV^{-1}) gate dielectric than for the device with an ALD Al_2O_3 ($D_{it} \sim 2.2 \times 10^{13}$–$2.4 \times 10^{13}$ cm^{-2} eV^{-1}) or an RTCVD Si_3N_4 ($D_{it} \sim 3.3 \times 10^{13}$–$3.5 \times 10^{13}$ cm^{-2} eV^{-1}) gate dielectric. A recent publication[14] indicates that the conventional conductance measurement could underestimate the interface states value. For this reason, two additional electrical evaluations were used: AC-g_m dispersion[8,15] and the V_{TH} shift during a positive gate bias stress.

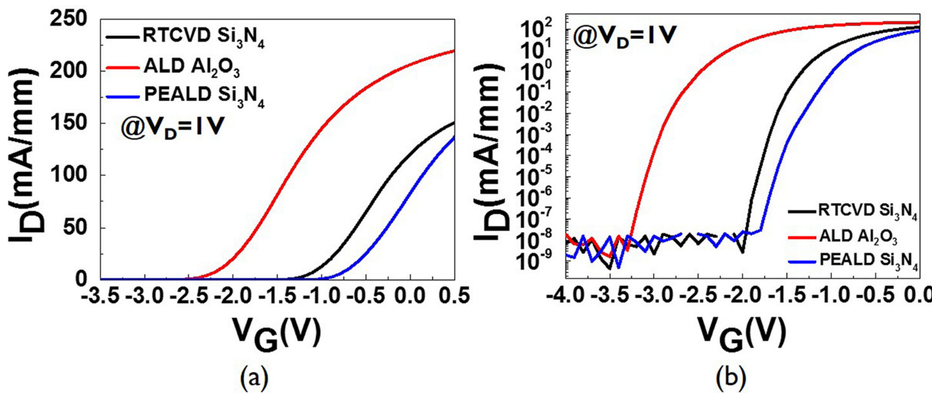

FIG. 2. I_D-V_G characteristics (linear-linear scale (a) and logarithmic-linear scale (b)) of devices with different gate dielectrics.

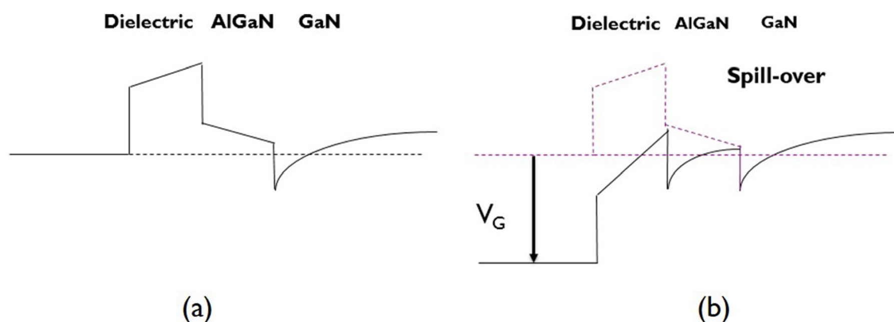

FIG. 3. Schematic band diagram of a GaN based MIS-HEMT in thermal equilibrium (a) and in the spill-over case where a second channel at the dielectric interface is generated (b).

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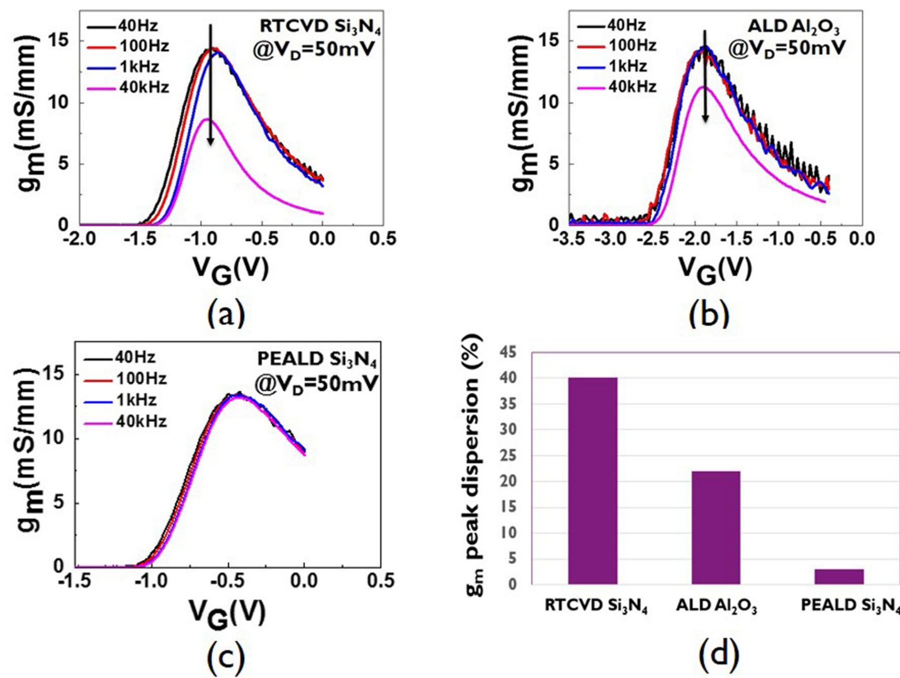

FIG. 5. The AC-g_m curves for RTCVD Si_3N_4 (a), ALD Al_2O_3 (b), and a PEALD Si_3N_4 (c) gate dielectric. Comparison of the peak AC-g_m frequency dispersion (d).

The AC transconductance (AC-g_m) technique was developed to examine the effect of border traps on the carrier transport, and it is assumed that the AC-g_m dispersion reflects the border trap density in the gate dielectric.[8,15] Significant g_m peak dispersion with respect to the different frequencies was observed, both for devices with RTCVD Si_3N_4 (Fig. 5(a)) and an ALD Al_2O_3 (Fig. 5(b)) gate dielectric. In contrast, significantly lower g_m peak dispersion was observed on the device with a PEALD Si_3N_4 gate dielectric as shown in Figs. 5(c) and 5(d). Consequently, based on the analysis from the conventional conductance method and AC-g_m dispersion, PEALD Si_3N_4 layer shows both a smaller D_{it} and less border traps compared to the other two gate dielectrics.

Analysis of the V_{TH} shift during a positive gate bias stress was the third technique we applied to compare the three different dielectrics. In order to avoid the pre-charge or discharge during each I_DV_G sweep, similar to Refs. 4 and 16, the I_DV_G was only measured up to the threshold voltage (V_{TH}) ($V_{meas} = V_{TH}$ shown in the inset of Fig. 6) value with respect to the fresh device with 1 ms delay after stress. The threshold voltage shift was estimated from the drain current degradation as shown in Fig. 6. A shift of the threshold voltage (ΔV_{TH}) was observed already for short stress time (2 s) for the devices with a RTCVD Si_3N_4 and a ALD Al_2O_3 gate dielectric. Again, the devices with a PEALD Si_3N_4 gate dielectric show the smallest V_{TH} shift.

Fig. 7 shows a summary of D_{it}, g_m peak dispersion and the V_{TH} shift. Note that the V_{TH} shift values were extrapolated after a 2 s stress as shown in Fig. 6. We observe a high correlation between D_{it}, g_m peak dispersion, and V_{TH} shift. This indicates that the V_{TH} shift is not only due to the interface states but also to the border traps inside the gate dielectric. As shown in Fig. 8, the conduction band of the AlGaN barrier is pulled down for a positive gate voltage. Hence, the electrons can be transferred from the channel to the interface between the gate dielectric and the AlGaN barrier, where they are trapped by interface states or border traps, leading to a V_{TH} shift. From this point of view, in order to minimize the V_{TH} shift, a good gate dielectric should both have a low interface state density and a low amount of border traps. However, it is important to note that (1) the frequency conductance technique was originally developed to characterize

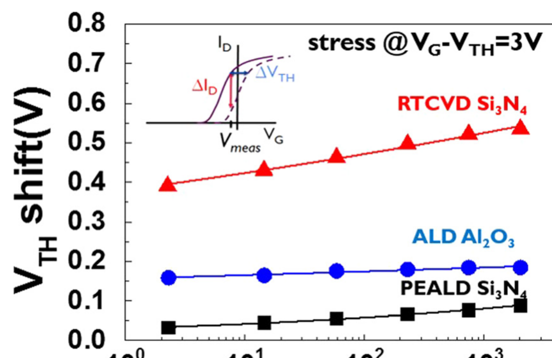

FIG. 6. V_{TH} shift vs stress time for devices with RTCVD Si_3N_4, ALD Al_2O_3, and PEALD Si_3N_4 as a gate dielectric.

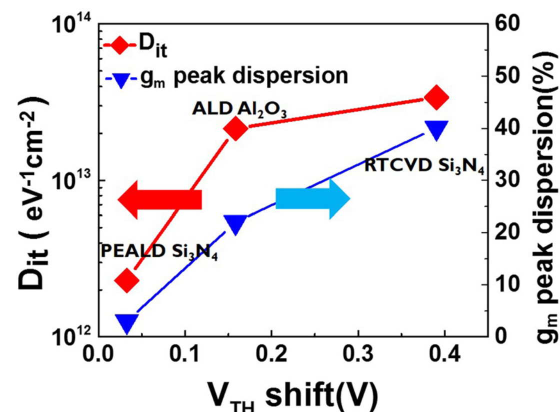

FIG. 7. D_{it} and g_m peak dispersion vs V_{TH} shift. The D_{it} values were extrapolated for E_C-$E_T \sim 0.32$ eV–0.33 eV as shown in Fig. 3. V_{TH} shift values were extrapolated after a 2 s stress shown in Fig. 6.

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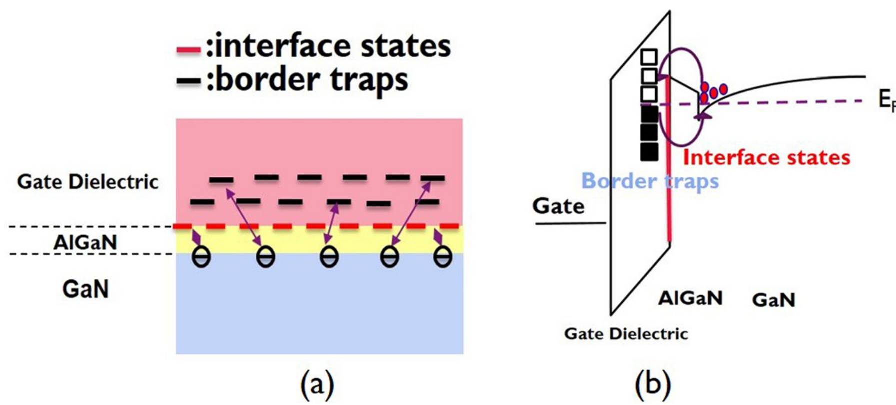

FIG. 8. Schematic of interface states and border traps in the a AlGaN/GaN MIS-HEMT (a) and band diagram (b).

interfaces with the physical assumption that the electrons only interact with the interface states,[13] and (2) the AC transconductance (AC-g_m) technique was originally used to examine the effect of border traps on the carrier transport without considering the impact from the interface states.[8] However, such a high correlation between D_{it}, g_m peak dispersion, and V_{TH} hysteresis suggests that the D_{it} values from typical conductance measurement could be influenced by border traps, especially since a high positive gate bias is needed (more than 2 V) to allow electrons to be injected across the AlGaN barrier and to interact with the gate dielectric interface in D-mode AlGaN/GaN MIS-HEMTs. On the other hand, the peak g_m dispersion could be affected by the interface states as well.

In this work, we used three different gate dielectrics to study the correlation between interface states, border traps, and V_{TH} shift during a positive gate bias stress. We conclude that the V_{TH} shift is highly related to the interface state density D_{it} and to the border traps, indicating that the electrons are trapped by both the interface states and the border traps. In order to minimize the V_{TH} instability in MIS-HEMTs, a gate dielectric with both a low D_{it} and a small amount of border traps is needed, e.g., PEALD Si_3N_4. We also showed that the frequency dependent conductance analysis and AC-g_m method need to be carefully used since the border traps influence the D_{it} measurement results and vice versa.

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