A 16 Channel High-Voltage Driver with 14 Bit Resolution for Driving Piezoelectric Actuators

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***Abstract*—A high-voltage, 16 channel driver with a maximum voltage of 72 volt and 14 bit resolution in a high-voltage CMOS (HV-CMOS) process is presented. This design incorporates a 14 bit monotonic by design DAC together with a high-voltage complementary class AB output stage for each channel. All 16 channels are used for driving a piezoelectric actuator within the control loop of a micropositioning system. Since the output voltages are static most of the time, a class AB amplifier is used, implementing voltage feedback to achieve 14 bit accuracy. The output driver consists of a push-pull stage with a built-in output current limitation and high-impedance mode. Also a protection circuit is added which limits the internal current when the output voltage saturates against the high-voltage rail. The 14 bit resolution of each channel is generated with a segmented resistor string DAC which assures monotonic by design behavior by using leapfrogging of the buffers used between segments. A diagonal shuffle layout is used for the resistor strings leading to cancellation of first order process gradients. The dense integration of 16 channels with high peak currents results in crosstalk, countered in this design by using staggered switching and re-sampling of the output voltages.**

***Index Terms*—High-voltage driver, piezoelectric actuators, HV-CMOS, monotonic by design, segmented DAC.**

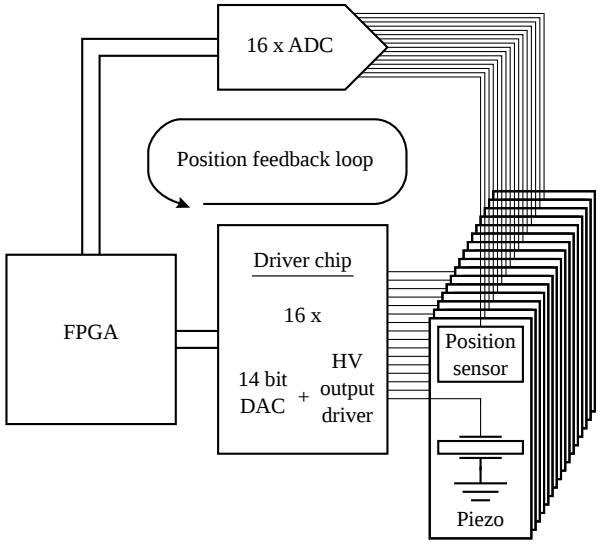

Fig. 1. Application of the designed 16 channel HV driver chip within a position feedback loop controlled by means of an FPGA.

I. Introduction

Piezoelectric actuators are being used in an increasing number of applications which require the combination of high precision together with minimal power consumption under static conditions [1]. More in particular multi-layered piezo actuators are widely applied for micropositioning in the fields of interferometry, microscopy, optical switches and wafer technology where a piezoelectric actuator is used for each spatial direction that needs to be steered [2]. When going to large systems where piezo arrays are implemented in multitude, an increasing amount of space and power consumption is needed for the high-voltage electronic drivers exposing the need for an integrated solution [3]. By using a modern CMOS process with HV-CMOS extensions, the integration of multiple high-voltage (HV) drivers and DACs onto one chip becomes feasible. This makes it possible to significantly decrease PCB area and optimize power consumption. In this work 16 HV drivers are implemented which each consist of a 14 bit DAC and a high-voltage class AB output stage. Although commercial examples can be found with a similar resolution and output voltage range, these have a maximum stable load capacitance ranging from 100 pF to 1 nF. This is perfect for driving MEMS arrays but insufficient for even the smallest piezoactuators used in micropositioning.

Piezoelectric actuators exhibit strong hysteresis nonlinearities [4], [5] which results in the need for a position feedback loop in applications requiring accurate positioning. The position of the designed driver chip within a possible implementation of such a feedback loop is shown in Fig. 1.

When combining several high-voltage drivers onto one chip, problems can arise concerning the power dissipation of individual drivers and the influence of the local heat generation on nearby drivers. This paper presents an output stage with a built-in current limitation which limits the power dissipation during switching and acts as a security measure in case of a shorted output. Main specification for the output driver consists of being able to drive the piezoactuator with an output voltage ranging from 0 V up to the high-voltage supply HV_{dd} - 1V with a minimum sourced and sunk current of 12mA during switching (allows a full-scale switch of a 1.5 μF load within 10ms).

Next to power dissipation, and the attributed heat dissipation, another issue with integrating several drivers and their respective DACs onto one chip is the level of inter-driver cross-

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TABLE I
STARTING SPECIFICATIONS FOR THE DAC AND HV OUTPUT STAGE.

Specifications HV driver	
Output voltage	0 V to HV_{dd} - 1V
Switching output current	$>$ 12 mA
Resolution	14 bit
INL	$<$ 32 LSBs
DNL	$>$ -1 LSB (monotonic)

talk. A possible solution to this issue which doesn't lead to an excessive increase in switching time is proposed in this article. With this technique, a chip integrating 16 output drivers, and potentially even more, becomes possible.

In a lot of piezoelectric actuator applications the most efficient option is to use a class D amplifier since this leads to powerful amplifiers with minimal levels of distortion [6], [7]. This is particularly the case for low power audio devices. For this application, which requires 14 bit of resolution, the minimum switching frequency is determined by the maximum allowed voltage ripple [8]. Due to the trade-off between switching frequency, voltage ripple and efficiency, a class D amplifier will results in a sub-optimal solution as will be shown later on. The high-voltage amplifier of choice for this application operates in class AB. A class B amplifier doesn't provide a higher efficiency in this case since a resistive feedback network is used which continuously needs current in case of a non-zero output voltage.

A high-voltage driver and a 14 bit monotonic by design DAC are implemented for each of the 16 channels. Due to the strong nonlinear hysteresis of piezoelectric actuators, the integral non-linearity (INL) of the DAC is allowed to be relative high (several tens of LSBs) without adding significantly to the overall non-linearity. However, since the driver is used within a larger position control loop, the DAC output needs to be monotonic by design to assure stable behavior of the system. Furthermore, integration of the DAC together with the output driver requires the DAC to cope with temperature gradients on the chip and at the same time achieve an accuracy of 14 bit with a limited INL.

The aim with this design was to achieve an as low as possible power consumption for the combination of DAC and HV output stage with the starting specifications given in Table I. Additional specifications which are of importance will be discussed further on in this paper.

II. DRIVER OVERVIEW AND CHIP TECHNOLOGY

The presented chip integrates 16 driver channels with each channel consisting of a 14 bit DAC followed by a class AB high-voltage output driver. In between the DAC and output driver a switching matrix is placed which allows to measure the DAC output and to apply a test signal at the input of the high-voltage output driver. The bits of the DACs and the direction of the testpin switching matrices is set by means of an SPI register. In this register there is also a bit per channel which determines whether a certain output is in high-impedance mode. The low-voltage and high-voltage part of each channel are powered by a 3.3 V and 72 V supply respectively while a 2.5 V reference signal is used for the 14 bit DACs. An overview of the chip can be seen in Fig. 2.

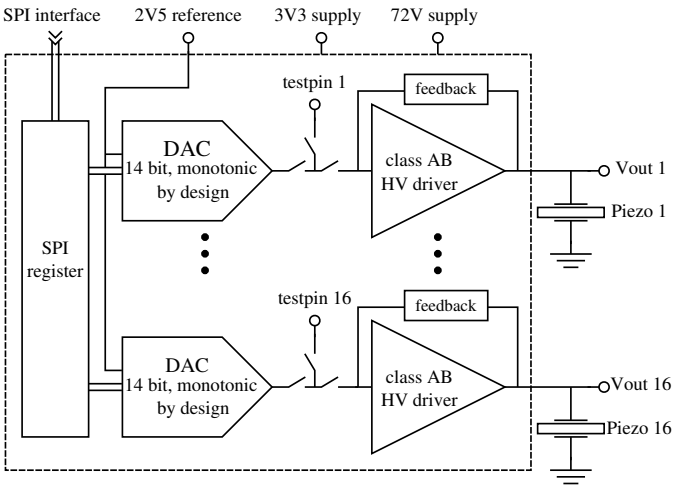

Fig. 2. Overview of the presented 16 channel high-voltage driver chip. The low-voltage and high-voltage part of the chip are powered by respectively 3.3 V and 72 V. A 2.5 V reference voltage is used for the 14 bit DACs. DAC-values and testpin direction are set by means of an SPI-register.

The technology of choice for the presented work is the On-Semi I3T80 technology which incorporates a 0.35 μm CMOS process with floating high-voltage quasi-vertical nDMOS and lateral pDMOS transistors [9]. The implemented transistors have a maximum rated bulk drain voltage V_{bd} of 70 V while the supply voltage needed to fully drive the piezoactuator is 72 V. However, the transistors have an avalanche breakdown voltage at or above 78.5 V which is the absolute upper voltage limit when the devices are in the off state. While the upper limit of the static safe operating area (SOA) is 70 V the high-voltage transistors can withstand a somewhat higher voltage. Since the mechanism which determines the static SOA of the devices is hot carrier degradation, the maximum voltage can be exceeded as long as this happens at limited current-densities. When looking at short current pulses, as is the case with this design, the limits on the maximum drain voltage are determined by the thermal (dynamic) SOA. The thermal SOA has the turn-on of the parasitic bipolar transistor in each DMOS as upper voltage limit which is well above 70 V.

III. CLASS AB HIGH-VOLTAGE OUTPUT DRIVER

A. Amplifier Class and Stages

As previously mentioned, driving a piezoelectric actuator is in many cases done most efficiently by using a class D amplifier. In this case 14 bit of accuracy requires a high-switching frequency for the amplifier in order to get enough attenuation from the LC low pass filter (with the C the piezoactuator capacitance and the L either externally or internally implemented depending on the value). To get a voltage ripple lower than half an LSB at the output (approximately 2.25 mV), the required attenuation is given by formula (1) which gives

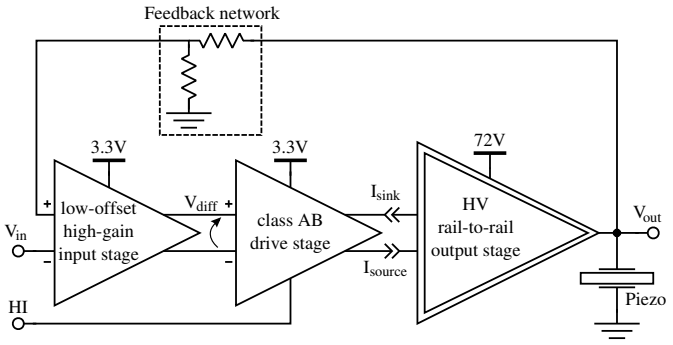

Fig. 3. Overview of the HV output driver. Three seperate amplifier stages are combined within the same feedback loop. The signal HI puts the output driver into high-impedance mode.

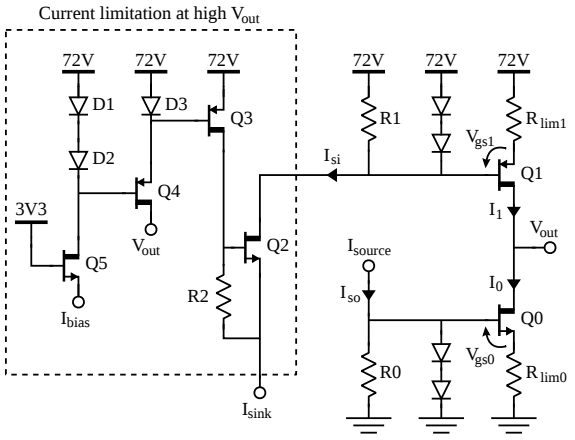

Fig. 4. Circuit used for the high-voltage rail-to-rail output stage implementing an output current limitation and limitation of the internal current in case the output voltage V_{out} saturates against the upper voltage rail.

a value of 86.03 dB for a supply voltage of 72 V.

$$\text{Attenuation} = \frac{V_{supply} \cdot \frac{2}{\pi}}{\frac{1}{2} \cdot \text{LSB}} = 86.03\text{dB}. \quad (1)$$

If a HV driver bandwidth of 5 kHz is considered and the LC filter gives 40 dB/decade attenuation, a switching frequency higher than 707.5 kHz is needed. This is not much higher than typical values of switching frequencies for high-voltage class D amplifiers which go up to 500 kHz [10]. However for the output transistors, with a total parasitic capacitance of 7 pF, the switching loss with a 707.5 kHz switching frequency already amounts to 12.8 mW. For the class AB amplifier presented in this paper, the quiescent current drawn from the 72 V supply for each output driver is 36.3 μA which leads to a continuous power consumption of 2.61 mW for the high-voltage part of the amplifier, which is considerably smaller than the switching losses of a class D output driver. As a result, for applications which require a low voltage ripple, and subsequently a high switching frequency, and where the overall power consumption is determined by the quiescent power consumption, as is the case for this and many other micropositioning systems, the use of a class AB will often be able to support a lower total power consumption.

The high-voltage output driver consists of three separate amplifier stages within the same feedback loop. Two of these amplifier stages are low-voltage (3.3 V) amplifiers with the first one a low-offset high-gain input stage and the second a class AB stage needed to drive the HV rail-to-rail output stage. The drive stage is also able to put the output driver into high-impedance mode as will be shown later on. An overview of the output driver can be seen in Fig. 3.

The input stage is used to generate an amplified version of the difference between the input voltages V_{diff} and the variation of the input stage offset over the input range will result in the main source of deterioration of the driver INL. At the drive stage the biasing and drive currents, I_{sink} and I_{source} are provided for the HV output driver. Biasing the output driver into class AB is thus done at the drive stage. The complete output driver has an open loop gain of 125dB with the dominant pole caused by the piezoactuator capacitance together with the HV driver output resistance (parallel combination of the resistive feedback network and rail-to-rail output stage) which amounts to roughly 5.85MΩ. The second pole is the result of the parallel combination of the feedback network and the input capacitance of the low-offset high-gain input stage and causes the requirement for a minimum capacitance of 100nF at the output of the HV driver resulting in a phase and gain margin of respectively 63.94^o and 27.26dB. This 100nF is much smaller than the capacitance of the majority of piezoelectric actuators which typically have a capacitance in the micro-farad range.

The input voltage V_{in} generated by the DAC ranges from 0 V to 2.5 V. This means that a voltage gain of 28.8 is needed to go up to the 72 V supply. To have some margin on the voltage gain, the feedback network creates a voltage division with a factor 30. Because of this somewhat larger division ratio, or due to a smaller supply voltage, the output voltage can saturate against the upper voltage rail.

B. HV Rail-to-Rail Output Stage

The HV output stage needs to source and sink current to and from the piezoactuator creating voltages going nearly rail-to-rail (0 V to 72 V). This stage requires a limited sunk/sourced current to avoid hot carrier degeneration of the output transistors or disturbance of nearby drivers due to excessive power dissipation and the resulting heat generation. Also a protection mechanism is to be built into the output stage to bring down the input current in case the output voltage runs stuck against the upper voltage rail. The circuit implementing this functionality is shown in Fig. 4.

When considering the circuit of Fig. 4 without the current limitation circuit at high V_{out} (I_{sink} node directly connected to the gate of Q1), it can be seen that by increasing the current I_{si} the gate-source voltage V_{gs1} of Q1 will increase and a current I_1 is sourced by Q1. By shifting the values of I_{so} and I_{si} a current can be sourced or sunk at the output node. The presence of resistors R0 and R1 is needed to bias transistors Q0 and Q1 with a sufficiently low biasing current I_{so} and I_{si}. The combination of two transistors in diode configuration (minimum size transistors) at the base of Q0 and Q1 and the resistors R_{lim0} and R_{lim1} creates an upper limit for the

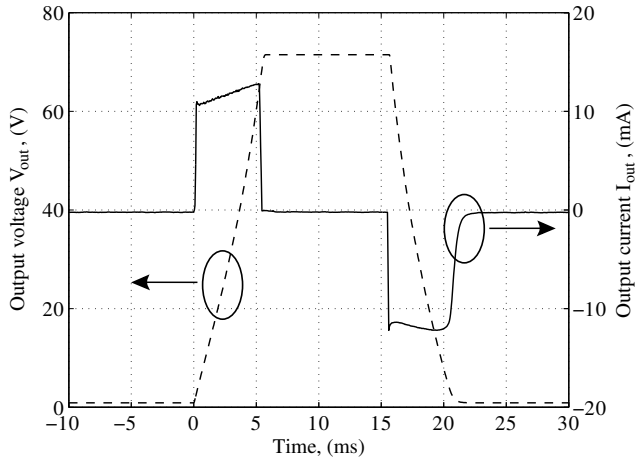

Fig. 5. Measured output voltage V_{out} and current I_{out} for a full scale (0 V-72 V) pulse with a 1.2 μF load capacitance. The sourced and sunk current is limited to approximately 12.5 mA.

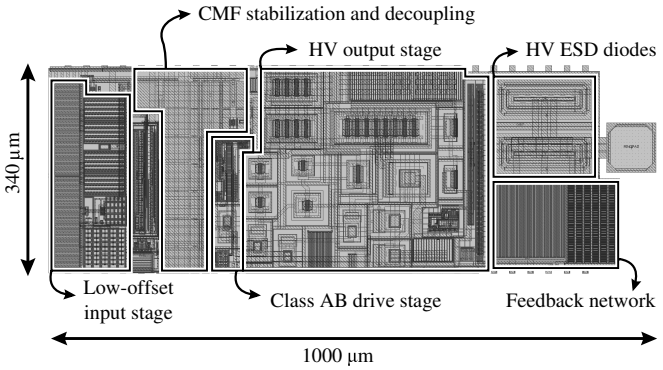

Fig. 6. Layout of the HV output driver measuring 1000 μm $\times$ 340 μm. The output driver consists of three amplifier stages: a low-offset input stage, a class AB drive stage and a HV output stage. Additional area is needed for the feedback network, HV ESD diodes and the CMF stabilization and decoupling capacitors.

sunk and sourced current. By increasing the resistor value of R_{lim0} and R_{lim1}, a maximum sourced or sunk current of approximately 12.5 mA is achieved.

Since a class AB drive stage is used to create I_{si} and I_{so}, the current I_{si} will remain high if the output voltage pinches off transistor Q1 before the fed back output voltage equals the input voltage of the output driver. This would lead to a large continuous power consumption in case several outputs saturate against the upper voltage rail due to e.g. collapse of the HV supply. To avoid this the current limitation circuit shown in Fig. 4 is added. The actual limitation is enforced by transistor Q2 together with resistor R2 which cut the current I_{si} when the drain current of transistor Q3 drops. This current in turn is controlled by a translinear loop consisting of D1 and D2 (transistors in diode configuration) and transistor Q3 and Q4. When the output voltage gets too close to the HV rail, the current through Q4 and thus Q3 is decreased. In order not to influence the normal operation of the output stage, the currents through transistors Q3 and Q4 need to be small, roughly 600 nA in this design, in comparison to the quiescent I_{si} current which is approximately 28.2 μA. Similar measures in case of transistor Q0 being pinched off aren't required since current I_{so} has a far smaller impact on the total power consumption as it is drawn from the 3.3 V rail.

The measured transient behavior of the output driver for a full scale pulse (0 V-72 V) with a 1.2 μF load is shown in Fig. 5. For this load capacitance, which is a typical value for piezoelectric actuators applied in micropositioning [2], a switching time of approximately 6 ms is achieved with a maximum sunk and sourced output current of roughly 12.5 mA. Based on the measured slew rate a full power bandwidth of 53 Hz is attained while the measured small signal bandwidth of the HV output driver amounts to 2.75 kHz.

By limiting the sunk and sourced current the output transistors Q0 and Q1 can remain relative small. Transistors Q0 and Q1 have a layout area of respectively 7680 μm^2 and 16500 μm^2 and their maximum V_{gs} voltage rise to 2.15 V and 1.75 V respectively which leads to a relatively low current density for these devices. This low current density is appropriate since the output transistors are used above their maximum drain-bulk voltage of 70 V. Although the output HV transistors can remain small, the layout of the HV output stage will still dominate the total layout area of the output driver as can be seen in Fig. 6. This is due to the area taken by the previously discussed current limitation circuit and the area needed by resistors R_{lim0} and R_{lim1}.

C. Class AB Drive Stage

The class AB drive stage has the function of biasing the HV output stage in class AB mode and to provide a high impedance mode of operation. This is done by means of the drive stage shown in Fig. 7.

The circuit in Fig. 7 uses a cross-coupled quad to accurately set the quiescent current and provide an expanding current characteristic in function of the differential input voltage V_{diff} [11]. By using the current mirrors Q0-Q1 and Q2-Q3 the expanding currents of the cross-coupled quad are used to drive the output stage. By increasing the W/L ratio of transistors Q0 and Q2 the maximum sunk and sourced current can be made larger. Communication between the low-voltage and high-voltage domain is commonly done by means of a cascode transistor [12] which is also done here by means of transistor Q4. When looking at the output stage of Fig. 4 it can be seen that cutting the currents I_{sink} and I_{source} will put the output in a high-impedance state. This is done in the drive stage by means of switches S0 and S1. However the resistive feedback network at the output node, as shown in Fig. 3, limits the maximum attainable output resistance to 5.85 MΩ.

D. Low-Offset High-Gain Input Stage

The behavior of the position of piezoactuators under voltage control can be extremely hysteretic which means that applications requiring accurate positioning use a position feedback loop. Because of this, the integral non-linearity (INL) of the HV-driver can be several tens of LSBs without any cause for concern. However a high resolution is needed to make sure that the position of the piezo can be accurately set. The goal for

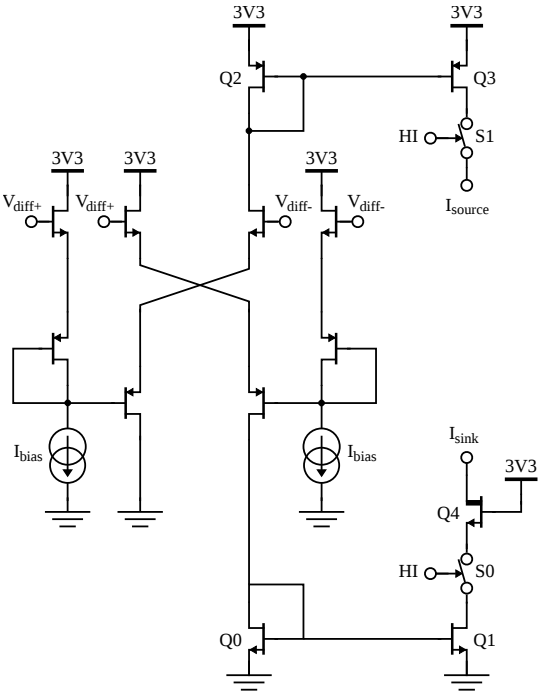

Fig. 7. Drive stage used to bias the HV output stage in class AB. Switches S0 and S1 implement a high impedance mode of operation for the output driver. Transistor Q4 in this schematic is a high-voltage device.

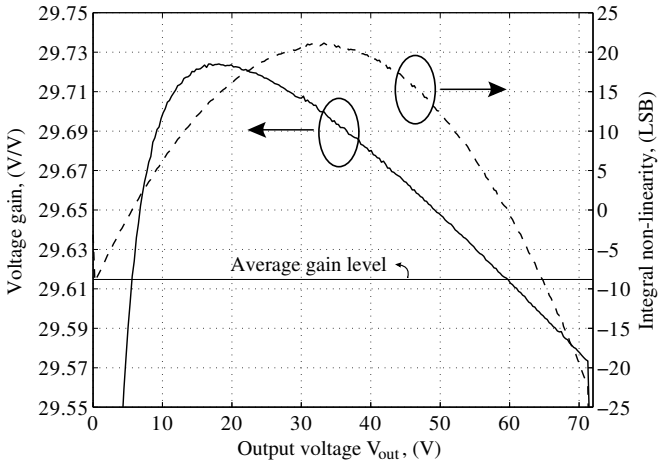

Fig. 8. Measured output driver voltage gain in function of the output voltage. The average gain amounts to 29.62 while the INL of the output driver remains smaller than 23 LSBs.

the output driver is an INL lower than 32LSBs which means that the combination of input-referred random and systematic offset needs to be lower than 4.88 mV ($32 \cdot 2.5$ V / 2^{14}). In Fig. 8 it can be seen that the INL added by the output driver remains below 23 LSBs (similar behavior was measured for a total of 64 channels).

A fully differential folded cascode opamp was implemented as input stage since the PMOS version of this circuit allows input voltages which go down to, or lower than, the ground rail while still providing high levels of gain as needed to reduce the systematic offset as much as possible [11]. In order to diminish the input-referred offset of the input stage, two large PMOS input transistors, biased in weak inversion, are used. Since a fully differential opamp is used, a common-mode feedback (CMFB) circuit is needed to set the common-mode output voltages. Large capacitors are needed to stabilize this CMFB circuit as shown in Fig. 6.

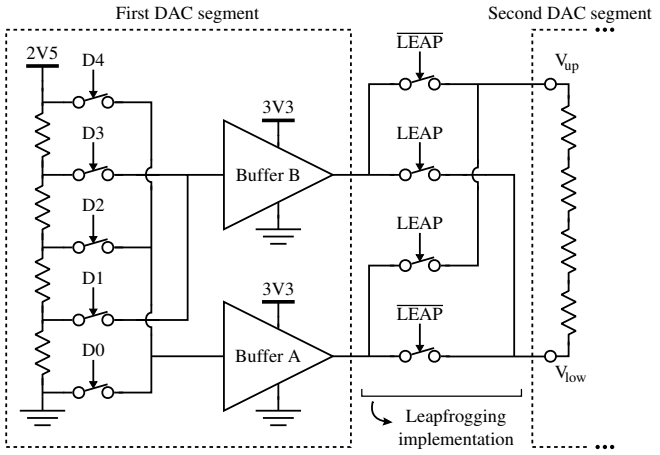

Fig. 10. Segmented resistor string DAC with a 2 bit first segment. Bits D0-D4 switch the correct voltage to either buffer A or B. Leapfrogging is used to assure monotonic behavior.

IV. Monotonic by design 14 bit DAC

A. Requirements and Topology

The two main requirements for the DAC are a 14 bit resolution and guaranteed monotonic behavior. An additional requirement is a full scale rise/fall time below 100 μs. This is implemented by means of a segmented resistor string DAC with a total of three segments of which a schematic overview is shown in Fig. 9. The principle of the three segment resistor string DAC is further explained in Fig. 10 in which focus lies on the first segment and the leapfrog switches in between segments. A first segment with only two bits is depicted in Fig. 10 for simplicity where the actual DAC uses a 5 bit first segment.

When looking at the switching matrix (switched by bits D0-D4) in Fig. 10 it can be seen that a certain switch is always connected to the same buffer. This ensures that the difference in offset between buffers A en B doesn't cause non-monotonic behavior and that buffer B (or A) leapfrogs buffer A (or B) when going from one section in the resistor string to the next. Each time buffer A and buffer B leapfrog (corresponds to the LSB of each segment), the second segment decoding direction needs to switch [13]. This is avoided by adding leapfrog switches between the first segment output buffers and the lower and upper connection of the resistor string of the next segment, which allows to limit the added complexity for the switching array (switches D0-D4) of the following segment.

Next to a monotonic by design topology and 14 bit resolution, a total channel INL lower than 32 LSBs is desired. To achieve this, taking into account the combination of DAC and output driver, an INL lower than 8 LSBs is desired for the DAC with a targeted yield of at least 99.7% (3σ interval). The INL of the DAC comes from the mismatch of the resistor strings and the difference in offset of the buffers in between resistor strings.

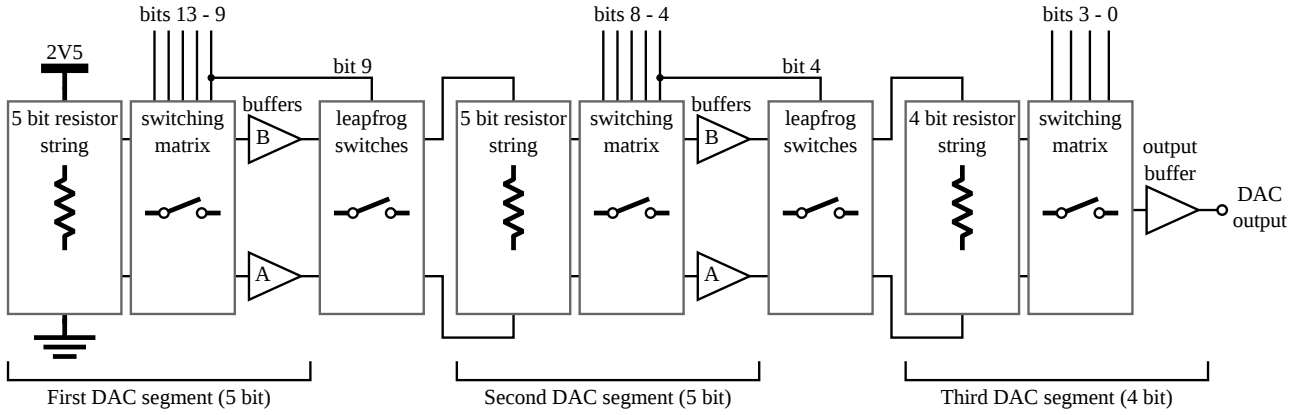

Fig. 9. Schematic overview of the 14 bit DAC which consists of a three segment resistor string DAC. The 5 MSBs are decoded at the first segment, bits 9 to 4 at the second segment and the 4 LSBs at the final segment.

For both these contributors the aim is to get an INL lower than 4 LSBs.

B. Segmentation and Resistor String Layout

A choice for the segmentation of the 14 bit DAC is made under the assumption that the maximum INL ($|\text{INL}|_{\text{max}}$) is dependent on solely the first segment. Then $|\text{INL}|_{\text{max}}$ for a N bit DAC in function of the maximum deviation on the unit resistor value due to mismatch (%matching) is given by [14]:

$$|\text{INL}|_{\text{max}} = \frac{1}{2} \cdot \text{LSB} \cdot 2^{\text{N}} \cdot \%\text{matching}. \tag{2}$$

This means that a 14 bit DAC will require 0.049% matching if a maximum INL of 4 LSBs is required. The number of bits in the first segment is a trade-off between the number of required resistors/switches and the matching level needed in the second segment. A higher number of bits in the first segment will lead to a low matching requirement for the second segment but will lead to a high number of required resistors. Since chip resistors have a minimum dimension, the minimum needed area for the first segment is linear with the number of resistors. Having more than 8 bits for the first segment isn't sensible since then not only the size of the resistor string, using minimum size resistors, becomes large but also the layout area needed for the circuit driving the switches becomes excessive.
In order to get an idea about the required matching for the second segment in function of the number of bits in the first segment, a choice needs to be made in respect to how large the maximum INL of the second segment ($|\text{INL}|_{\text{max,seg2}}$) can be with respect to the INL of the first segment ($|\text{INL}|_{\text{max,seg1}}$). In this design a 16 times smaller INL was chosen for the second segment to make sure that the initial assumption regarding the overall DAC INL holds, which leads to the following formula for the second segment INL:

$$\begin{aligned} |\text{INL}|_{\text{max,seg2}} &= \frac{|\text{INL}|_{\text{max,seg1}}}{16} \\ &= \frac{1}{2} \cdot \text{LSB} \cdot 2^{\text{N-N1}} \cdot \%\text{matching}. \end{aligned} \tag{3}$$

Equation 3 gives the maximum INL of the second segment with N1 the number of bits of the first segment. The required matching for the second segment resistors, with $|\text{INL}|_{\text{max,seg1}}$ equal to 4 LSBs, is then given by:

$$\%\text{matching} = \frac{1}{2^{\text{N-N1+1}}}. \tag{4}$$

Based on the previously mentioned considerations a 5 bit first segment was chosen which leads to a required matching of 0.098% for the second segment. For this segment the same layout of the first segment is re-used which ensures that the required level of matching will be attained. The last segment is a 4 bit resistor string which can be made more than four times smaller then the first two segments due to the lower matching requirements. The complete 14 bit DAC will thus comprise of two 5 bit segments, one 4 bit segment and five buffer stages as can be seen in the layout shown in Fig. 11. The layout area needed for the buffers is large in comparison to the layout area of the resistor strings. This is due to the additive nature of the INL caused by a difference in buffer offset, i.e., a difference in offset voltage between the buffers of the first segment will have the same effect on the overall DAC INL as a difference in offset between the buffers of the second segment which translates to a low offset requirement. Also the buffers require large compensation capacitors which are the result of using a low biasing current leading to a high buffer output resistance which, together with the buffer input and output capacitance, causes a low frequency parasitic pole. To get sufficient matching between the resistors of a certain segment, the area of the segment unit resistor needs to be increased since the random mismatch between resistors is inversely proportional to the square root of their area. This leads to a high-ohmic poly resistor with a value of 40kΩ for the unit resistor and an area of 640μm^2. Systematic mismatch, on the other hand, is caused by process and temperature gradients and increases with the separation between resistors. To eliminate the influence of first order gradients a diagonal shuffle layout can be used [15]. A detail of the layout of the first and second segment is shown in Fig. 12. The 5 bit first and second segment of the DAC uses a diagonal shuffle layout

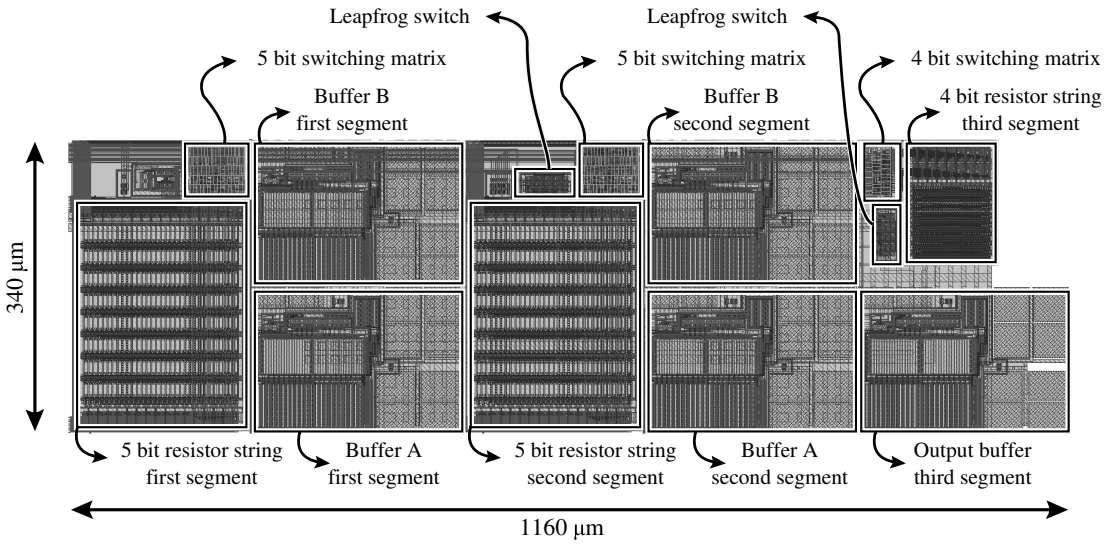

Fig. 11. Layout for the complete 14 bit DAC measuring 1160 μm $\times$ 340 μm. Five buffers are needed of which two in between the first and second segment, two between the second and third segment and one output buffer. Two leapfrog switches are necessary with one in between the buffers of the first segment and the 5 bit second segment resistor string and another to connect the second segment buffers with the 4 bit resistor string.

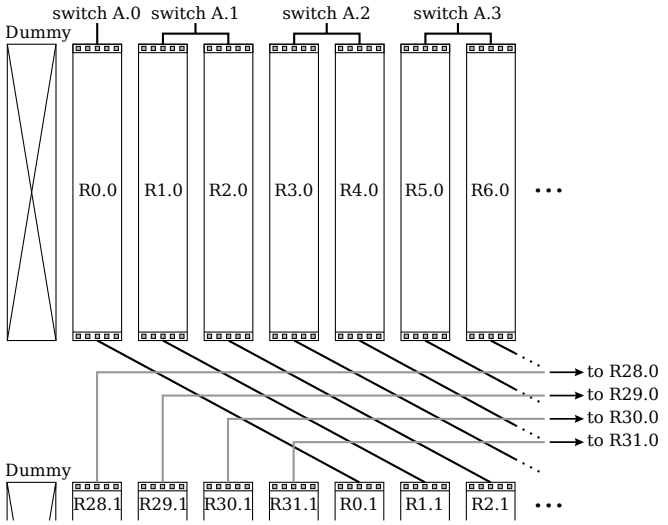

Fig. 12. Detail of the 5 bit resistor string implementing a diagonal shuffle layout with a shift of 4 resistors for each row resulting in a total of 8 rows. At the top the connections to the switches leading to one of the buffers (buffer A) are shown. Dummies are added on the right and left of the layout.

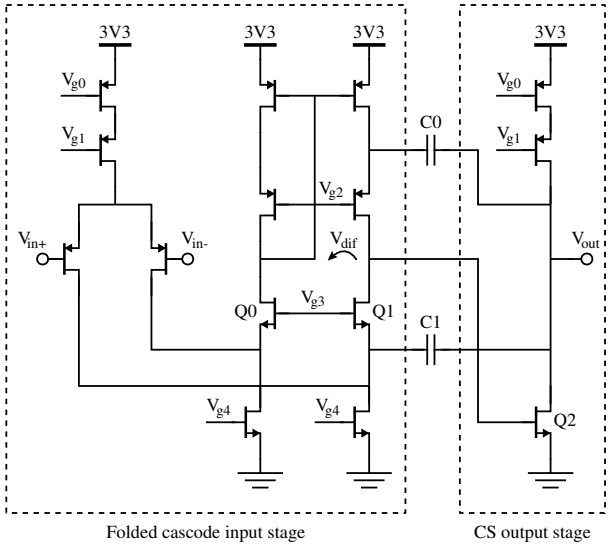

Fig. 13. Opamp circuit used as low-offset buffer in between segments. A folded cascode PMOS input stage is implemented with a common source (CS) NMOS output stage. Capacitors C0 and C1 are added for stabilization of the opamp.

with a shift of 4 resistors for each row which means that a total of 8 rows is needed. The total area for the resistor string of the first and second segment is 40950 μm^2. The last 4 bit segment uses a shift of 2 resistors resulting in 8 rows and a resistor string area of 8820 μm^2.

C. Low-Offset Buffer

The increase in INL of the complete DAC due to the difference in offset voltage of the different buffers is set to be smaller than 4 LSBs. Also the buffer needs a Vin- and output that can go down to the ground rail to keep the zero code error minimal. Moreover, to minimize the static error between the Vin- and output the buffer requires a large loop gain. These requirements are fulfilled by using a two-stage opamp with a folded cascode PMOS input stage followed by a common source NMOS output stage. The schematic for this opamp can be seen in Fig. 13. Due to the use of a two-stage opamp, compensation needs to be added which is done by means of capacitors C0 and C1.

The use of a common source (CS) NMOS output stage will allow that the output voltage V_{out} can go very close to the ground rail, however, it also causes a difference voltage V_{dif} between the drains of transistors Q0 and Q1 in Fig. 13. This results in a systematic offset voltage between the opamp inputs which is minimized by increasing the gain of the folded cascode stage. The total power consumption of the buffer stage is approximately 7 μA which leads to a gain bandwidth for

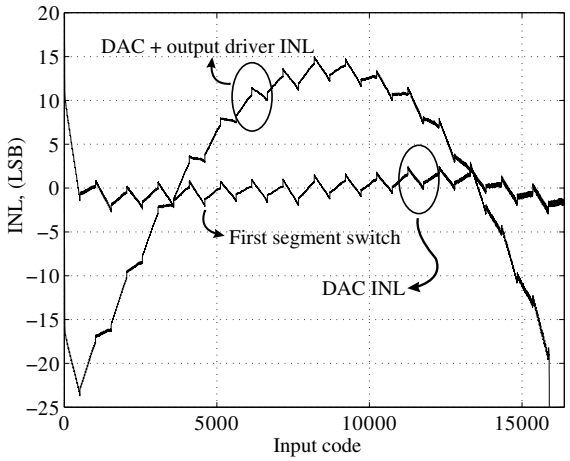

Fig. 14. Measured INL for all input codes for both the DAC and the DAC together with the output driver. The switching points of the first segment can clearly be seen. The zero code error for the DAC is smaller than 10 LSBs.

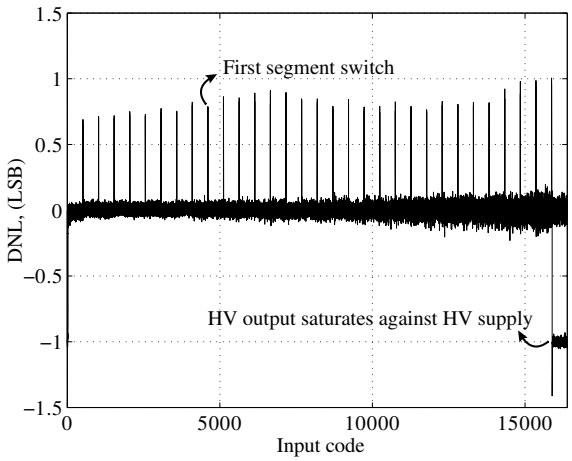

Fig. 15. Measured DNL for all input codes for both the DAC and the combination of the DAC and output driver. The DNL of these two overlap almost perfectly up to the point where the HV output voltage saturates against the HV supply rail. Both show monotonic behavior (as expected) and switching points of the first segment can clearly be seen.

the buffer of 240 kHz. The measured rise and fall time (10% - 90%) at the DAC output for a full scale DAC switch amount to respectively 72.8 μs and 19.2 μs with a load capacitance of 4.7 pF placed at the testpin which is roughly the same as the input capacitance of the HV output driver.

D. INL and DNL

The INL and DNL of the 14 bit DAC have been verified by means of the testpin in between the DAC and the HV output driver (see Fig. 2). In Fig. 14 the measured INL of the DAC and the INL of the full channel (DAC + output driver) can be seen. Clearly noticeable are the switching points of the first DAC segment. Due to the difference in offset between the buffers of the first segment, the INL curve shows a wave pattern. The zero code error is smaller than 10 LSBs which is mainly influenced by the sizing of the output NMOS transistor in the low-offset buffer. When neglecting the zero code error an INL smaller than 4 LSBs is achieved. For the full channel the INL curve is the combination of the INL curve shown in Fig. 8 and the DAC INL. A maximum INL of 23 LSBs is measured for the full channel. The INL of the complete channel is not significantly degraded by the DAC INL due to the specific shape of the output driver INL and the use of a best fit line. The measured DNL of the DAC and the combination of the DAC with the HV output driver is shown in Fig. 15, and demonstrates monotonic behavior with spikes in the DNL curve at each point that the first segment buffers leapfrog.

V. Driver Noise, PSRR and Crosstalk

A. Driver Noise and Power Supply Rejection Ratio (PSRR)

The use of a feedback network with a high impedance and small biasing currents means the amount of noise at the output of the driver becomes non-negligible. Noise measurements resulted in a typical integrated output noise of 1mV_{pp} and 1.6mV_{pp} for an integration bandwidth from 20Hz up to 1kHz and 10kHz respectively. These levels are sufficiently low when considered against the LSB at the output of approximately 4.5mV. Integration over higher bandwidths doesnt make sense when considering the limited bandwidth of piezoactuators.

A resolution of 14 bit means that a variation on the output voltage due to a fluctuation of the power supply will quickly result in an error of several LSBs when the DC and AC power supply rejection ratio (PSRR) isnt sufficiently high. The presence of several switching output driver on the same chip together with the impedance of both the low-voltage (3V3) and high-voltage (72 V) supply lines can result in strong fluctuations of the supply voltage. This is hard to solve by adding on-chip capacitors since these would take an excessive amount of chip area (mainly fluctuations below 10kHz are of importance due to the limited bandwidth of piezoactuators). Moreover it isn't possible to use metal-insulator-metal (MIM) capacitors on the high-voltage supply due to the maximum voltage rating of the insulator layer which means that all capacitance on the HV supply needs to come from capacitors using interdigitated metal layers.

The HV part of the driver is relatively insensitive to fluctuations on the HV supply since current inputs drive the HV output stage as shown in Fig. 4. In order to make the low voltage part of the chip independent from fluctuations on the 3V3 rail, the DAC reference voltage is chosen at 2.5 V, see Fig. 9, which equals the maximum voltage to be buffered in the DAC and at the input of the HV output driver. By providing some headroom between the maximum DAC voltage and the 3V3 rail it becomes possible to use cascoded current sources to bias the DAC buffers, see Fig. 13, thus increasing the PSRR. When measuring the PSRR of both the 3V3 and the 72 V rail at the HV output, the 3V3 PSRR will be lowered with the 29.4 dB voltage gain of the output driver. Measurement of the DC PSRR of the 3V3 and 72 V rail at the HV output results in a value of respectively 43.2 dB and 92.2 dB. In other words, a variation of 10 mV at the 3V3 rail results in a 2.34 μV and 69.2 μV variation at the DAC and HV output respectively, corresponding to 0.015 LSB. For the HV rail this means that a 1 V variation results in a 24.5 μV (0.0054 LSB) difference at the HV outputs.

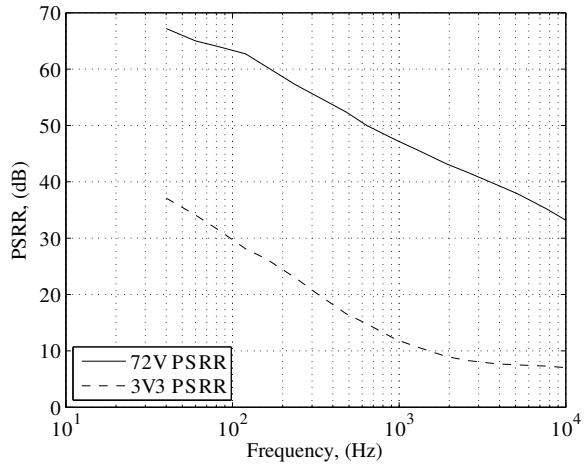

Fig. 16. Measured PSRR for the low-voltage (3V3) and high-voltage (72 V) rail at the HV output from 30 Hz to 10 kHz. The 3V3 PSRR is roughly 30 dB lower than the 72 V PSRR which corresponds to the voltage gain in the HV output driver.

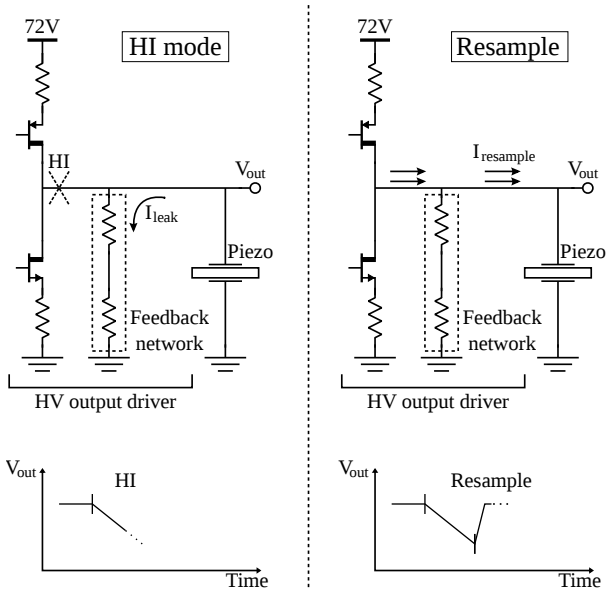

Fig. 17. Current flow and evolution of the output voltage during the HI mode (left) and the resampling of the output (right).

Although the bandwidth of most piezoactuators is small, not only the DC PSRR is of importance. The measured AC PSRR (from 30 Hz - 10 kHz) is shown in Fig. 16 and decreases in function of the frequency. Taking into account a piezoactuator with a resonance frequency of 200 Hz, a PSRR of 68.9 dB and 24.2 dB is measured for respectively the 72 V and the 3V3 rail. The PSRR for the 3V3 becomes lower for higher frequencies (at 200 Hz a 10 mV variation at the 3V3 rail corresponds to a 0.14 LSB difference at the HV output), however, the fluctuations of the 3V3 rail will typically be much lower since the currents sourced by this rail are several orders lower than these drawn from the 72 V rail. Also the amount of on-chip decoupling of the 3V3 rail is quite large (6.8 nF) thus dampening voltage variations at higher frequencies.

B. Driver Crosstalk

When integrating several drivers onto the same chip with their respective DAC, crosstalk between drivers becomes an important aspect. For instance, when five drivers switch downwards at the same time, a current of roughly 62.5 mA is sunk into the on-chip ground. With an impedance of the on-chip ground of 10 mΩ this leads to a rise of the ground level with 625 μV corresponding to 4.1 LSBs at the DAC which corresponds to an error of 2.05 LSBs with the DAC output halfway. Adding to this is the variation of the on-chip ground impedance with the location of the disturbed channel. The worst case of crosstalk will occure for channel 7 and 8 which are located in the middle of the chip having the highest ground impedance.

In order to cope with the driver crosstalk two techniques are discussed in this paper. One technique is to stagger the switching which limits the crosstalk to short pulses which, together with the limited piezo bandwidth, lead to a lower average crosstalk. The proposed, second method is one in which, during the switching of one or several drivers, the non-switching drivers are put into high-impedance mode by means of the HI switches shown in Fig. 7. The piezo capacitance then acts as a sort of sample and hold capacitor which isolates the driver output voltage from crosstalk between drivers. It should be noted that the feedback network is placed directly at the output which leads to current leaking out of the piezo capacitance in case the output driver is placed into high-impedance mode. To counter this the output needs to be resampled during the switching of the other drivers. This method and the attributed currents and piezoactuator voltages during the HI-mode and the resampling period are shown in Fig. 17. Both methods of countering driver crosstalk were tested by switching all channels but channel 8 from 72 V to 0 V and measuring the output voltage of channel 8. The result for this worst case scenario can be seen in Fig. 18.

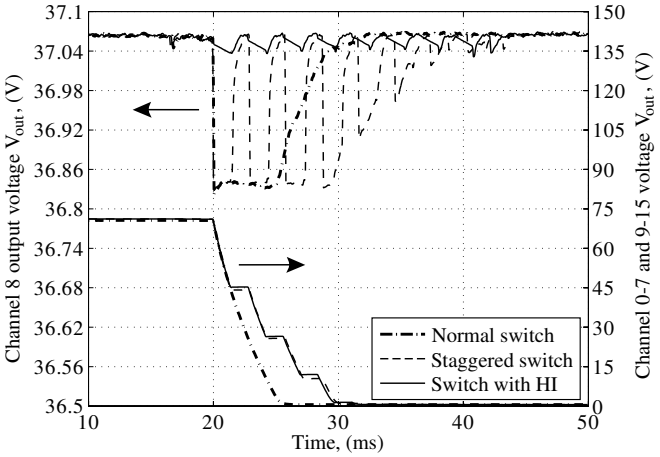

Fig. 18. Channel 8 output voltage for a switching of all other channels from 72 V down to 0 V. Crosstalk levels are measured for three different modes of switching: normal switching, staggered switching and staggered switching with the use of the high-impedance mode.

By using staggered switching, the switching time increases significantly while the crosstalk levels are still high (peak crosstalk voltage of approximately 52 LSBs). When using the

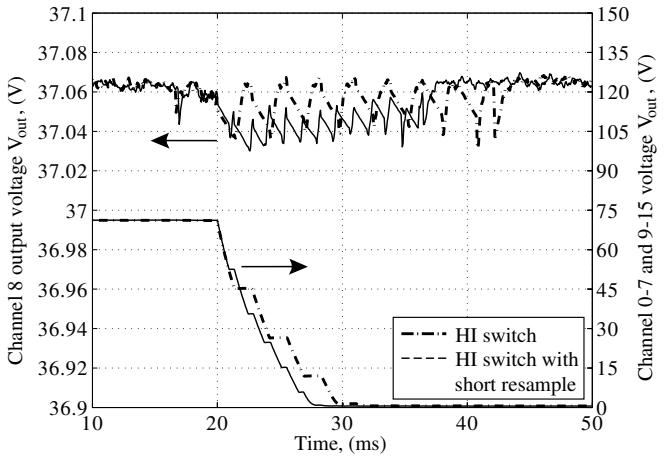

Fig. 19. Channel 8 output voltage for a switching of all other channels from 72 V down to 0 V using the proposed switching method. Switching and crosstalk voltages are measured for a shorter resample time and a resample time equal to the switching time.

proposed method the crosstalk drops to a reasonable level (5 LSBs) but Fig. 18 shows that it still causes a doubling of the switching time. The resampling time, however, can be made much smaller than the switching time and thus lead to a much smaller increase in switching time. This is demonstrated in the measurements shown in Fig. 19 where a resampling time that is three times shorter than the switching time is used. The result is a 8ms switching time which is a significantly smaller increase of the normal switching time of 6 ms in comparison to the 12 ms switching time achieved by using a resample time equal to the switching time.

As mentioned previously the crosstalk levels shown in Fig. 18 and Fig. 19 are for a worst case scenario. Moreover the driver and piezoactuator are typically placed in a larger position feedback loop, due to the piezoactuators non-linear position under voltage control, which means that the position feedback loop itself will cancel out any crosstalk if the loop bandwidth is sufficiently large.

VI. Driver Summary

Throughout this paper several measurements of both the 14 bit DAC and HV output driver were shown. A summary of this data is shown in Table II and Table III which show the properties of respectively the 14 bit DAC / HV output driver and the full channel. The measurements for the 14 bit DAC where performed with a 4.7 pF load, corresponding to the load of the HV output driver, while the data of the HV output driver is obtained with a 1.2 μF load which is a typical value for piezoactuators applied in micropositioning.

By using a class AB HV output driver the quiescent current from both the 3V3 and 72 V rail is limited to respectively 271 μA and 36.3 μA which results in a total chip quiescent power consumption of 56.1 mW. For each channel the sunk and sourced current is limited to approximately 12.5 mA which means that each channel can deliver an instantaneous power of roughly 894 mW (71.5 V $\times$ 12.5 mA) leading to a possible total chip power delivery of 14.3 W.

Due to the high PSRR and the use of the previously discussed

TABLE II
Summary of the output driver and 14 bit DAC characteristics.

Output driver (1.2 μF load)		DAC (4.7 pF load)	
Voltage gain	29.5 dB	Number of bits	14
Max. output current	$\approx$12.5 mA	Output rise time	72.8 μs
Max. output voltage	71.5 V	Output fall time	19.2 μs
INL	$<$23 LSBs	INL	$<$4 LSBs
Slew rate	$\approx$12 V/ms	DNL	$<$1 LSB
Small signal bandwidth	2.75 kHz	Zero code error	$<$10 LSBs
Full power bandwidth	53 Hz		

TABLE III
Summary of channel (DAC + output driver) characteristics.

Channel (1.2 μF load)	
Quiescent current (72V)	36.3 μA
Quiescent current (3V3)	271 μA
INL	$<$23 LSBs
DNL	$<$1 LSB
Output noise (20Hz - 1kHz)	1.0mV_{pp}
Output noise (20Hz - 10KHz)	1.6mV_{pp}
DC PSRR (72V)	92.2 dB
DC PSRR (3V3)	43.2 dB
Max. driver crosstalk voltage	$<$35 mV

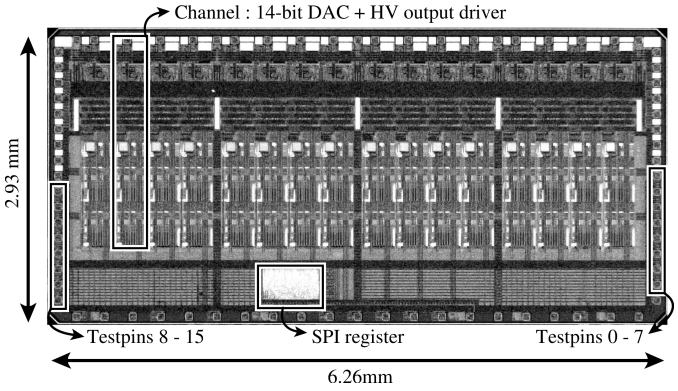

Fig. 20. Chip photomicrograph showing 16 HV channels with a total area of 2.93 mm $\times$ 6.26 mm. Also visible is the SPI register used to set the DAC values together with the testpins.

staggered high-impedance switching, it is possible to integrate 16 channels onto the same chip. A photomicrograph of the complete chip can be seen in Fig. 20 and has a total area of 2.93 mm $\times$ 6.26 mm (18.3 mm^2). In the total chip area, 11.8 mm^2 is reserved for the driver channels (14 bit DAC + HV output driver), 0.216 mm^2 is needed for the SPI register and the remaining area (6.28 mm^2) is taken up by biasing circuitry, signal distribution, ESD, IO-pins and decoupling.

VII. Conclusion

In this paper a 16 channel HV driver is presented which incorporates a HV class AB output driver and a 14 bit

monotonic by design DAC for each channel. The push-pull output driver has a current limitation built in which allows to limit layout area and crosstalk levels but also makes it possible to use the output transistors slightly above their maximum voltage rating. Additionally a safety mechanism is discussed which avoids high continuous current in case the output voltage saturates against the high-voltage rail. To the best of the authors knowledge this is the first demonstration of the integration of a high amount of HV piezoactuator drivers onto one chip with their respective DACs.

The 14 bit DAC has a segmented topology consisting of a 5 bit, 5 bit and 4 bit section. Segmentation of the DAC is based on the presented analysis of the trade-offs between matching and the number of bits chosen for each segment. Each DAC section consists of a resistor string which uses leapfrogging of the buffers to achieve a monotonic by design DAC. To attain sufficient matching levels for the resistor string, a diagonal shuffle layout is implemented which, together with the low-offset buffer, result in an INL lower than 4 LSBs and a zero code error smaller than 10 LSBs.

The integration of several drivers onto one chip with their respective DAC can lead to high crosstalk levels, as shown in this paper. To counter this the HV output driver and 14 bit DAC were designed to achieve a high PSRR. Furthermore a method of staggered switching with resampling of the output voltage onto the piezoactuator capacitance is proposed. It is demonstrated that by using this technique it is possible to significantly reduce the crosstalk levels (reduction from 52 LSBs to 5 LSBs) while still achieving low switching times. It thus becomes possible to closely integrate a high number of piezo drivers onto one chip with acceptable crosstalk levels.

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