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56+ Gb/s Serial Transmission using Duobinary Signaling

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Abstract

In this paper we present duobinary signaling as an alternative for signaling schemes like PAM4 and Ensemble NRZ that are currently being considered as ways to achieve data rates of 56 Gb/s over copper.
At the system level, the design includes a custom transceiver ASIC. The transmitter is capable of equalizing 56 Gb/s non-return to zero (NRZ) signals into a duobinary response at the output of the channel. The receiver includes dedicated hardware to decode the duobinary signal. This transceiver is used to demonstrate error-free transmission for different PCB channel lengths including a state-of-the-art Megtron 6 backplane demonstrator.

Authors' biographies

Timothy De Keulenaer is a Doctoral Researcher at INTEC-IMEC. He was born in Mortsel, Belgium, in 1987. He received his bachelor and master degree in applied electronics from Ghent University, Ghent, Belgium, in 2008 and 2010 respectively. Since August 2010, he has been working towards a PhD degree in the INTEC Design Laboratory of the department of Information Technology associated with IMEC. His research focuses on high-speed integrated circuit design and signal integrity aspects for backplane communication.

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1. Introduction

Recently, standards groups like the OIF CEI-56G-VSR/MR and the IEEE P802.3bs 400 GbE have been looking into serial data rates above 50 Gb/s as the line speed for future generation PHY's. The OIF is looking at serial data rates of 56 Gb/s, and different signaling and modulation schemes, such as PAM4 and Ensemble NRZ, which are being considered as ways to achieve these data rates over copper.

In this paper we present duobinary signaling as an alternative for achieving data rates above 50 Gb/s. Duobinary signaling is a 3-level modulation scheme that reduces the required channel bandwidth to half of that required for NRZ, and as such, has a bandwidth requirement on par with PAM4. The generation of a duobinary signal can make use of the inherent frequency-dependent channel loss, and hence requires less equalization, greatly reducing the overall system requirements. We will look at the differences between duobinary and PAM4 modulation with respect to transmitter and receiver complexity, required equalization, etc.

A duobinary transmitter and receiver capable of operating at speeds of 56 Gb/s and above, specifically designed for backplane transmission, were designed for system-level demonstration. The transmitter accepts a pre-coded NRZ signal and equalizes the frequency-dependent channel loss to produce a duobinary signal at the output of the channel. A dedicated receiver recovers the two eye-patterns – typical for a duobinary constellation – and decodes them to the original NRZ data sequence.

For system-level evaluation and validation, test boards were designed. Integrated circuit chips were flip-chip mounted onto these test boards. Eye-pattern and bit-error-rate (BER) measurements were performed at 56 Gb/s on a state-of-the-art Megtron 6 backplane demonstrator.

2. Duobinary signaling

In the quest to reach higher serial data rates in electrical interconnects, there are several active solutions currently being pursued by the industry: increasing serial symbol rates with adaptive equalization and pre-emphasis, shifting to more complex signal constellations [1][2], and using multi-carrier modulation [3][4].
Here, as a point of reference for discussion, we use standard 2-level NRZ modulation, illustrated in the left-hand side of figure 1. The use of a higher order modulation, such as pulse-amplitude modulation (PAM) with 4 levels (PAM4 – illustrated in the center of figure 1) – while targeting the same data rate as the NRZ – allows for the reduction of the transmission bandwidth from 1/T to 1/2T (with T being the pulse width of the signal). PAM with 4 or more levels (PAM4, PAM5, PAM8, etc.) has been investigated.
The consequence of moving to multi-level modulation is that signal reception requires more decision levels with reduced level spacing. As a result, for the same average signal power and receiver noise, the probability of receiving a symbol in error is higher and the signal is more susceptible to deterioration due to inter-symbol interference (ISI). This signal-to-noise ratio (SNR) performance conclusion is based on a channel that has a flat frequency response over the bandwidth of all signaling types being compared. If this was the case, there would be no motivation to use a higher order constellation. In fact, for

backplane channels, the amplitude response inevitably rolls off as a function of frequency and will have nulls originating from e.g. via holes between signal layers. As a result, for certain channels, it is possible for multi-level, narrow bandwidth signaling to obtain a larger eye-opening, and hence a better SNR than NRZ. Whether or not this happens and for what type of signaling, very much depends on the channel frequency response and the desired data transmission rate. This phenomenon is true for PAM signaling as well as partial response (PR) signaling.
PAM4 with equalization is currently being used in the industry and has been shown to provide very good performance even over long traces. However, the susceptibility of PAM4 to ISI results in transceiver circuits typically being complex and difficult to integrate.

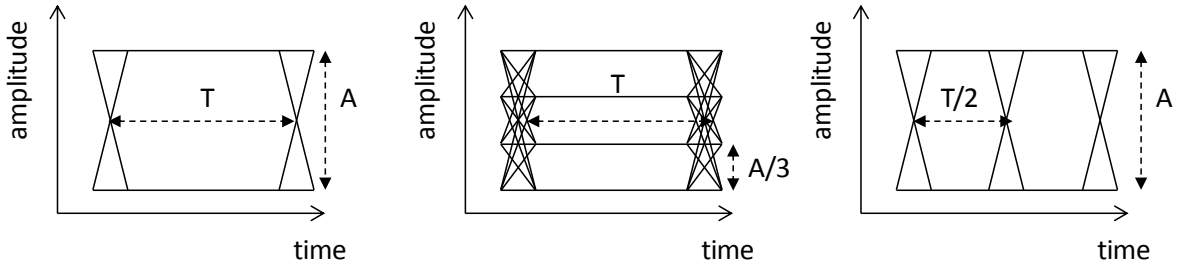

Figure 1: Waveforms of three modulation formats (from left to right): standard NRZ, PAM4 and NRZ with double bit rate.

The second solution towards reaching higher interconnect speeds is increasing the symbol rate, as indicated in the right-hand side of figure 1. The reduced symbol time (T/2 instead of T) leads to the expansion of the bandwidth occupied by the signal (see figure 2, left and center). However, low-cost dielectric materials used to construct backplane printed circuit boards exhibit strong frequency-dependent losses. The frequency-dependence leads to deterioration of signal integrity for any type of signal propagating through that channel. In order to overcome this problem, in some high-speed interconnect systems, the use of costly microwave substrates and special high-bandwidth backplane connectors is often required. Nevertheless, for long trace lengths impedance discontinuities from structures like via holes may still result in unacceptable transmission characteristics [5][6]. In order to overcome the imperfection of the channel, typically equalization and pre-emphasis techniques must provide correction for the entire frequency spectrum of the NRZ data.

The third alternative is to move away from baseband modulation formats towards multi-carrier formats. As illustrated in the right-hand side of figure 2, data is transmitted in multiple signal bands, which are individually equalized to accommodate imperfections of the physical channel. Multi-carrier techniques have been shown to be practical solutions for last mile digital subscriber loop (DSL) solutions [3]. However, for very high-speed backplane transmission, the cost and power consumption of transceiver integrated circuits still exceed the respective budgets [4]. Multi-lane transmission techniques for reaching higher interconnect speeds, such as the Ensemble NRZ modulation format, have also been demonstrated [7] but it remains to be seen whether such designs can find a practical application.

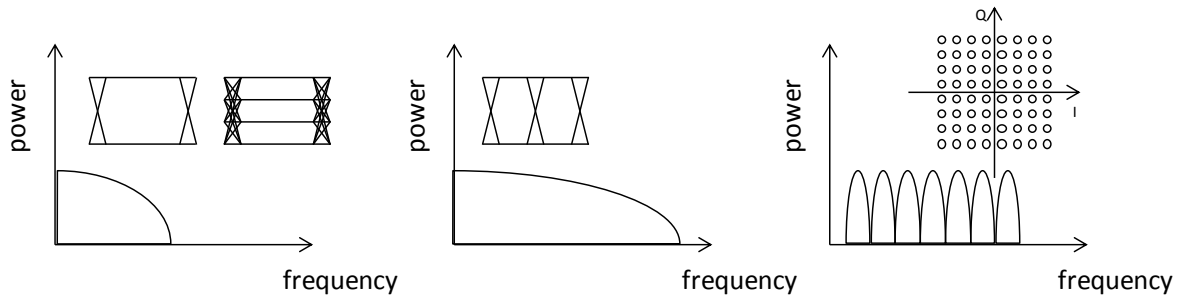

Figure 2: Waveforms of three modulation formats: standard NRZ and PAM4 (left), NRZ with higher bit rate (center), multi-carrier signal spectrum with quadrature amplitude modulation (QAM)-64 constellation in the inset (right).

The alternative approach to reaching higher interconnect speed adopted in this design is the use of PR signaling. In PR formats, data to be transmitted is temporally distributed over multiple symbols. In the particular case of duobinary modulation, each bit of information is distributed between two symbols as can be expressed by the simple Z-transform filter representation, $1+z^{-1}$. The controlled ISI forms a 3-level signal. Such waveform of duobinary modulation is schematically depicted in the center of figure 3.

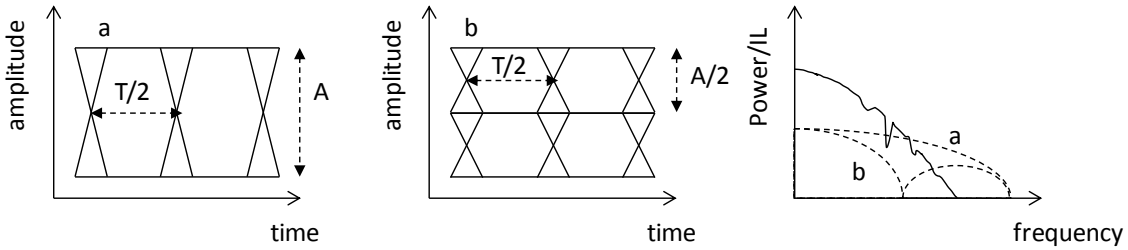

Figure 3: Waveform of NRZ (left) and duobinary modulation (center) for the same bit rate. Right-hand side of the figure compares the power spectral density of NRZ (a) and duobinary (b) modulation for the same bit rate with a superimposed example insertion loss profile of a physical channel (solid line).

Duobinary signaling was first proposed by Lender in 1963 [8] and evolved over the following decade [9][10]. This PR coding technique reduces the required signal bandwidth for transmission as compared to NRZ signaling. As a result the power spectral density (PSD) of the signal is concentrated in the lower frequency region of the channel, which exhibits less loss and irregularities. The cumulative PSD for duobinary is compared to that of NRZ in figure 4. The narrow bandwidth characteristic of the duobinary modulation has been used in both electrical [11][12] and optical transmission systems [13-17].

Traditionally, binary data is converted to duobinary data at the transmitter and then sent through the channel. In such a system, the conversion to duobinary is done using either a finite impulse response (FIR) filter that takes the form of a delay-and-add filter or a low-pass filter that results in an approximation of this frequency response. The resulting duobinary waveform uses significantly less bandwidth than its binary counterpart. This is clearly seen in figure 4, where the PSD of NRZ and duobinary are compared. It should be noted that in order to increase the signaling rate for duobinary as well as for NRZ

modulation, it is necessary to use a higher symbol rate (see figure 3, left and center). However, despite the higher symbol rate, the PSD of the duobinary format remains confined, due to the limited allowable signal-state transitions.

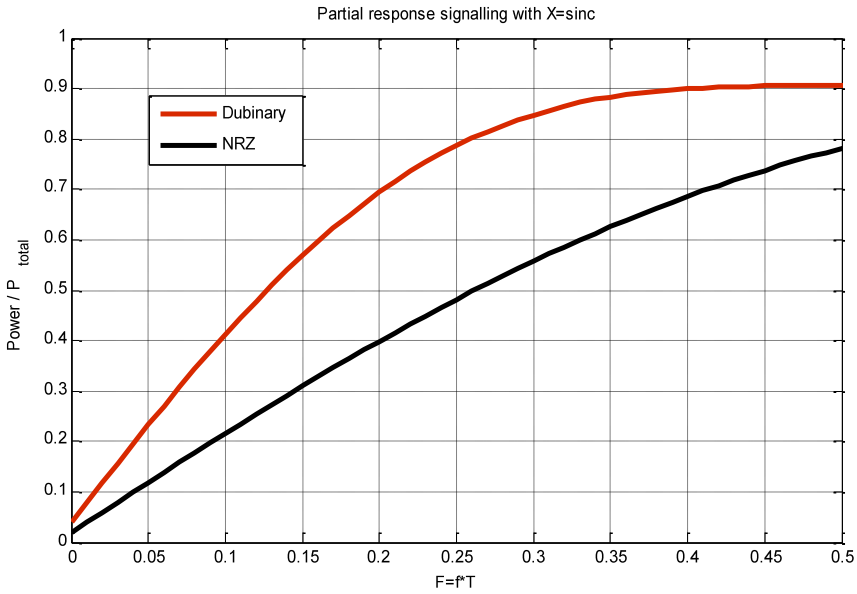

Figure 4: Cumulative PSD of duobinary modulation compared to NRZ; cumulative PSD is normalized to total signal power in both cases.

The required duobinary filter response can also be realized using the combination of the channel response and a FIR pre-emphasis filter [11][18]. The complex data spectrum originating in the transmitter is re-shaped such that the resulting waveform available at the receiver after traveling through the channel is a duobinary signal. The transmission system, shown in figure 5, has several main components: a binary data source, a duobinary pre-coder, a signal spectrum reshaping filter, the channel, a duobinary-to-binary data converter, and a NRZ receiver.

The typical channel will have a frequency roll-off that is much steeper than that of the desired duobinary signal. As a result, the reshaping filter is required to emphasize the higher frequency components as well as to flatten the group delay response across the signal spectrum. As the duobinary data spectrum has a null at ½ the bit rate, the amount of high-frequency emphasis is greatly reduced when compared to uncoded NRZ signaling. Additionally, nulls that occur in the transfer function of the channel are predominantly located towards the higher end of the frequency spectrum. Therefore, the compact spectrum of duobinary signaling provides a distinct advantage.

The FIR filter used for pre-emphasis is indeed an indispensable element of the design as it allows shaping the signal response towards the desired duobinary format while respecting the variations in specific channel characteristics. If we define the complex transmission frequency response of the backplane as $H_{CH}(\omega)$, then the required filter response $H_{FIR}(\omega)$ becomes:

$$H_{\mathrm{FIR}}(\omega) = \frac{H_{\mathrm{D}}(\omega)}{H_{\mathrm{CH}}(\omega)}$$

where $H_D(\omega)=1+\exp^{(-j\omega T)}$, which is the frequency response of a duobinary filter. In general, an ideal $H_{FIR}(\omega)$ filter has many coefficients. A practical filter will be truncated to only a few filter taps, which are required to suppress the pre-cursor and 2 or 3 post-cursor symbols.

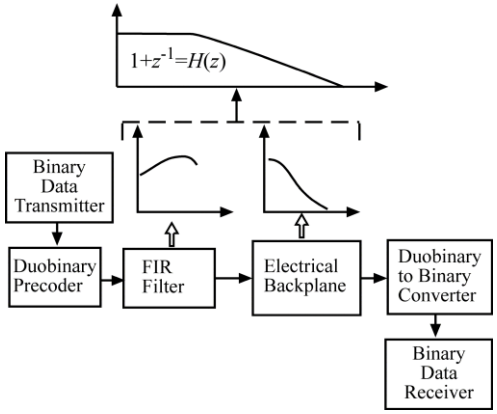

Figure 5: Duobinary transmission system architecture.

The low-pass characteristic of duobinary PR signaling goes beyond the compression of spectrum within the low-loss region of the channel. The limited bandwidth requirement is also beneficial to the design of the front-end components of the transceiver. These components can also be considered as part of the channel response. Effectively this relaxes the integrated circuit bandwidth requirements, opening possibilities to use a broader range of silicon processes and relaxed impedance matching requirements. Similar considerations apply to channel design, such as the mitigation of differential skew. Differential skew converts higher frequency components to common-mode, effectively resulting in a low-pass characteristic for the differential mode. This low-pass characteristic can become a part of the duobinary response, relaxing the design criteria even for the highest symbol rates.

When comparing duobinary to PAM4, a final point to consider is that the redundant information that exists in duobinary signaling is not actually used in the detection process as we have outlined so far. There is, in fact, additional information that can be extracted from limited permissible data transitions. Error detection is briefly discussed by Pasupathy in [9]. It is very possible that some limited error detection can be implemented that would further improve the BER performance of duobinary signaling.

3. Custom ASIC design for 50+ Gb/s duobinary link

To support next generation serial 56 Gb/s transfer rates across a backplane there are no off-the-shelf components available. For this speed custom transmitter and receiver chips were designed. The transmitter consists of a feed-forward equalizer that shapes the transmission channel (backplane + additional loss in connecting cables etc.) to a duobinary shape. The receiver translates the duobinary input data into 4 quarter-rate NRZ streams, using a novel architecture, which is demonstrated to work up to 56 Gb/s.

3.1 Feed-forward equalizer

3.1.1 Introduction to feed-forward equalization

Feed-forward equalization (FFE) is one of the most common equalization techniques used in serial data paths. Generally, the FFE equalizes voltage by summing of voltage levels from multiple controlled taps representing the weight of the preceding and following voltage level samples. The summation is continuous over the entire waveform. Compared to other equalization techniques such as decision-feedback equalization (DFE), FFE equalization techniques only correct voltage levels of the transmitted waveform with information about the analog waveform itself. Therefore, the chip design is less complicated and requires fewer gates, thus, in most cases the chip designed using FFE is less expensive and more power efficient.

3.1.2 Implementation of the 5-tap FFE

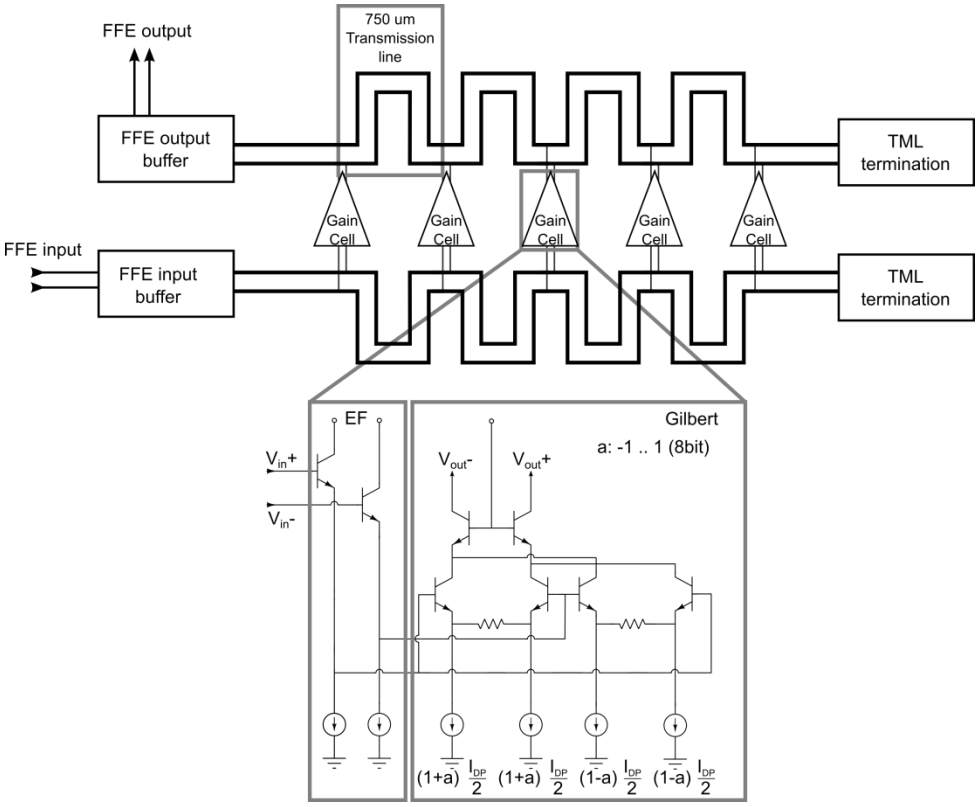

Figure 6: 5-tap FFE block diagram.

Figure 6 shows the topology of the 5-tap FFE. The gain cell is a variable gain amplifier. It is implemented as a Gilbert cell, and is the critical sub-block in the FFE design. These cells realize the equalization coefficients or tap weights. Therefore, each gain stage can be considered as an analog multiplier with a high-speed data input and a low-speed control signal. In addition, by keeping the summed current of both differential pairs

constant, the current flowing through the transmission line termination resistor is constant, thus keeping the bias voltage of the FFE output buffer constant.
As shown in figure 6, the delay of each tap is implemented by high-impedance sampling of a transmission line at the input of the gain cells. At the output a high-impedance addition on the transmission line is performed. The overall delay of each tap is defined as the sum of the delay at the input and at the output.
On-chip transmission lines (TML) have been used in various FFE's as low-loss delay elements, because of their very high bandwidth and low power dissipation [19]. In this FFE design, each meandered transmission line section in between the gain cells is 750 um long and is designed to have a 50 Ohms characteristic impedance. Meanwhile, the input and output TML are terminated by on-chip resistors.

3.1.3 Parameter optimization

Finding the optimal parameters for a duobinary channel in a 5-dimensional space is challenging. However, the methodology proposed in this section provides a good starting point. It is based on frequency-domain measurements which can be done quickly and accurately. The response of each tap is measured at maximum gain (5 measurements). These measurements are converted into the time-domain by calculating the impulse response. Figure 7 shows that the 5 taps are separated in time by a delay of 12.4 ps, corresponding to the delays introduced by the transmission lines. Also one can see that the later taps have a lower output power, which is caused by the loss across the transmission line.

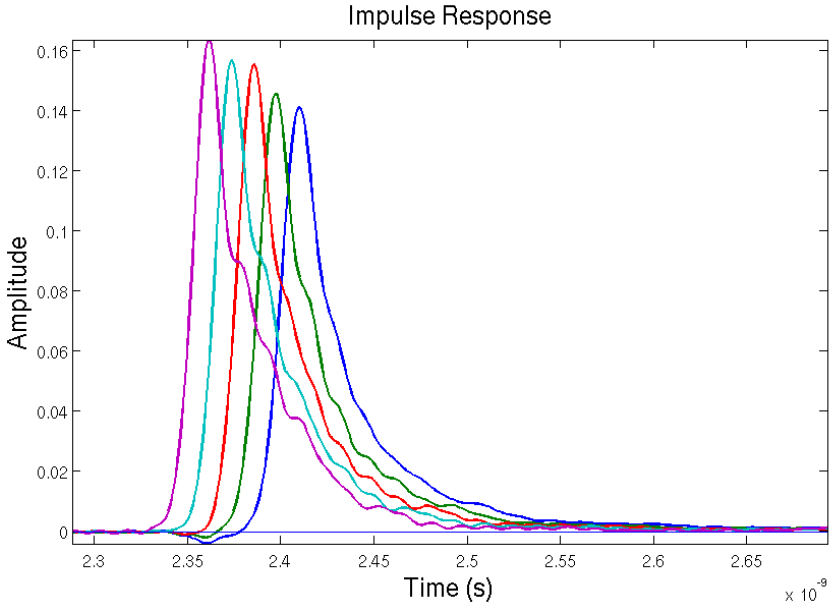

Figure 7: Overlapping impulse responses of the FFE.

From the Gilbert cell implementation one can assume the gain of the taps is linear. As a result the FFE output can be calculated as a linear combination of the impulse responses of the taps. The complete system can be modeled by the convolution of the channel

impulse response and the taps or by multiplying them in the frequency-domain and recalculating the impulse responses.
Using the measured impulse responses, a least-square-error (LSE) fit to the idealized duobinary response is done. The idealized response consists of two bit-spaced narrow sinc pulses. The LSE fit matches the 5 normalized FFE parameters as well as the optimal timing. In this way, it selects the optimal number of pre- and post-cursors in the FFE. The result of such a fit is shown in figure 8.

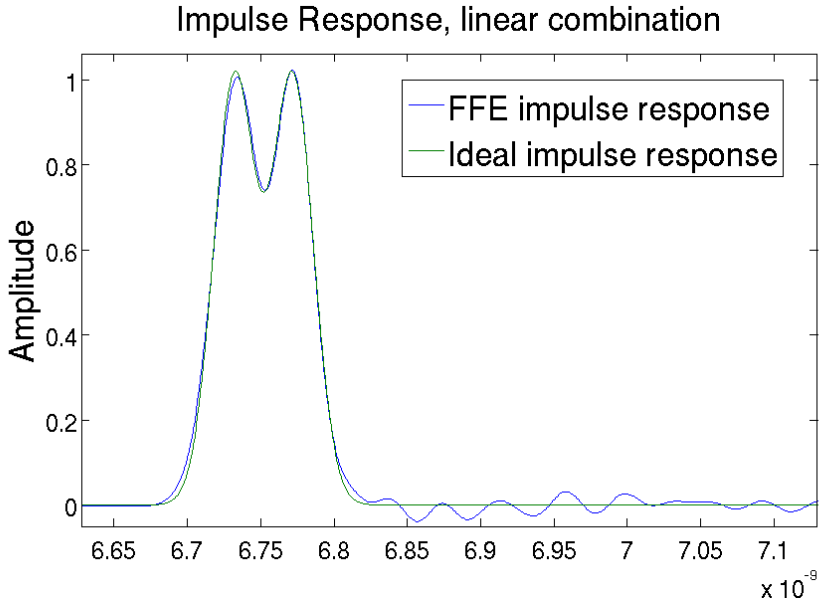

Figure 8: Fitting the FFE output to the ideal duobinary response.

It is clear that the FFE is capable of matching the main cursors of the duobinary channel. There is some remaining error which will result in extra inter symbol interference, which is evident from the eye-diagram of figure 9.

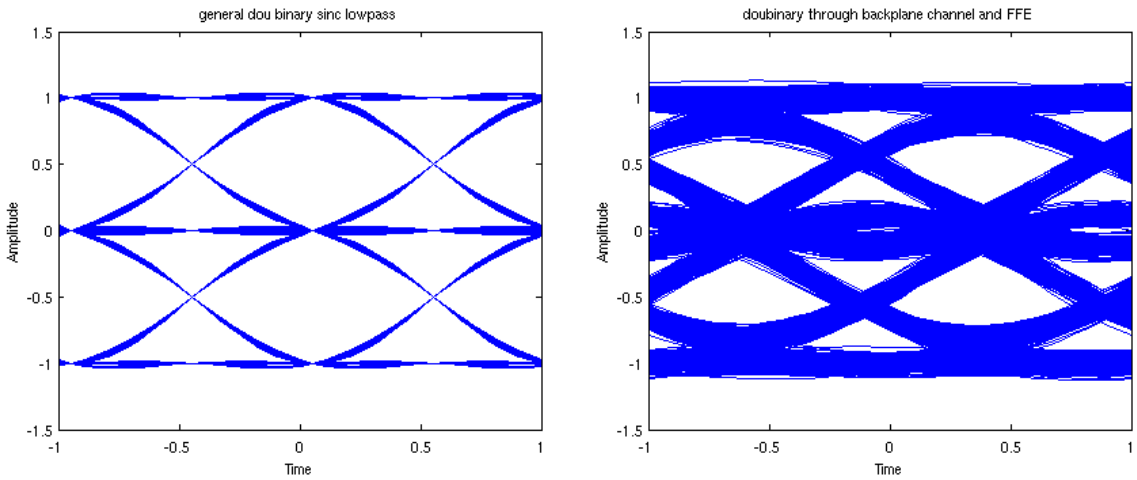

Figure 9: Simulated eye-diagram of the ideal (left) and fitted (right) duobinary signal.

3.2 Duobinary receiver

3.2.1 Introduction to duobinary receivers

The first duobinary-to-binary converter proposed by Lender [8] comprised a full-wave rectifier. Although this is a viable solution, it is not trivial to scale it up to the multi-gigabit per second range. However, in 2005 Sinsky et al. [11] demonstrated an innovative pseudo digital approach, shown in figure 10, which could potentially be very fast.
To further increase the speed capability of this duobinary receiver, an on-chip de-multiplexing step is added before the XOR operation. This new architecture is shown in figure 11. Sampling the data before decoding the duobinary signal introduces some extra challenges, because the data is highly unbalanced (the ratio of 0's to 1's is closer to 75% compared to the expected 50%). Implementing this technique in a fast SiGe BiCMOS process allowed us to reach record breaking speeds of 56 Gb/s across a backplane.

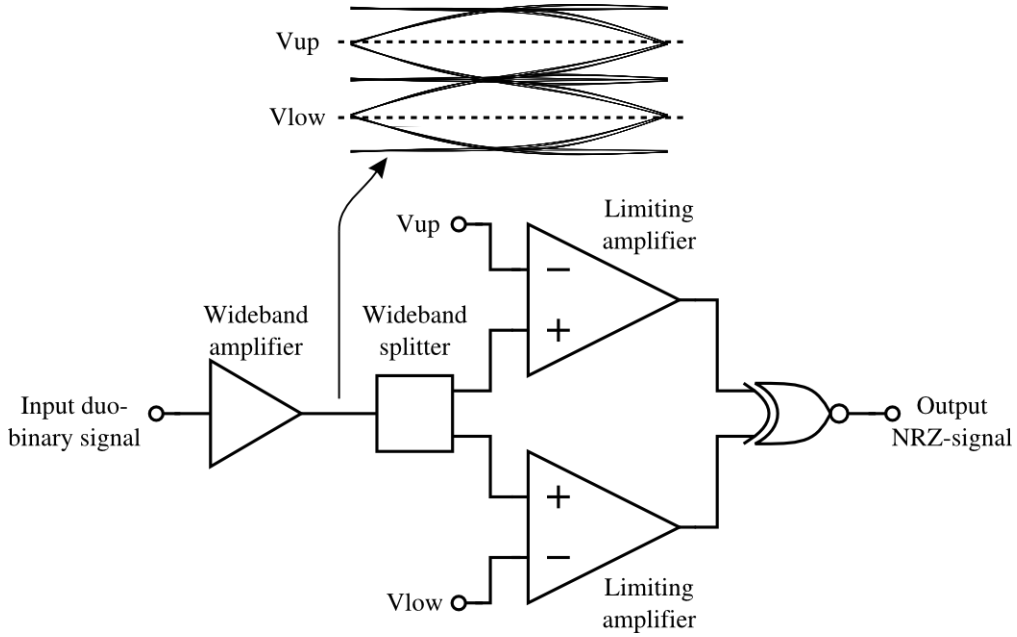

Figure 10: First proposed pseudo digital duobinary-to-binary converter.

After the duobinary decoding, the data is again de-multiplexed to reduce the output bit rate and get a re-timed signal at the output. The final data output is a quarter-rate stream.

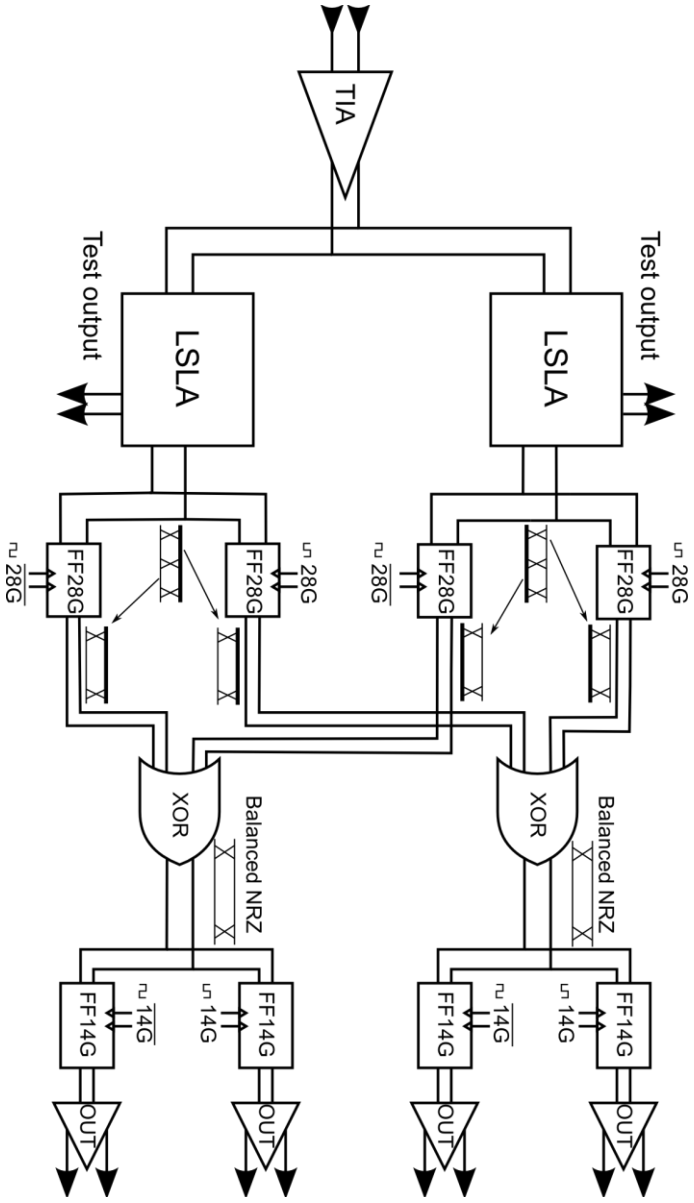

Figure 11: Implemented high-speed receiver architecture.

3.2.2 Implementation of the sub blocks

The most important blocks designed are the input buffer, the level-shifting limiting amplifier (LSLA) and the fast re-timer stage. The trans-impedance amplifier (TIA) used as input buffer is explained in [20], it has sufficient bandwidth to receive the 56 Gb/s duobinary signal on-chip and distribute it to the LSLA's.

The LSLA shown in figure 12 consists of 2 traditional current-mode logic (CML) gain stages, 2 level-shifting stages and a buffer connecting to the sampling stage and a buffer connected to an output driver to be able to display the upper or lower eye-patterns off-chip.

The first stage of the LSLA is used to shift the data up (or down) with a 7-bit digital controlled level (plus 1 sign bit) to retrieve the upper eye-pattern from the duobinary

stream. Due to the unbalance in the recovered eye-pattern (ideally 25% top and 75% bottom mark densities) the crossing will not be in the middle of the eye-pattern anymore after amplification. To overcome this, a second level-shifting stage is added which has coarse control over the eye-pattern crossing.

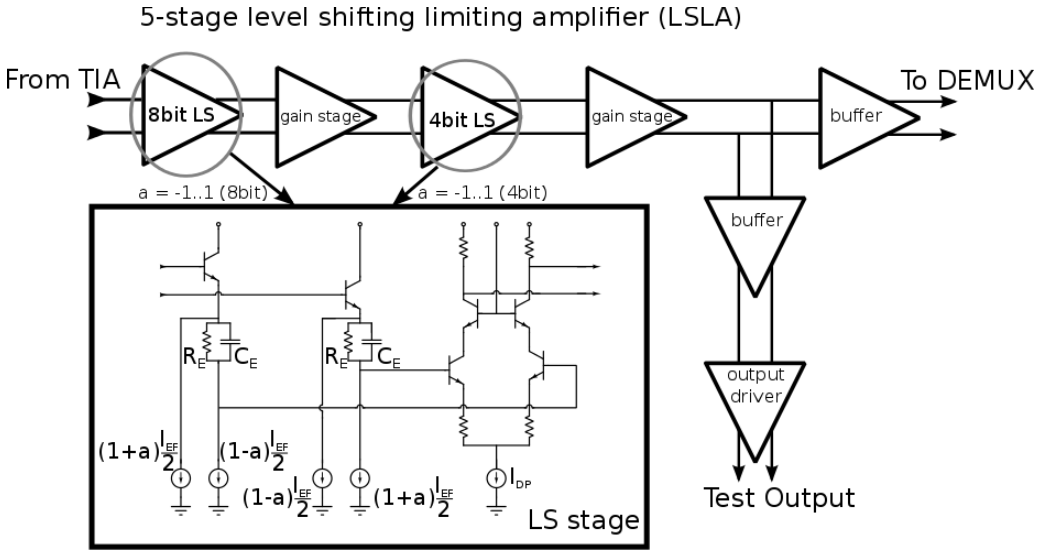

Figure 12: Block diagram of a LSLA, including schematic of the level-shifting stages.

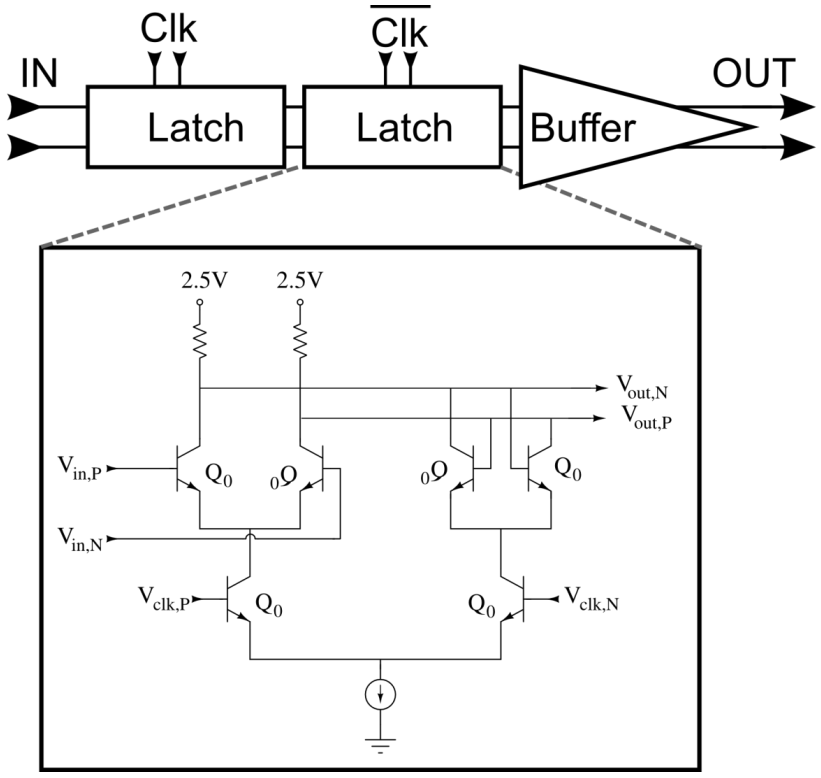

Figure 13: Block diagram of the high-speed sampling stage, including schematic of the latch.

The high-speed sampling stage consists of two CML latch stages with antiphase differential half-rate clock inputs (at 28GHz). When the clock is high, the sampling stage acquires the data and makes the decision on whether the input is a 1 or a 0, when the clock is low, the data gets regenerated to the digital CML levels. This stage is succeeded by another latch stage which samples the regenerated data to make sure the output of the sampling stage is a digital half-rate CML signal. This is illustrated in the block diagram of figure 13. Underneath the block diagram the schematic of the latch is shown. The load resistor in each latch stage is 55 Ohms. To have about 400 mV differential swing for the XOR gate, the bias current is around 4 mA for each latch working at 2.5 V.
In total there are 4 sampling stages on the receiver die, as shown in figure 11. The clock is distributed in such a way that 2 stages sample at the rising edge and the other 2 stages sample at the falling edge, which effectively divides the bit rate by 2. Each half bit rate signal is then processed by the XOR gates to decode the duobinary data. After decoding, an extra de-multiplexing stage is added resulting in a quarter-rate re-timed differential output.

4. Eye-pattern and BER measurements

4.1 Measurement setup

For system-level evaluation and validation test boards were designed. The TX and RX chips are flip-chip mounted onto these test boards. The data generator is connected to the TX board using coax cables. All coax cables used in the measurement setup are 20 cm long. Each of the coax cables adds a certain amount of loss to the total link loss. The coax cables used have about 1.05 dB of loss at 28GHz.
The complete measurement setup is shown in figure 14. The signal goes through an FFE which pre-shapes the frequency content of the signal at the output of the TX. Figure 15 shows the losses added by the TX board. At 28 GHz the TX board adds 5.6 dB of losses.

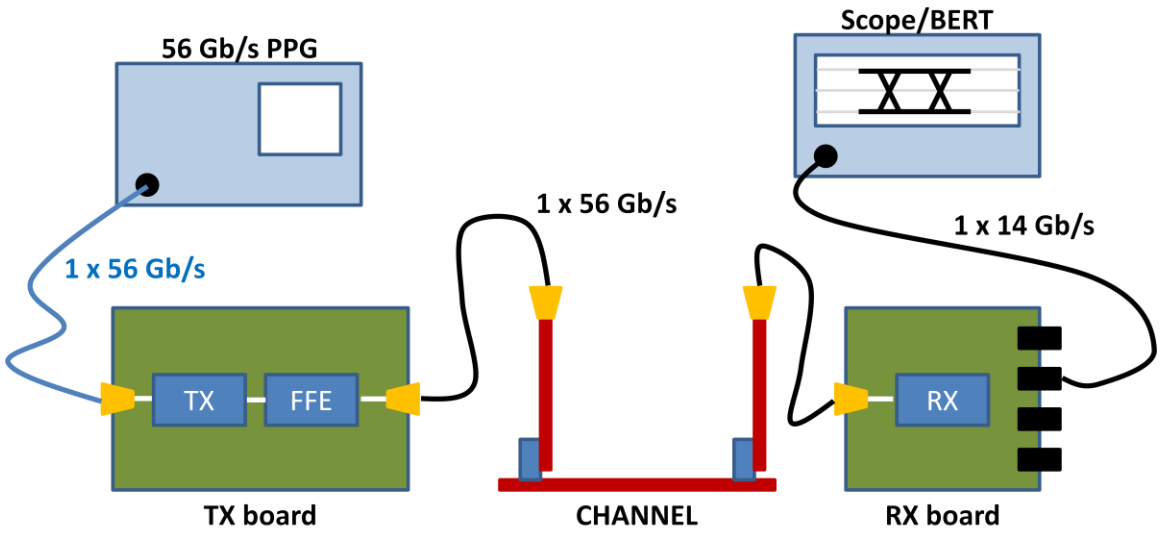

Figure 14: Measurement setup.

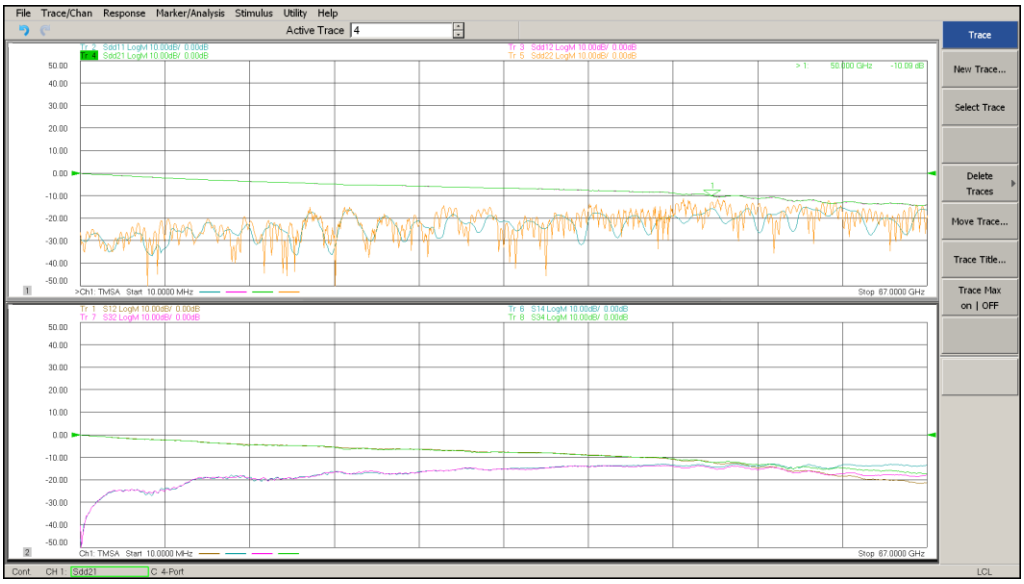

Figure 15: TX board losses.

The output of the TX board is connected to the input of the channel using a pair of coax cables, and the output of the channel is connected to the input of the RX board using a second pair of coax cables. The amount of losses added by the input lines of the RX board is shown in figure 16. A total of 3.8 dB of losses are added by the RX board at 28 GHz. Finally, the output of the RX boards is connected to the scope/BERT. The losses added by the different components in the measurement setup are summarized in table 1. At 28 GHz a total of 11.5 dB of losses are added by the coax cables and the TX and RX boards.

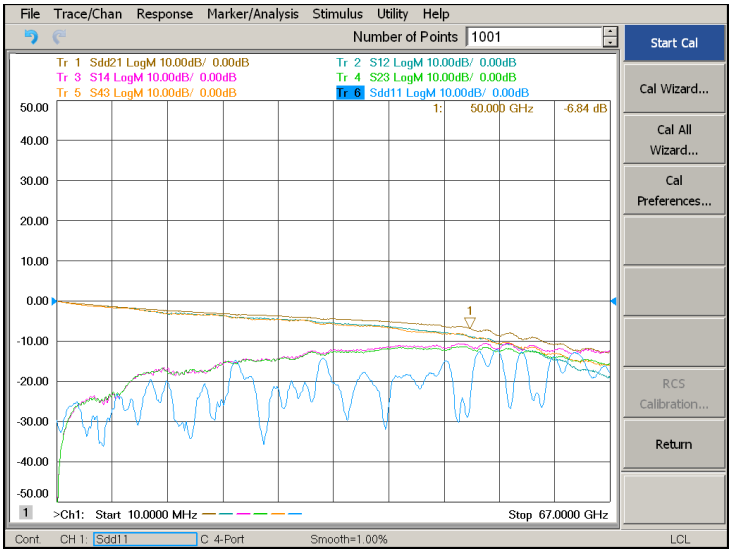

Figure 16: RX board losses.

Back-to-back measurements show a vertical and a horizontal eye-opening at the input of the RX board of 57 mV and 12 ps (0.67 UI) respectively. This results in error-free (BER < 1E-12) transmission at 56 Gb/s, the eye-diagram is shown in figure 17. The back-to-back link has a loss at the Nyquist frequency (28 GHz) of 11.5 dB introduced by the boards and cables connecting the boards.

COMPONENT	LOSSES
TX board	5.60 dB
Coax TX board to channel	1.05 dB
Channel losses	IL [dB]
Coax channel to RX board	1.05 dB
RX board	3.80 dB
Total losses	IL + 11.5 dB

Table 1: Total amount of losses added by measurement environment.

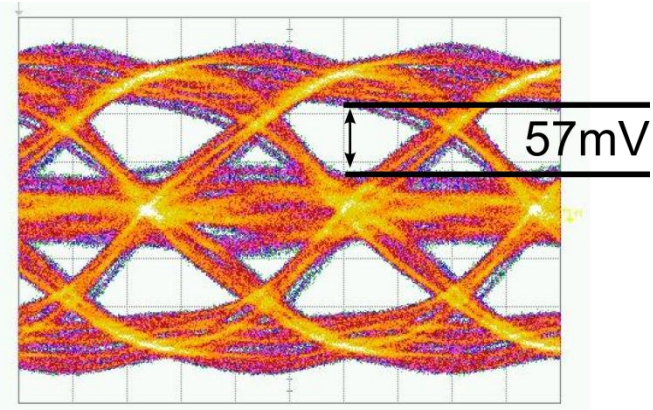

Figure 17: 56 Gb/s output eye-diagram of the transmitter.

4.2 Measurements on ExaMAX® demonstrator

To validate the chip design and to demonstrate 56 Gb/s duobinary transmission over a backplane, measurements have been carried out on a demonstrator using the state-of-the-art ExaMAX® connector system (see figure 18).
The demonstrator consists of 2 daughter cards plugged into a backplane using 2 ExaMAX® connectors. The backplane has 24 layers and is 160 mil (4.1 mm) thick. The daughter cards have 18 layers and are 94 mil (2.4 mm) thick. The trace lengths on the backplane vary between 1.7 in and 26.75 in. The trace length on the daughter cards is 6 in. This results in a minimum total interconnection length of 13.7 in (35 cm) + 2 connectors. The material used for building the backplane and daughter cards is Megtron 6. The backplane traces have a loss of about 1.3 dB per inch at 28 GHz. The insertion loss of the 13.7 in channel is shown as the red line in figure 19. The 13.7 in channel insertion loss at 28.8 GHz is about 28 dB. As explained above the measurement setup adds an additional 11.5 dB of losses at the Nyquist frequency. The total losses of the channel + measurement setup are shown as the blue line in figure 19.

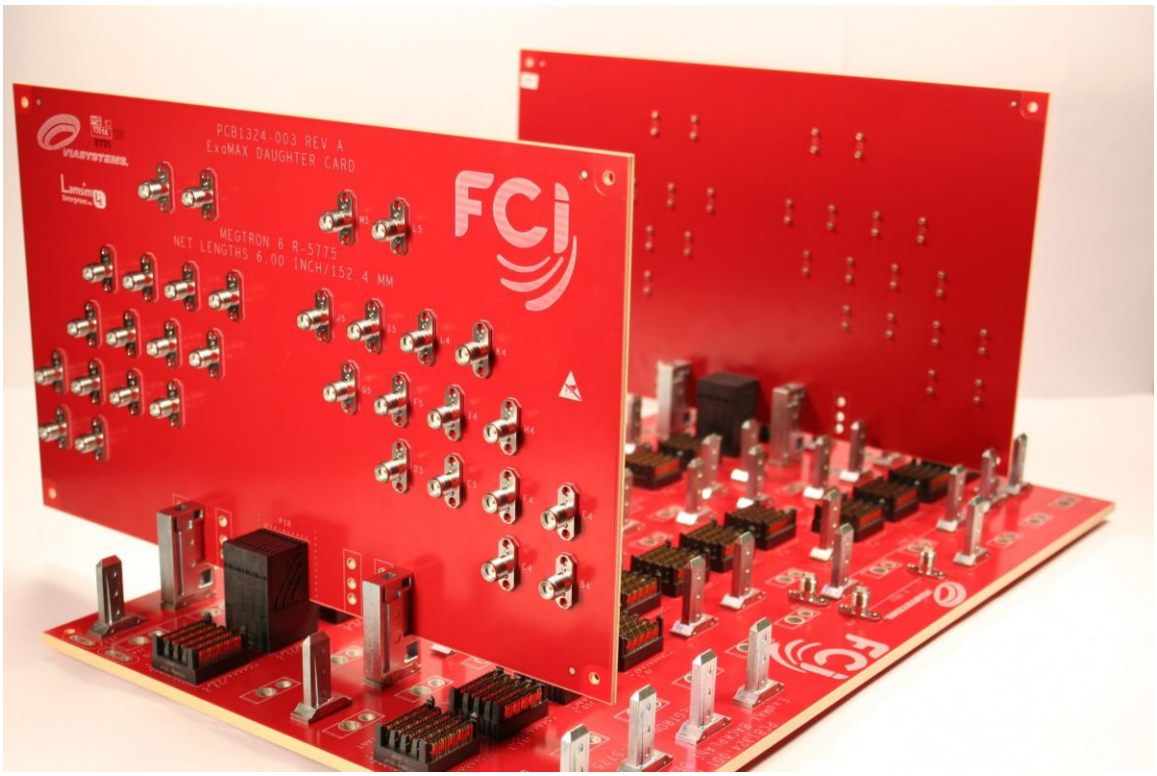

Figure 18: ExaMAX® backplane demonstrator.

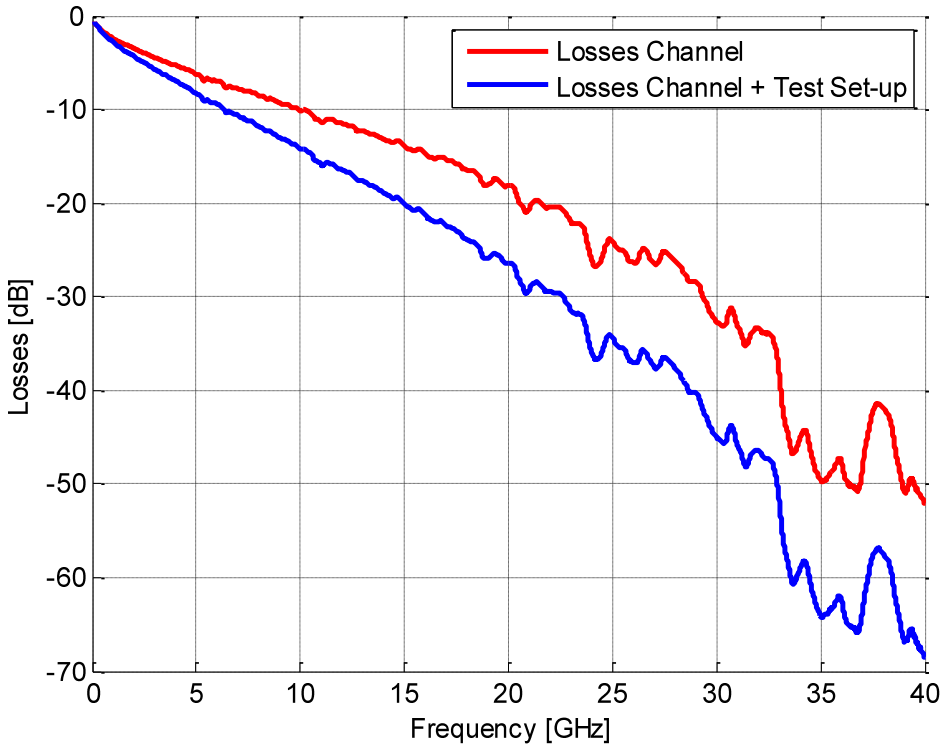

Figure 19: Losses 13.7 in backplane channel only (red) and total losses of backplane channel + test setup (blue).

Measurements started at 40 Gb/s on the shortest link (13.7 in, 35 cm). The loss at the Nyquist frequency is 28.8 dB, resulting in a vertical and a horizontal eye-opening of 18.2 mV and 15 ps (0.6 UI) respectively, compared to the maximum output eye-pattern at the transmitter having an eye-opening of 93.4 mV and 19.1 ps (0.76 UI) at 40 Gb/s. Both eye-patterns are shown in figure 20. This results in error-free (BER < 1E-12) transmission when connected to the duobinary decoder.

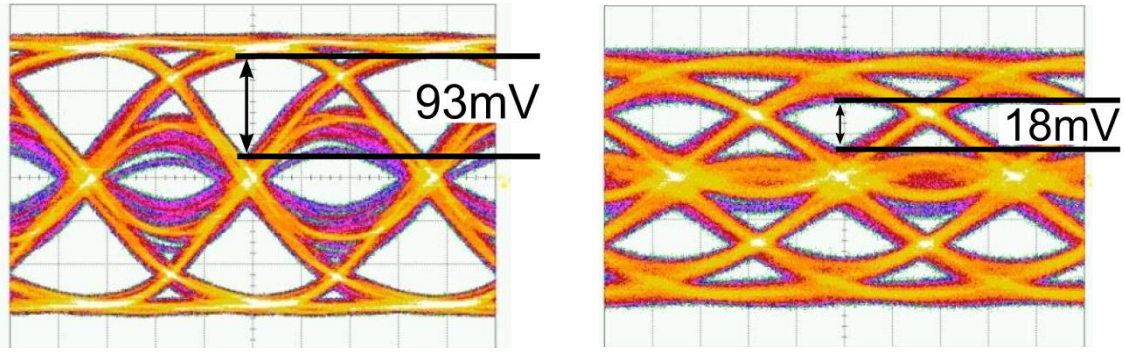

Figure 20: 40 Gb/s output eye-pattern at the transmitter (left) and after a 13.7 in backplane channel (right).

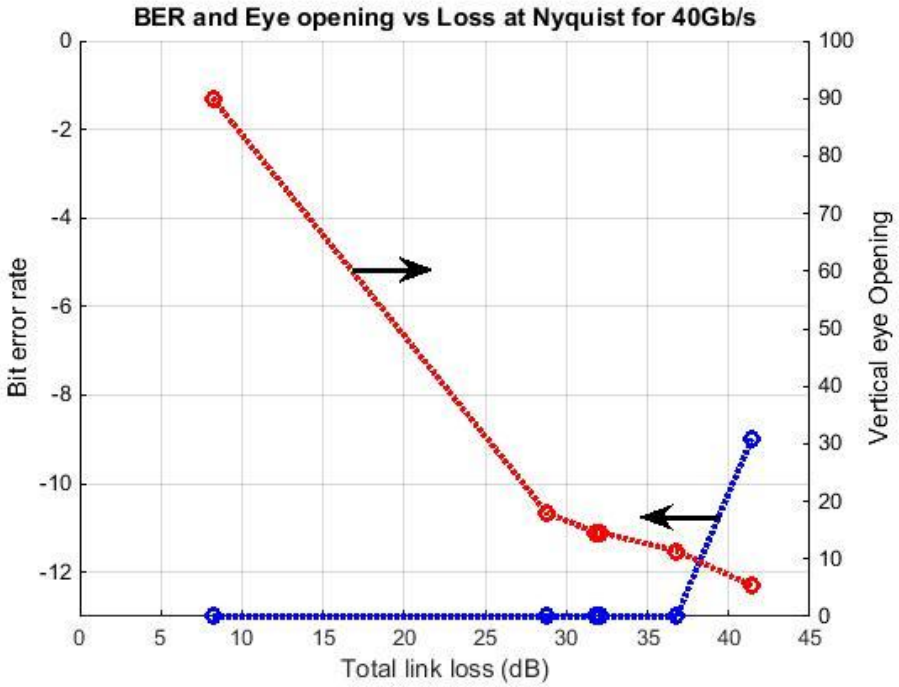

Figure 21: Chart showing the BER (blue) and the vertical eye-opening (red) as a function of the loss at the Nyquist frequency for a 40 Gb/s signal measured across the ExaMAX® backplane.

In figure 21 it is shown that a total loss (backplane + test setup) at the Nyquist frequency of up to 36.8 dB can be received error-free (BER < 1E-12), and up to 41.4 dB with a BER

below 5E-9, which is considered OK for a link with FEC in the current 25 Gb/s IEEE 802.3bj standard. The 36.8 dB loss corresponds to a total channel length of 22 in, while the 41.4 dB loss corresponds to a total channel length of 27 in. At 36.8 dB and 41.4 dB the vertical eye-opening are 11 mV and 5 mV respectively, as shown in figure 22.

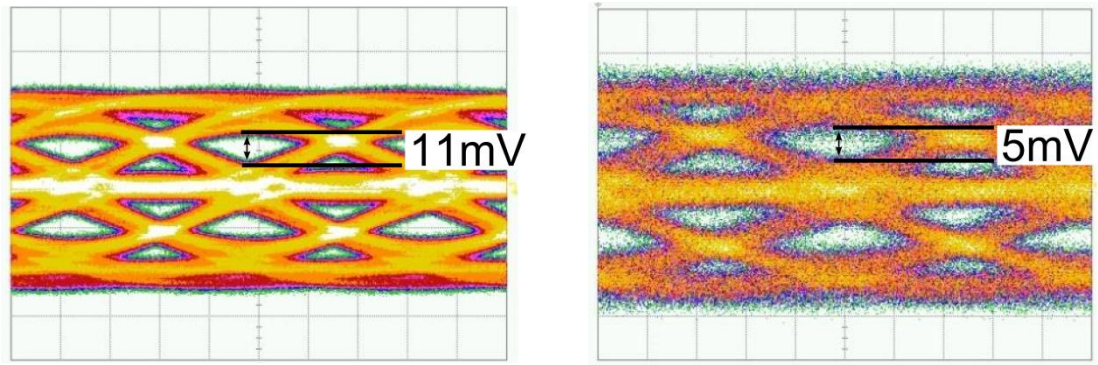

Figure 22: Eye-diagrams of the 40 Gb/s duobinary signal across a 22 in (left) and a 27 in (right) backplane channel.

Moving towards higher speeds leads to more frequency-dependent loss. At 50 Gb/s the signal after a 13.7 in backplane channel was still received error-free (BER < 1E-12), with an eye-opening of 6.8 mV as shown on the left in figure 23.
By increasing the speed to 56 Gb/s the loss at the Nyquist frequency increases further, and the vertical eye-opening at the input of the receiver decreases to about 6 mV as shown on the right in figure 23. The BER obtained at 56 Gb/s is better than 5E-9, which is more than sufficient assuming FEC is applied.

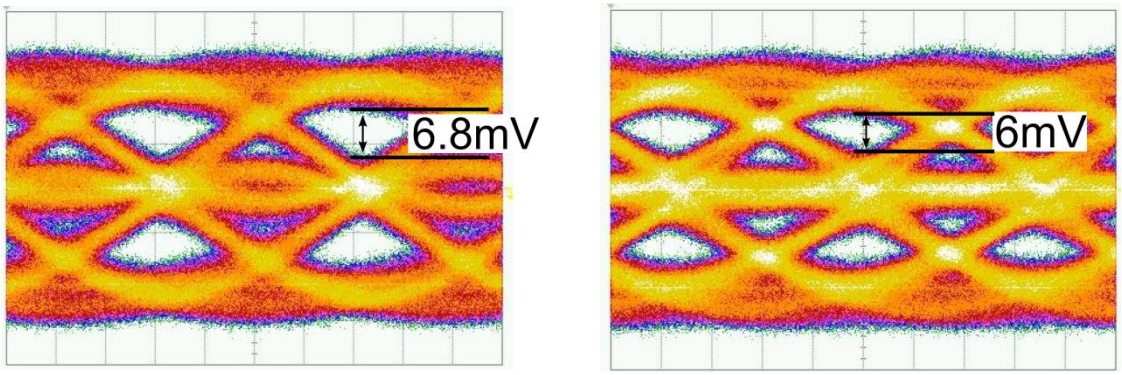

Figure 23: Eye-diagrams of the 50 Gb/s (left) and 56 Gb/s (right) signal after a 13.7 in backplane channel.

4.3 Design of active daughter cards

The performance of the transceiver chipset is limited by the total amount of losses that can be compensated for by the FFE. In the sections above we have shown that a total of 11.5 dB of losses at 28 GHz are added by the measurement setup. These losses are caused by the TX and RX test boards and by the coax cables needed to connect the different

boards together. These losses can be drastically reduced if we can directly mount the chips on the daughter cards in the backplane demonstrator.
The losses we recover this way can be used to achieve longer lengths on the backplane. If we could completely recover the 11.5 dB of losses at 28 GHz added by the current measurement setup, taking into account a loss of 1.3 dB/in at 28 GHz in the backplane traces, this would mean we could add 9 in to the backplane trace. The total interconnection length we could obtain this way would be 22.7 in (58 cm).
New active daughter cards are currently being designed where the duobinary chipset is directly mounted on the cards. These daughter cards will allow for the inclusion of crosstalk aggressors in future measurements. Updated measurement results using the new daughter cards will be presented at the conference.

5. Conclusions

In this paper it is shown that 56 Gb/s transmission across current backplane connectors and with mature chip technologies is possible using duobinary signaling and an FFE with only 5 taps, consuming less than 500mW from a 2.5V power supply. No other forms of equalization (such as e.g. continuous-time linear equalization) have been used in the measurement setup. Initial measurements have shown it is possible to transmit 56 Gb/s duobinary signals successfully over a channel with up to 40 dB of losses at the Nyquist frequency.

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References

[1] J.H. Sinsky et al, "42.8 Gbit/s PAM-4 data transmission over low-loss electrical backplane", *Electronics Letters*, vol. 48, no. 19, pp. 1206-1208, September 13, 2012.

[2] D. G. Kam, T. J. Beukema, Y. H. Kwark, L. Shan, X. Gu, P. K. Pepeljugoski, M. B. Ritter, “Multi-level Signaling in High-density, High-speed Electrical Links”, DesignCon 2008.

[3] Maes J., Guenach M., Hooghe K., Timmers M., "Pushing the limits of copper: Paving the road to FTTH", *2012 IEEE International Conference on Communications (ICC)*, pp. 3149-3153, 10-15 June 2012.

[4] H. Isono, H. Sakamoto, Y. Miyaki (Fujitsu Optical Components), T. Tanaka, T. Takahara, “Discrete Multi-Tone for 400GbE 10km reach”, www.ieee802.org/3/bs/public/14_05/isono_3bs_01_0514.pdf .

[5] Beukema T., "Design considerations for high-data-rate chip interconnect systems", *IEEE Communications Magazine*, vol. 48, no. 10, pp 174-183, October 2010.

[6] R. Kollipara, B. Chia, C. Yuan, J. Zerbe, G. Patel, T. Cohen, B. Kirk, “Practical Design Considerations for 10 to 25 Gbps Copper Backplane Serial Links”, DesignCon 2006.

[7] Singh A., Carnelli D., Falay A., Hofstra K., Licciardello F., Salimi K., Santos H., Shokrollahi A., Ulrich R., Walter C., Fox J., Hunt P., Keay J., Simpson R., Stewart A., Surace G., Cronie H., "A pin- and power-efficient low-latency 8-to-12Gb/s/wire 8b8w-coded SerDes link for high-loss channels in 40nm technology", Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International , pp. 442-443, 9-13 Feb. 2014.

[8] A. Lender, “The duobinary technique for high-speed data transmission”, IEEE Trans. Communications Electronics, vol. 82, no. 2, pp. 214-218, May 1963.

[9] S. Pasupathy, “Correlative Coding: a bandwidth efficient signaling scheme", Invited paper, IEEE Communications Society Magazine, vol. 15, No. 4, pp. 4-11, July 1977.

[10] P. Kabal, S. Pasupathy, ``Partial-response signaling", IEEE Transactions on Communications, vol. COM-23, No. 9, pp. 921-934, Sept. 1975.

[11] J.H. Sinsky, M. Duelk, A. Adamiecki, "High-speed electrical backplane transmission using duobinary signaling", IEEE Transactions On Microwave Theory and Techniques, vol. 53, no. 1, pp. 152-160, Jan. 2005.

[12] J.H. Sinsky et al, "39.4-Gb/s Duobinary Transmission Over 24.4 m of Coaxial Cable Using a Custom Indium Phosphide Duobinary-to-Binary Converter Integrated Circuit", IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 12, pp. 3162-3169, Dec. 2008.

[13] J. Lee, N. Kaneda, T. Pfau, A. Konczykowska, F. Jorge, J. Dupuy, and Y. Chen, "Serial 103.125-Gb/s Transmission over 1 km SSMF for Low-Cost, Short-Reach Optical Interconnects", in Optical Fiber Communication Conference: Postdeadline Papers, (Optical Society of America, 2014), paper Th5A.5.

[14] Lyubomirsky I., "Quadrature Duobinary for High-Spectral Efficiency 100G Transmission", Journal of Lightwave Technology, vol. 28, no. 1, pp. 91-96, January 2010.

[15] Yonenaga K., Kuwano S., "Dispersion-tolerant optical transmission system using duobinary transmitter and binary receiver", Journal of Lightwave Technology, vol. 15, no. 8, pp. 1530-1537, Aug 1997.

[16] D. van Veen, V. E. Houtsma, A. Gnauck, P. Iannone, “40-Gb/s TDM-PON over 42 km with 64-way Power Split using a Binary Direct Detection Receiver,” in European Conference and Exhibition on Optical Communication, OSA Technical Digest (online) (Optical Society of America, 2014), paper PD.1.4.

[17] D. van Veen, V. E. Houtsma, P. Winzer, and P. Vetter, "26-Gbps PON Transmission over 40-km using Duobinary Detection with a Low Cost 7-GHz APD-Based Receiver", in European Conference and Exhibition on Optical Communication, OSA Technical Digest (online) (Optical Society of America, 2012), paper Tu.3.B.1.

[18] Beyene W.T., Amirkhany A., "Controlled Intersymbol Interference Design Techniques of Conventional Interconnect Systems for Data Rates Beyond 20 Gbps", IEEE Transactions on Advanced Packaging, vol. 31, no. 4, pp. 731-740, Nov. 2008.

[19] A. Momtaz, M.M. Green, "An 80 mW 40 Gb/s 7-tap T/2-spaced feed-forward equalizer in 65 nm CMOS", IEEE J. Solid-State Circuits, Vol. 45, No. 3, Mar. 2010.

[20] De Keulenaer T., Ban Y., Li Z., Bauwelinck J., "Design of a 80 Gbit/s SiGe BiCMOS fully differential input buffer for serial electrical communication", IEEE ICECS, 2012