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DC-bus Voltage Controllers for a Three-Phase Voltage-Source Inverter for Distributed Generation

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Abstract An important function of the bus voltage controller of voltage-source inverters (VSI) for distributed generation (DG) applications is to control the balance between ac and dc power. Nevertheless is the bus voltage controller not the critical part of the control of the VSI. Therefore it is justified that little attention is paid to the design of this bus voltage controller what can be seen in literature. However, this controller can (negatively) influence the behaviour of the VSI. In three-phase systems a ripple can exist in the bus voltage due to unbalance or harmonics present in the grid voltage or current. This ripple can interact with the bus voltage controller which can have negative consequences on the injected current. Also the timing of updating the output of the bus voltage controller can have consequences on the waveform distortion which can result in oscillations. In this paper the focus is on the timing of updating. An overview of three possible bus voltage controllers is given. The response of the different implementations of dc-bus voltage controllers during a transient is simulated.

Keywords

model, digital control, three phase voltage-source inverter (VSI), distributed generation, neutral-point-clamped VSI

1. Introduction

An important function of the dc-bus voltage controller of VSI for DG applications is to control the balance between the power at the grid-side and the power at the dc side. The dc-bus voltage controller outputs the fundamental input conductance which results in the reference current. The bus voltage controller is not the critical part of the control of the VSI because balancing the input and output power is a slow process and the (large) capacitor at the dc-bus serves as a buffer. Therefore it is justified that little attention is paid to the design of this bus voltage controller which can be seen in literature [**?**, 1–9]. However this controller can (negatively) influence the behaviour of the VSI. For three-phase systems under symmetric operation (three-phase symmetrical voltage and current) there is no ripple at the dc-bus voltage as opposed to single-phase systems where a ripple at double grid frequency exists. If an unbalance (in voltage or current) or harmonics are present in a three-phase system, a ripple occurs at the dc-bus voltage. This ripple can interact with the bus voltage controller if it was not designed to handle a distortion in the dc-bus voltage [10]. The interaction can result in harmonics in the injected current. The bus voltage controller is usually a PI-controller with a randomly chosen sample frequency [2], [11–14]. The sample frequency is usually chosen low in order to reduce the effect of ripple on the bus voltage. By choosing a low sample frequency the response of the bus voltage controller will also be slow. This can result in high over- or undervoltages of the bus voltage in case of severe faults. Another method to improve the ripple rejection is to sample at the zero-crossings of the ripple. By doing so the ripple becomes a hidden oscillation for the bus voltage controller [15]. In [16] and [17] a low pass filter is used to filter out the ripple. Adding a low pass filter degrades the transient response of the dc-bus voltage control and causes a larger variation of dc-bus voltage in the transient state.

Another aspect of the bus voltage controller is the timing of updating the output. The output of the bus voltage controller can be synchronised with the zero-crossings of a phase voltage [?, 1–9]. This method will result in a step in the amplitude in the other two phases of the injected current if the output is changed due to a transient in the power balance. This step in the amplitude will negatively influence the grid voltage. This can be prevented by changing the timing of updating the output of the bus voltage controller.

A balance has to be found between the reaction speed of the bus voltage controller and the resistance against variations of bus voltage on the bus voltage controller. Increasing the reaction speed by increasing the sample and update frequency of the bus voltage controller can lead to harmonics in the injected current in case of unbalance or harmonics in the grid voltage or current. The timing of updating the output of the bus voltage controller can also be important. In the following the emphasis will be placed on the timing of updating.

This paper will address three different bus voltage controllers:

- 100 Hz bus voltage controller
- 100 Hz bus voltage controller with delayed updates at the zero-crossing of the grid voltage
- 1 kHz bus voltage controller

The advantages and disadvantages of the different bus voltage controllers will be given. The transient behaviour of these three bus voltage controllers will also be studied.

2. The Voltage Source Inverter

There are two possibilities to interface the DG connected inverter to a three-phase four-wire system, which is typically the topology of a low-voltage distribution network. One possibility is to have a three-wire inverter which is connected to the four-wire system by means of a Δ/Y_g isolation transformer. Since the isolation transformer is heavy and expensive, it is not desired in many applications. The second possibility is using a transformerless four-wire inverter.

There are generally two types of four-wire inverter topologies: three-leg with split dc bus and four-leg. The three-phase three-leg inverter with split dc-bus enables to implement a three-phase four-wire system with a neutral point. Compared to a three-phase three-wire system, it does not require the isolation transformer to create a neutral point and it provides three-dimensional control. Compared to a three-phase four-leg topology, it saves two power switches and also reduces control complexity. A disadvantage of this topology is that the dc-bus capacitors have to be oversized because harmonic current can flow through these capacitors into the neutral wire.

Fig. 1 depicts the topology of the three-phase neutral-point clamped voltage-source inverter. The three-phase three-leg inverter has a split dc-bus where the top and bottom halves of the dc-bus are assumed to be evenly distributed such that half of the dc-bus voltage is over each capacitor. The dc-bus can be energized by a (small) DG-unit, like fuel cells, photovoltaic devices and wind turbines. The inverter outputs are connected to a three-phase second order L-C filter which attenuates high frequency components resulting from switching.

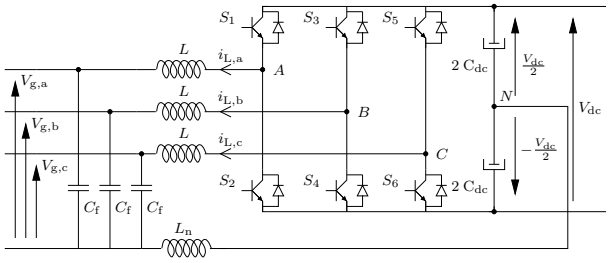


Figure 1: Topology of the three phase neutral-point-clamped voltage-source inverter

3. The Control Strategy

The control strategy for the three-phase neutral-point-clamped voltage-source inverter is depicted in Fig. 2. The dc-bus voltage controller provides the balance between the ac and the dc-bus power. The output of the bus voltage controller is the fundamental input conductance g_1 at the ac-side of the inverter. The input conductance is multiplied with the fundamental component of the grid voltage which results in the reference current. By doing so, the inverter provides a sinusoidal current. The phase angle of the fundamental component of the grid voltage is obtained by using a Phase Locked Loop (PLL).

The design of the current controller is based on the $\mathcal{Z}$-domain model of the inverter instead of the frequently used Laplace-domain model. The sampling of the signals and the dynamics of the pulse-width modulator are more accurately described by using a $\mathcal{Z}$-model which results in a better controller. The bandwidth of the current controller is 2 kHz which allows to track the 50 Hz reference current perfectly. The output of the current controller is added to the output of the duty-ratio feed-forward. The duty-ratio feed-forward branch is added to obtain a better disturbance rejection [18]. The result of this summation is the input of the PWM modulator which outputs the switching-signals for the inverter.

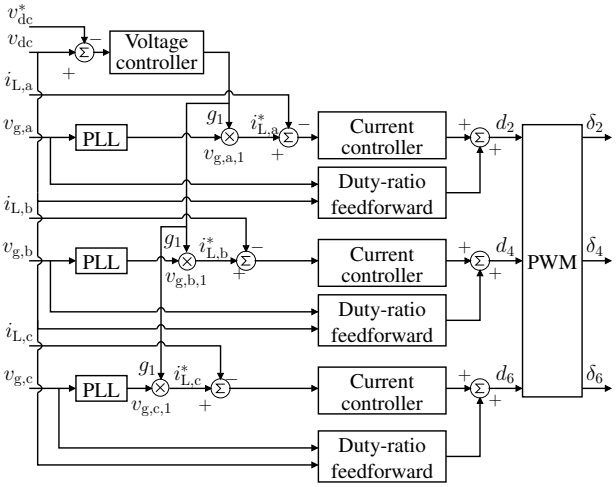


Figure 2: Control strategy for the three-phase neutral-point-clamped voltage-source inverter

4. Theoretical Model

In order to design the voltage controller, the transfer function of the input conductance to the output voltage has to be derived. This transfer function enables to design the output voltage controller in the $\mathcal{Z}$-domain. Fig. 3 depicts the model which is used to derive the transfer function of the input conductance to the output voltage. The instantaneous power $p_1(t)$ is given by:

$$\begin{aligned} p_1(t) = v_{\mathrm{g,a}}(t)\; i_{\mathrm{L,a}}(t) - \frac{L}{2}\,\frac{\mathrm{d}i^2_{\mathrm{L,a}}(t)}{\mathrm{d}t} \\ + v_{\mathrm{g,b}}(t)\; i_{\mathrm{L,b}}(t) - \frac{L}{2}\,\frac{\mathrm{d}i^2_{\mathrm{L,b}}(t)}{\mathrm{d}t} \\ + v_{\mathrm{g,c}}(t)\; i_{\mathrm{L,c}}(t) - \frac{L}{2}\,\frac{\mathrm{d}i^2_{\mathrm{L,c}}(t)}{\mathrm{d}t} \end{aligned} \qquad (1)$$

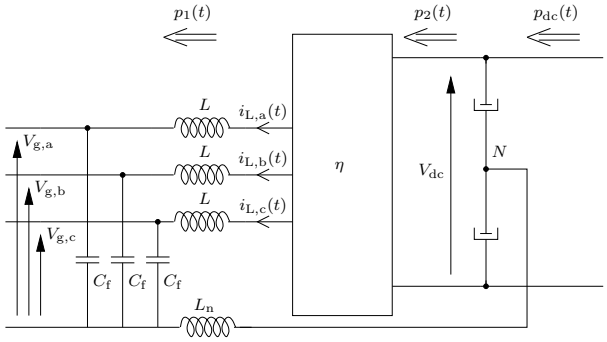


Figure 3: Model to derive the transfer function of the input conductance to the output voltage

The dc-power is given by:

$$p_2(t) = p_{\rm dc}(t) - \frac{C_{\rm dc}}{2}\,\frac{{\rm d}v_{\rm dc}^2(t)}{{\rm d}t} \tag{2}$$

The relationship between input and output power is given by:

$$p_1(t) \;=\; \eta\, p_2(t) \tag{3}$$

where η is the efficiency of the inverter.
It can be assumed that the zero sequence component of the injected current is very small which results in that the power in the neutral can be neglected. The control strategy which is used (cf Fig. 2) validates the assumption that the zero sequence component of the injected current can be neglected.
It is assumed that the current control works perfectly, such that the following relationship can be justified:

$$i_{\rm L,x}(t) \;\approx\; g_1(t)\, v_{\rm g,x}(t) \tag{4}$$

with x= phase a, b or c.
Equations (1)–(4) result in the following differential equation:

$$\begin{aligned} g_1(t)\, v_{\rm g,a}^2(t) - \frac{L}{2}\,\frac{{\rm d}(g_1(t)\, v_{\rm g,a}(t))^2}{{\rm d}t} \\ +g_1(t)\, v_{\rm g,b}^2(t) - \frac{L}{2}\,\frac{{\rm d}(g_1(t)\, v_{\rm g,b}(t))^2}{{\rm d}t} \\ +g_1(t)\, v_{\rm g,c}^2(t) - \frac{L}{2}\,\frac{{\rm d}(g_1(t)\, v_{\rm g,c}(t))^2}{{\rm d}t} \\ = \eta\, p_{\rm dc}(t) - \eta\,\frac{C_{\rm dc}}{2}\,\frac{{\rm d}v_{\rm dc}^2(t)}{{\rm d}t} \end{aligned} \tag{5}$$

In small-signal analysis each variable can be written as the summation of the steady-state value and a small excursion from this steady-state:

$$\begin{array}{ll} v_{\rm g,x}{=}V_{\rm g,x} + \hat{v}_{\rm g,x} & i_{\rm L,x}{=}I_{\rm g,x} + \hat{i}_{\rm g,x} \\ v_{\rm dc}{=}V_{\rm dc} + \hat{v}_{\rm dc} & p_{\rm dc}{=}P_{\rm dc} + \hat{p}_{\rm dc} \\ g_1{=}G_1 + \hat{g_1}. & \end{array}$$

where capitals are used for steady-state values and hatted small letters for small excursions from steady-state. The grid voltage in phase a, $V_{g,a}(t)$, in steady-state can be written as:

$$V_{\rm g,a}(t) = \sqrt{2}\, V_{\rm g,rms}\, \sin(\omega\, t) \tag{6}$$

where $V_{\rm g,rms}$ is the rms-value of the nominal amplitude of the grid voltage.
The small signal equation of (5) is obtained by subtracting the equilibrium of equation (3) with equation (5) which results in:

$$\begin{aligned} 2\, G_1\, [V_{\rm g,a}(t)\, \hat{v}_{\rm g,a}(t) + V_{\rm g,b}(t)\, \hat{v}_{\rm g,b}(t) \\ +V_{\rm g,c}(t)\, \hat{v}_{\rm g,c}(t)] + 3\, V_{\rm g,rms}^2\, \hat{g_1}(t) \\ -6\,\frac{L}{2}\, G_1\, V_{\rm g,rms}^2\,\frac{{\rm d}\hat{g_1}(t)}{{\rm d}t} - 2\,\frac{L}{2}\, G_1^2\, V_{\rm g,a}(t)\frac{{\rm d}\hat{v}_{\rm g,a}(t)}{{\rm d}t} \\ -2\,\frac{L}{2}\, G_1^2\, V_{\rm g,b}(t)\,\frac{{\rm d}\hat{v}_{\rm g,b}(t)}{{\rm d}t} - 2\,\frac{L}{2}\, G_1^2 V_{g,c}(t)\frac{{\rm d}\hat{v}_{g,c}(t)}{{\rm d}t} \\ -L\, G_1^2\, \hat{v}_{\rm g,a}(t)\,\frac{{\rm d}V_{\rm g,a}(t)}{{\rm d}t} - L\, G_1^2\, \hat{v}_{\rm g,b}(t)\,\frac{{\rm d}V_{\rm g,b}(t)}{{\rm d}t} \\ -L\, G_1^2\, \hat{v}_{\rm g,c}(t)\,\frac{{\rm d}V_{\rm g,c}(t)}{{\rm d}t} \\ = \eta\, \hat{p}_{\rm dc}(t) - \eta\, C_{\rm dc}\frac{{\rm d}(V_{\rm dc}(t)\, \hat{v}_{\rm dc}(t))}{{\rm d}t} \end{aligned} \tag{7}$$

A ripple on the bus voltage can cause the bus voltage controller to inject a current containing harmonics. In order to avoid this, the bandwidth of the voltage controller is set low. Averaging equation (7) over one period of the grid voltage is justified because the bandwidth of the voltage controller is small (25 - 100 Hz). When the bandwidth is larger, this averaging is no longer justified. The resulting equation will then have terms in $\hat{v}_{g,a}(t)$, $\hat{v}_{\rm g,b}(t)$ and $\hat{v}_{\rm g,c}(t)$ which are disturbances for the process "input conductance to the output voltage". When tuning a bus voltage controller having a larger bandwidth, care should be taken that the phase margin of the PI controller is large enough such that the process is stable under all conditions.
The averaging of equation (7) over one period of the grid voltage results in the elimination of the terms in $V_{g,x}(t)$:

$$\begin{aligned} 3\, V_{\rm g,rms}^2\, \hat{g_1}(t) - 6\,\frac{L}{2}\, G_1\, V_{\rm g,rms}^2\frac{{\rm d}\hat{g_1}(t)}{{\rm d}t} \\ = \eta\, \hat{p}_{\rm dc}(t) - \eta\, C_{\rm dc}\frac{{\rm d}(V_{\rm dc}(t)\, \hat{v}_{\rm dc}(t))}{{\rm d}t} \end{aligned} \tag{8}$$

In the Laplace domain, equation (8) can be written as:

$$\begin{aligned} \hat{v}_{\rm dc}(s) = \frac{3\, V_{\rm g}^2(s\, L\, G_1\; - 1)}{s\, \eta\;\, C_{\rm dc}\, V_{\rm dc}}\, \hat{g_1}(s) \\ +\frac{1}{s\, \eta\, C_{\rm dc}\, V_{\rm dc}}\hat{p}_{\rm dc}(s) \end{aligned} \tag{9}$$

This results in the transfer function of the input conductance to the output voltage (in per unit):

$$\frac{\hat{v}_{\rm dc}^{\#}(s)}{\hat{g_1}^{\#}(s)} = \frac{3\, V_{\rm g}^2}{\eta\, C_{\rm dc}\, V_{\rm dc}}\,\frac{1}{V_{\rm dc}^{\rm ref}\, Z^{\rm ref}}\,\frac{s\, L\, G_1 - 1}{s} \tag{10}$$

The zero $s \;=\; 1/(L\; G_1)$ can be neglected because it is situated at very high frequency (15 kHz) compared to the desired bandwidth of the output voltage controller (25 - 100 Hz). By neglecting this zero, the transfer function of the input conductance to output voltage (in per unit) can be written as:

$$\frac{\hat{v}_{\rm dc}^{\#}(s)}{\hat{g_1}^{\#}(s)} = \frac{-3\, V_{\rm g}^2}{s\eta C_{\rm dc} V_{\rm dc}}\,\frac{1}{V_{\rm dc}^{\rm ref} Z^{\rm ref}} \equiv \frac{-1}{\tau_v s} \tag{11}$$

with

$$\tau_v = \frac{\eta C_{\mathrm{dc}} V_{\mathrm{dc}} V_{\mathrm{dc}}^{\mathrm{ref}} Z^{\mathrm{ref}}}{3 V_{\mathrm{g}}^2} \tag{12}$$

The open loop transfer function of the output voltage controller in the $\mathcal{Z}$-domain can now be written as:

$$G_{\mathrm{tot}}(z) = \frac{T_{\mathrm{b,v}}}{2\,\tau_v} \frac{z+1}{z\,(z-1)} \tag{13}$$

where $T_{\mathrm{b,v}}$ is the sample period of the output voltage controller.
This transfer function can be used to tune the PI-controller of the bus voltage controller. The step response of the bus voltage controller is optimised by tuning the PI-controller using Sisotool in Matlab.

5. The DC-bus Voltage Controller

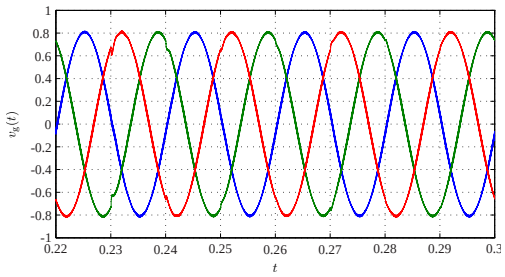
In the following section an overview of the different bus voltage controllers is given. In order to test the different bus voltage controllers, the following experiment is done. At t=220 ms the DG power is reduced from 2 kW to 660 W during 40 ms. At t=260 ms the DG power is restored to 1 kW.

A. 100 Hz bus voltage controller

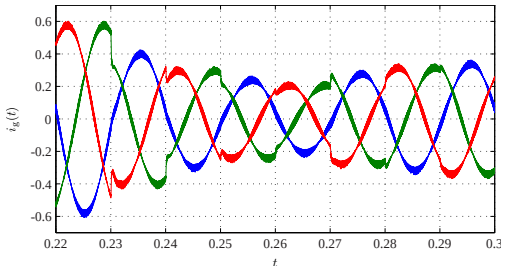
A first possibility for a bus voltage controller is the 100 Hz bus voltage controller. This bus voltage controller samples the bus voltage at a frequency of 100 Hz. The output of this controller is updated every 10 ms and is synchronized with the zero-crossings of the fundamental voltage of phase a. The current of phase a is changed at the zero-crossings in order to minimize the waveform distortion due to the updates of g_1 at the zero-crossings [15]. When the output of the bus voltage controller changes due to a transient in the power balance, there will be a step in the current of phase b and c which may result in oscillations. These oscillations can become significant if the grid has a low resistance.
Fig. 4 depicts the response of the bus voltage controller during the test. A step in the current in phase b and c can be seen. The oscillations caused by the step in the current result in a distorted current.
The low frequency of the voltage controller (100 Hz) results in a slow response and in high over- or undervoltages of the bus voltage in case of severe faults.

B. 100 Hz bus voltage controller with delayed updates at the zero-crossing of the grid voltage

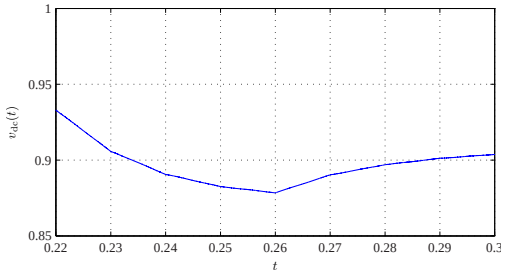
To improve the bus voltage controller of §A.. The reference value for the current in every phase is updated with the zero-crossings of the respective fundamental voltage. So when the input conductance changes, the reference values of the current in phase a, b and c will alternatively be updated. This has a beneficial effect on the current waveform. In contrast to the bus voltage controller of §A. there will be no distortion in the current.
Fig. 5 depicts the response of the bus voltage controller during the experimental test. It can be seen that there are



(a) The grid voltage



(b) The grid current



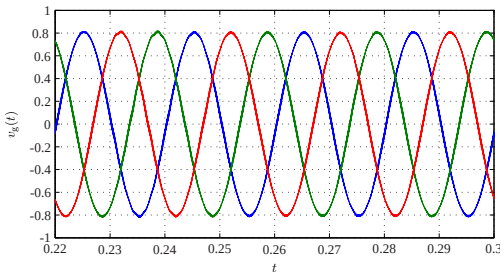
(c) The bus voltage

Figure 4: The grid voltage, grid current and bus voltage using the classical 100 Hz bus voltage controller. At t=220 ms the DG power is reduced from 2 kW to 660 W during 40 ms.

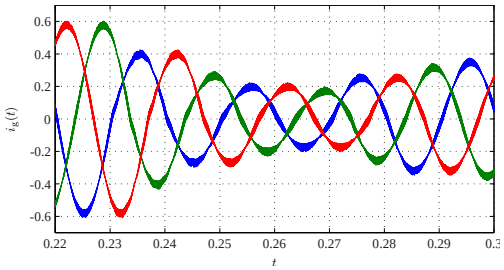
no steps in the reference currents in contrast to Fig. 4. The changes in amplitude at the zero-crossings can be noticed in Fig. 5(b).
The sample frequency of the bus voltage controller with delayed updates is the same as the sample frequency of the bus voltage controller of A., namely 100 Hz. The response of the present voltage controller will not be faster in case of severe faults.

C. 1 kHz bus voltage controller

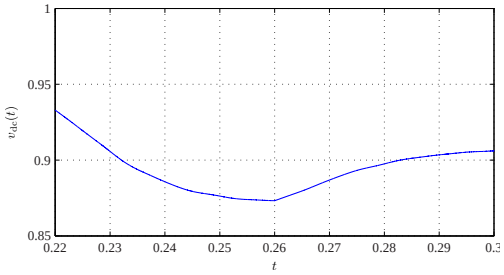
A third possiblity is the 1 kHz bus voltage controller. This controller takes samples of the bus voltage at a frequency of 1 kHz. The output of the voltage controller is also updated at 1 kHz.
Fig. 6 depicts the response of the bus voltage controller during the experimental test. In Fig. 6(b) it can be seen that there are oscillations in the current caused by a step in the reference current.
This bus voltage controller has a fast response but is sensitive to distortions in the bus voltage caused by harmonics or unbalance in the grid [10]. An oscillation in the bus voltage can result in the introduction of unwanted harmonics in the current.



(a) The grid voltage

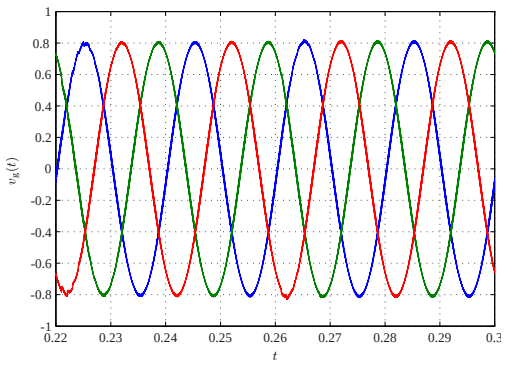


(b) The grid current

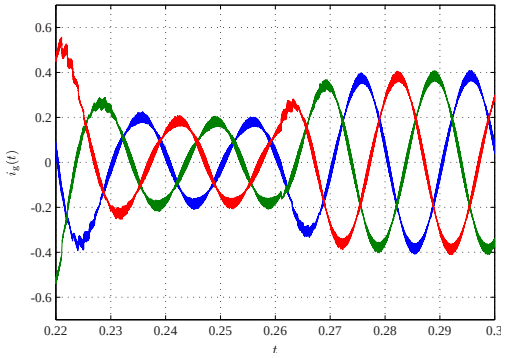


(c) The bus voltage

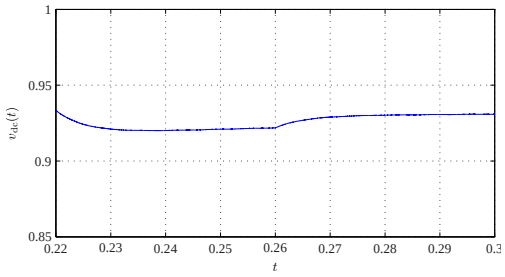
Figure 5: The grid voltage, grid current and bus voltage using the "100 Hz bus voltage controller with delayed updates at the zero-crossing of the grid voltage". At t=220 ms the DG power is reduced from 2 kW to 660 W during 40 ms.



(a) The grid voltage



(b) The grid current



(c) The bus voltage

Figure 6: The grid voltage, grid current and bus voltage using the "1 kHz bus voltage controller". At t=220 ms the DG power is reduced from 2 kW to 660 W during 40 ms.

6. Conclusion

An important function of the bus voltage controller of voltage-source inverters for distributed generation applications is to control the balance between the ac and the dc power. In three-phase systems a ripple can exist in the bus voltage due to unbalance or harmonics present in the grid voltage or current. This ripple can interact with the bus voltage controller which can have negative consequences for the injected current. In case of severe faults the bus voltage controller has to be able to react fast so high under- and overvoltages are avoided. The timing of updating the output of the bus voltage controller is also important because it can have consequences on the waveform distortion. In this paper the focus is on the timing of updating. A overview of three different bus voltage controller implementations is given and their response on a sudden transient is simulated.

The "100 Hz bus voltage controller" has a low bandwidth, such that the voltage controller does not respond to a double frequency ripple which can be present in the bus voltage. However this bus voltage controller has a slow response so severe faults can lead to high under- or overvoltages. During transients there will be a step in the current which may result in oscillations. These oscillations can become significant if the grid has a low resistance.

The second bus voltage controller is the "100 Hz bus voltage controller with delayed updates at the zero-crossing of the grid voltage" which also has a low bandwidth and a slow response in case of severe faults. The delayed updates at the zero-crossing of the grid voltage result in a distortion-free current so there will not be oscillations in the grid current.

The third and last bus voltage controller is the "1 kHz bus voltage controller" which has a high bandwidth. This results in a fast response in case of faults. An unbalance or harmonics in the grid voltage or current will result in harmonic components in the injected current because the bus voltage controller will react on the ripple in the bus voltage.

Each bus voltage controller has advantages and disadvantages and the optimal controller will differ depending on the application.

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