Digital bilinear feedback for low-power double-sampling sigma-delta modulators

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This document is an author's draft version submitted for publication to Electronics Letters.
The actual version was published as [1].

REFERENCES

[1] M. De Bock and P. Rombouts, "Digital bilinear feedback for low-power double-sampling sigma-delta modulators," *Electron. Lett.*, vol. 51, no. 1, pp. 27–U57, Jan. 8 2015.

Digital bilinear feedback for low-power double-sampling Sigma Delta modulators

M. De Bock and P. Rombouts

This paper presents a novel double-sampling technique for use in Sigma-Delta modulators. The proposed technique uses a digital bilinear filter in the feedback path of the modulator loop. The bilinear filter suppresses the quantisation noise folding that results from the double-sampling path mismatch. Unlike other solutions for the quantisation noise folding, the digital implementation of this filter allows to share the input sampling capacitor with the feedback sampling capacitor without any additional analog gain stages. This way, the power consumption in the input signal buffer can be greatly reduced, because it benefits from the nullator effect at the input of the Sigma-Delta loop and hence the current needed to drive the shared sampling capacitor is drastically reduced. Moreover, the proposed double-sampling technique is also suitable for a single-ended circuit implementation of double-sampling.

Introduction: Sigma-Delta modulators ($\Sigma\Delta$M) are widely used as low power high accuracy analog-to-digital converters (ADC). While recent research has focused more on modulators with a continuous time loop filter, switched-capacitor (SC) discrete time loop filters remain popular because they are less sensitive to parameter variations and clock jitter. In SC integrators, the double-sampling technique allows to double the sampling frequency of the circuits, without increasing the required opamp bandwidth. This way, the oversampling ratio (OSR) can be doubled which leads to an increased $\Sigma\Delta$M ADC resolution for the same power budget.

However, extending the simple (single sampling phase) SC-integrator to a double-sampling equivalent in a straight-forward manner limits the achievable resolution in a conventional $\Sigma\Delta$M because it gives rise to quantisation noise folding (QNF) [1]. Various approaches have been presented to counteract this QNF. The modified noise transfer function presented in [2] reduces the QNF but degrades the quantisation noise shaping and complicates the overall modulator design. In [3, 4] alternative differential SC integrator circuits that do not lead to QNF are presented, but the use of these circuits in a $\Sigma\Delta$M increases the load current for the input buffer extensively and cannot be used in a single-ended circuit implementation. In this letter, we will present a novel double-sampling scheme that counteracts the QNF without increasing the requirements on the input signal buffer.

Double-sampling and quantisation noise folding: Fig. 1(a) shows the simple SC integrator for use in the first stage of the $\Sigma\Delta$M loop filter. A single sampling capacitor C_A samples the input signal of the modulator (V_{in}) during the first clock phase (ϕ_1). During the next clock phase (ϕ_2), it samples the feedback signal of the modulator (V_{FB}) while at the same time the output voltage V_{out} is updated.

In this integrator circuit, both V_{in} and V_{FB} drive the same sampling capacitor. Since this sampling capacitor will be large due to thermal noise constraints, both V_{in} and V_{FB} will require additional buffering to drive this sampling capacitor. Designing the input buffer will be challenging as it needs to have a full swing low noise output with high signal integrity (THD<-100 dB) and fast slewing. However, in fig. 1(a) the voltage step that the input buffer needs to apply to the sampling capacitor is only the difference between V_{in} and V_{FB} of the previous time step. Due to the nullator effect of the $\Sigma\Delta$M-loop, this is approx. equal to the quantisation noise, which is very small in multi-bit ($\Sigma\Delta$M). This drastically reduces the voltage step and corresponding current that the input buffer needs to provide and will relax the design of the input buffer accordingly.

To make this circuit double-sampling, an additional sampling capacitor C_B is added with switches driven by dual clock phases as shown in fig. 1(b). However, in practice the sampling capacitors C_A and C_B are never completely matched. This results in an integrator gain mismatch between the two clock phases. We define the mismatch as $\delta = (C_A - C_B)/(C_A + C_B)$. In [1] it is shown that this integrator gain mismatch results in an additional error term e_{QNF} that is also integrated on C_{FB}:

$$e_{\text{QNF}}(z) = \delta \left(V_{\text{FB}}(-z) - z^{-1} V_{\text{in}}(-z) \right) \tag{1}$$

We see that the additional error term folds signals at $f_s/2$ ($z = -1$) back into the low pass signal band ($z = 1$). This is not a problem for the input signal, as we can assume that this signal will have a bandwidth that is smaller than $f_s/2$ due to the Nyquist sampling criterion. However, the feedback signal will contain a lot of (shaped) quantisation noise at $f_s/2$. Hence, the parasitic effect of the path mismatch is therefore often called quantisation noise folding (QNF), as it folds the shaped quantisation noise back into the signal band. The double-sampling integrator of fig. 1(b) also shares the input and feedback sampling operation on the same capacitors. Similar to the case for the simple integrator of fig. 1(a), the input buffer will have a drastically reduced load current if this integrator circuit is used as the first integrator stage of a double-sampling $\Sigma\Delta$M.

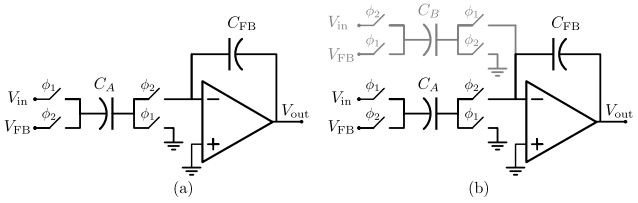

Fig. 1 *(a) A conventional simple SC-integrator (b) and the extension to double-sampling.*

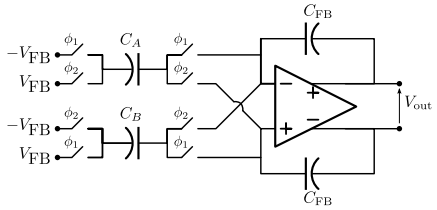

Fig. 2 *The fully-floating differential bilinear integrator presented by Senderowicz [3].*

Solutions to counteract quantisation noise folding: In [3], the fully-floating differential bilinear integrator shown in fig. 2 was introduced. For this integrator circuit it can be shown that even in the case of mismatch between C_A and C_B, the differential output signal V_{out} does not contain the error term of eq. (1). In a $\Sigma\Delta$M, this integrator circuit can then be used to sample the feedback signal V_{FB}. An additional conventional input sampling branch to sample V_{in} can then be added to this circuit as shown in [1] to make the first integrator stage in a $\Sigma\Delta$M.

However, the input and feedback signals are now sampled on different capacitors. This means that the circuit can't benefit from the nullator effect of the loop and the load current of the input buffer is now proportional to V_{in}. This leads to severe requirements on the input buffer design. Also, since the fully-floating bilinear integrator of fig. 2 is a differential implementation for which the single-ended circuit version is not feasible, this technique is not applicable in a single-ended circuit implementation of double-sampling. Variants such as the efficient floating double-sampling integrator presented in [4] have the same problem.

The modified noise transfer function presented in [2] does allow to share the sampling of the input and feedback signal on the same capacitor and it is also suitable for a single-ended circuit implementation of double-sampling. However, a major drawback of this approach is the complicated design of this modified noise transfer function which will always increase the residual quantisation noise in the signal pass band and as such will lead to an increase in power consumption for the same $\Sigma\Delta$M ADC resolution.

Proposed scheme: To counteract the QNF, we propose a new system level approach. Fig. 3 shows the new double-sampling scheme with digital bilinear feedback. Looking at eq. (1), we can reduce the QNF by making sure that $V_{\text{FB}}(-z) \approx 0$ over the signal band. Analysing the proposed scheme in fig. 3 in the $\mathcal{Z}$-domain, the feedback signal is

$$V_{\text{FB}} = H_{\text{FB}}(z) \left(STF(z) V_{\text{in}}(z) + NTF(z) Q(z) \right) \tag{2}$$

where we have introduced the signal transfer function (STF) from input V_{in} to the output D and the noise transfer function (NTF) from the quantisation noise Q to the output D as is common in $\Sigma\Delta$M analysis. Choosing $H_{\text{FB}} = (1 + z^{-1})$, the resulting QNF error term is now

$$e_{\text{QNF}}(z) \approx \delta (1 - z^{-1}) NTF(-z) Q(-z) \tag{3}$$

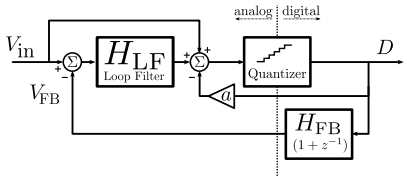

Fig. 3 *The proposed double-sampling ΣΔ-modulator architecture with a digital bilinear feedback filter to counteract the QNF.*

where we have again neglected the contribution of V_{in}. From this we see that the QNF error term is greatly reduced in the lowpass signal band due to the first order differentiation $(1-z^{-1})$. The additional feedback path (with parameter a) towards the quantizer input in fig. 3 is added to have complete control over the loop filter design [1].

Since the output D of the modulator loop is a digital signal, the feedback filter H_{FB} can be implemented in the digital domain. Implementing this bilinear factor in the digital domain allows us to use the double-sampling integrator of fig. 1(b). The only alteration is that the feedback DAC circuit now must be able to produce $2^{n_{bit}+1}$ different levels (for a $2^{n_{bit}}$-level quantizer). The feedback DAC complexity has increased by one bit, but this will have only a small effect on the power consumption in a SC ΣΔM as it will not increase the total load capacitance for the operational amplifier used in the integrator circuit.

However, since we will use the circuit of fig. 1(b), the input and feedback sampling operation is shared on the same capacitor. Since the feedback signal and input signal are approx. the same due to the nullator effect in a ΣΔM, the effective load seen by the buffer for the input signal is drastically reduced. This is even more so due to the bilinear factor which filters out even more quantisation noise in the feedback signal. Another advantage of the proposed double-sample scheme over the fully-floating bilinear integrator of fig. 2 is that it is also suitable for a single-ended implementation.

As in any multi-bit ΣΔM, the feedback DAC requires some kind of linearisation technique. The only alteration is that the complexity of the linearisation scheme will also be slightly increased as they will have to operate on an $2^{n_{bit}+1}$-level DAC. Standard linearisation schemes like data-weighted averaging (DWA) [5] can still be used.

Simulation Results: Fig. 4 compares the output power spectrum (PSD) of a system level simulation with a behavioural model in Matlab-Simulink for 2 different implementations of a double-sampling ΣΔ-modulator. The first (a) uses the proposed digital bilinear feedback scheme with the integrator circuit of fig. 1(b). The latter (b) uses the fully-floating bilinear integrator of fig. 2 [3]. Both modulators have the same feed-forward architecture with a third order loop filter and a 9-level quantizer, while the unit elements of the feedback DACs have normally distributed random mismatch errors with $\sigma = 1\%$ which are linearised with DWA. For the proposed digital bilinear feedback double-sampling scheme two DWA blocks operate interleaved. As can be seen in the output PSDs, for lower frequencies ($f < f_s/100$) the spectrum is dominated by the first-order shaped (-20dB/decade slope) mismatch errors of the DAC elements due to the DWA. For higher frequencies ($f_s/100 < f_s/10$) we find the expected -60dB/decade slope due to the third order loop filter. The spectra for both modulators are almost the same and this can also be seen from the output signal SNDR after decimation (OSR=32), which is 84.6 dB and 84.8 dB respectively. From this we conclude that both techniques give almost equal output resolution and the QNF is sufficiently suppressed by the first order noise shaping of eq. (3).

The main advantage of the proposed double-sampling scheme is that it reduces the load current of the input buffer that drives the sampling capacitors. This load current will always be proportional to the voltage step that the input buffer needs to apply to the sampling capacitor and the size of the sampling capacitor (which is the same for both implementations). Fig. 5 shows the normalised voltage step (relative to full scale) that the input buffer needs to drive every clock cycle for both double-sampling schemes. For the proposed digital bilinear feedback double-sampling technique (a), the normalised voltage step has a maximum of 0.29 and an rms value of 0.077. The maximum step is proportional to V_{LSB} and the rms value is below $V_{LSB}/2$. However, when the fully-floating bilinear integrator is used (b), the input buffer has to drive a voltage step that is proportional to V_{in} every clock cycle. We see that the proposed digital bilinear feedback scheme drastically reduces the maximum and rms voltage step and

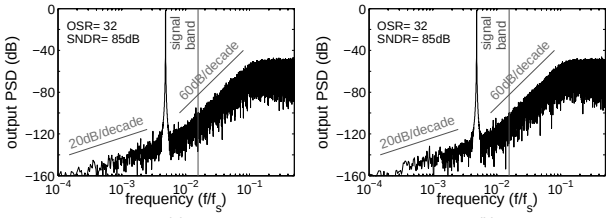

Fig. 4 *Comparison of the output power spectrum when DWA is used as DAC-linearisation scheme for (a) the proposed double-sampling ΣΔM using the integrator circuit of fig. 1 and (b) the double-sampling ΣΔM with the fully floating bilinear integrator of fig. 2 [3] (input tone is -1.5 dBFS at $f \approx f_s/200$).*

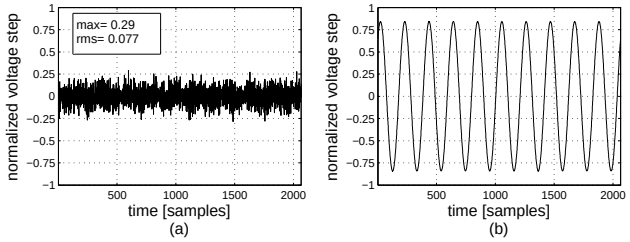

Fig. 5 *The normalised voltage step (relative to full scale) that the input buffer needs to drive into the sampling capacitor for (a) the proposed digital bilinear double-sampling scheme and (b) the fully-floating bilinear feedback ΣΔM over approx. 10 periods of the input signal (input tone is -1.5 dBFS at $f \approx f_s/200$).*

corresponding current that the input buffer needs to deliver and this effect will become even more significant as the number of bits in the quantizer and feedback DAC is further increased.

Conclusion: A new double-sampling technique for use in Sigma-Delta modulators is presented which uses a digital bilinear filter in the feedback path. While it is also suitable for a single-ended implementation of double-sampling, the biggest advantage of the proposed double-sampling scheme is that it allows sharing of the input and feedback sampling operation on the same capacitor without any additional analog circuits. This way it improves on prior techniques, as the input buffer will have to drive significantly less current and as a result can be designed with a lower power consumption. This makes this technique suitable for low power solutions in e.g. massive column parallel ADCs.

Acknowledgment: This work was supported by the Special Research Fund (BOF) of Ghent University

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