

Textronics – Definition, Development and Characterization
of Fibrous Organic Field Effect Transistors

Textronica – Definitie, ontwikkeling en karakterisering
van een vezelgebaseerde organische veldeffecttransistor

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the art of making impossible, possible

Introduction

Smart textiles and intelligent clothing or wearable technology are firmly established elements in today's textile world. Not only does the textile industry see opportunities in the development of this new product category, but also closely related industries have understood that smart textile products are important for their own future, namely chemistry and electronics.

Reasons for industries' interest are apparent. The basis of intelligent clothing will always be located in textiles. The chemical industry sees opportunities for instance in thin film technology that could be applied in light emitting diodes or transistors on textile substrates and the electronics industry does welcome the new textile substrate type. Each industry takes a different lead in integrating electronic functions into the textile and completes this process on differing levels.

This dissertation has three parts:

Part I sets the scene by giving an extensive overview on the current developments in the field of smart textiles with particular reference to two different aspects:

- i. research and development,
- ii. commercial availability.

The exploration of both aspects is instrumental in developing the definition of the concept of textronics.

Part II, tests the concept of textronics. The outcome of a range of technical experiments, which have been conducted on fibrous transistors, will be presented. The potential of application of organic electronics in smart textiles will be discussed here.

Part III, gives conclusions based on Part I and II, as well as suggests on how the research could be most effectively be continued.

Chapter 1 will introduce all aspects related to smart textiles from the world of chemical, electrical and textile engineering followed by a description of each discipline. The description will vary in depth and scope, focusing on the primary aim to ensure a shared knowledgebase of all readers. It is to be born in mind that this process does involve a degree of selectivity in terms of the scope of background knowledge of each discipline covered. It is envisaged closing the intra-disciplinary gaps by building a knowledge bridge between the various subject disciplines involved in industrial production of smart textiles. This study will contribute to the development of a truly inter-disciplinary approach.

Chapter 2 clarifies basic definitions of smart textiles and the essential components of smart textiles will be explained. In addition, a systematic approach to the classification of smart textiles has been constructed.

Chapter 3 follows up this systematic approach to classification. It is grounded in in-depth analysis of research, published patent applications and commercially available products. Furthermore, the challenges to be met when producing smart textiles are explored and the rational for investment into full integration of electronic function built into textiles is highlighted.

Chapter 4 completes Part I, containing the conclusions of the findings of chapter 3. In particular, results from the analysis of the smart textiles research and product landscape are followed up. Challenges detected on the technical level of textronics are identified. In addition, the current classification system of smart textiles at the European Patent Office (EPO) will be compared with the systematic approach suggested in this dissertation.

Chapter 5 sets the stage for the technical part of this dissertation. An introduction to the topic: transistors, is given and an approach on how the transistor is transferred onto the textile substrates is described. In addition, explanatory background knowledge will be reviewed. The transistor to be transferred onto a filament does comprise the deposition of four layers, namely gate, dielectric, semiconductor and source and drain electrodes.

For information regarding the technical details, chapter 6 describes all materials used in the experimental part as well as the techniques that were applied. Furthermore, the methods for characterization of morphological and electrical properties are disclosed.

In Chapter 7, a set of challenges in applying the gate layer are demonstrated.

Chapter 8, discusses the source and drain layer despite being application of the final layer in the transistor architecture. The reason is that the electrodes also serve in characterising the underlying layers and therefore, play a significant role. A variety of materials and deposition technologies have been assessed.

Chapter 9 contains the experimental results related to the application of the dielectric layer. Information about the layer's morphology and electrical properties has been collected and is discussed.

The work on the semi-conductive layer within the transistor architecture is presented in chapter 10. The challenges in detecting crystallinity in the layer as well as in characterising the layer electrically are established.

Chapter 11 contains the concluding remarks related to both parts of this dissertation. The challenges as discussed in the technical part of this dissertation are briefly recapitulated and as well as a range of options in terms of addressing these challenges are offered.

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List of abbreviations

Abbreviation

$(\text{C}_2\text{F}_4)_n$	poly(tetrafluoroethylene), fluorine
[bmim][Tf2N]	1-butyl-3-methylimidazolium bis(trifluoromethanesulfonate)
2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic Force Microscopy
a-IGZO	Amorphous indium-gallium-zinc-oxide
Al	Aluminium
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
Alq_3	Tris(8-hydroxyquinoline)aluminium
AS	Arsene
Au	Gold
B	Boron
BGBC TFT	Bottom-Gate-Bottom-Contact Thin Film Transistor
BGTC TFT	Bottom-Gate-Top-Contact Thin Film Transistor
$\text{C}_2\text{H}_6\text{O}$	Ethanol
ccc	Cathode current collector
CEN	European Committee for Standardization
Clevertex	Project acronym
CO_2	Carbondioxide
COLAE	Project acronym
CPU	Central processing unit
Cr	Cromium
CVD	Chemical vapour deposition
D	Drain
DMF	Dimethylformaldehyde
DOD	Drop-on-demand
ECT	Electrochemical transistor
EG	Ethylene glycol
E_g	Band gap
EL	Electroluminescent
ELIS	Electronics and Information Systems department
EPO	European Patent Office

Abbreviation	
ETFE	Ethylene tetrafluoroethylene
FET	Field Effect Transistor
FIB	Focused Ion Beam
FinFET	Fin (thin silicon) field effect transistor
G	Gate
Ge	Germanium
GPS	Global Positioning Systems
HCS	Hard-clad silica
HEMT	High-electron-mobility transistor
I.D.E.A.	Instruments of Dallas, Texas and Industrial Development Engineering Associates
IC	Integrated circuits
ICT	Information and Communications Technologies
I_{DS}	Current between drain and source electrode
IGFET	Insulated Gate Field Effect Transistor
IL	Ionic liquid (IL)
IPA	Isopropanol
IPR	Intellectual property rights
JFET	Junction Field Effect Transistor
k	Dielectric constant
LED	Light Emitting Diode
Lipon	Lithium phosphorus oxynitride
LTO	Low temperature oxide
MESFET	Metal-Semiconductor-Field-Effect-Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NaOH	Sodiumhydroxide
NMP	1-methyl-2-pyrrolidone
n-type	Negative charge conductor
OE-A	Organic Electronics Association
OFET	Organic Field Effect Transistor
P	Phosphorus
P_2O_5	Phosphorus pentoxide
P3HT	Poly(3-hexylthiophene-2,5-diyl)
Parylene C	Poly(chloro-p-xylene)
PCB	Printed circuits boards
PCT	Patent Cooperation Treaty

Abbreviation	
PECVD	Plasma Enhanced Chemical Vapour Deposition
PEDOT	Poly(3,4-ethylenedioxythiophene)
PEDOT:PSS	Poly(ethylene-dioxythiophene)/Polystyrene sulfonate
PEDT:tos	Tosylate-doped PEDOT
PEDT-S	Poly(4-(2,3-dihydrothieno[4-b]-[1,4]dioxin-1-yl-mthoxy)-1-butanefulfonic acid
PEN	Poly(ethylene naphthalate)
PES	Polyester
PHEMT	Pseudomorphic HEMPT
PI	polyimide
poly(ViEtIm)	Poly(1-vinyl-3-methylimidazolium bis(trifluoromethanesulfonimide)
ProeTEX	Project acronym
PSS	Poly(styrenesulfonate)
p-type	Positive charge conductor
PV	Photovoltaic
PVA	Polyvinylalcohol
PVD	Physical Vapour Deposition
PVP	Polyvinylpyrrolidone
PVP	Poly-4-vinylphenol
RFID	Radio frequency identification
RH	Relative humidity
RR P3HT	Regioregular poly(3-hexylthiophene)
R&D	Research and Development
S	Source
SFIT	Smart Fabrics and Interactive Textiles
Si	Silicon
SiC	Silicon carbide
SMARTpro	Project acronym
SMD	Surface Mount Display
SYSTEX	Project acronym
TE	Thermoelectric
TFT	Thin Film Transistor
TGBC TFT	Top-Gate-Bottom-Contact Thin Film Transistor
TGTC TFT	Top-Gate-Top-Contact Thin Film Transistor
TiO ₂	Tin dioxide
TIPS-pentacene	6,13-bis(Triisopropylsilylethynyl) pentacene

Abbreviation

TU DA	Technical University Darmstadt
UV/VIS	Ultraviolet-visible spectrophotometry
VDC	Venture Development Corporation
V_{DS}	Voltage between drain and source electrode
V_{GS}	Voltage between source and drain electrode
VMOS	V-groove shape metal oxide semiconductor transistor
VUB	Vrije Universiteit Brussel
WECT	Wire ECT
WTFT	Wire thin film transistor
XRD	X-Ray Diffraction
ZnO	Zinc-oxide
ZnO_2	Zinc Dioxide
α -6T	α -sexithiophene

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Summary

The field of smart textiles is a multidisciplinary one. Textile, chemistry, and electronic engineering are dominant, but increasingly material science and physics play an important part. With the involvement of such a range of scientific subjects, definitions are variable and at time confusing.

This dissertation refers to smart textile systems with an electronic function, so-called e-textiles. While the electronic function can be integrated at various levels into the textiles, the definition of concepts on a scientific technological basis is problematic. This study explores whether or not comparability of integration technologies is achievable. To this end, the technical level of the concepts for integration was assessed. The smart textiles landscape, including commercial products, patent applications and research in the field has been outlined and analysed. To allow the comparison of technologies, a set of five integration levels has been established. The levels relate to the integration of the electronic function starting at rigid electronics inserted by design, followed by rigid and flexible microelectronics attached to the textile substrate, and textronics permitting full integration. The latter achieves the highest level of integration from a textile engineering perspective and is referring to textronics.

Textronics are textile substrates onto or into which the electronic function is generated directly, added-on or built-in. This function can be generated on fabric (planar), on fibres or yarns (cylindrical) or material level hence, the electronic function and the textile substrate are inseparable. This is an important point when comparing textronics with rigid or flexible electronics which can be removed from the textile and still function independently. An example of textronics is an organic field effect transistor built on a polyester filament. Main manufacturing techniques to produce textronics are situated in thin film technologies.

The organic field effect transistor (OFET) is a three terminal electronic component, i.e. it comprises three electrodes. In the top-contact-bottom-gate (BGTC) transistor architecture, the gate layer is applied directly onto the substrate. A dielectric layer to electrically insulate the

gate from the rest of the structure is applied, after which the semi-conductor is deposited onto the dielectric layer. Compared to inorganic FETs, the semi-conductor layer within the OFET does not comprise inorganic material such as silicon, but is of organic nature.

Finally, the source and drain electrodes (top-contacts) are added onto the active material in a predefined distance from each other forming a channel. Depending on the material in the active layer, the transistor can make use of either p-type or n-type material. When voltage is applied to the gate, the electrical field causes the active material in the channel to change electrical properties. The conductivity of the semi-conductor in the channel is either increased (p-type) or decreased (n-type) representing an electrical switch enabling the flow of current between source and drain.

Experimentally, this fibrous transistor architecture is applied onto a polyester filament by using different thin-film process technologies. Firstly, the filament is coated with copper by electroless deposition to generate the gate layer. Subsequently, the dielectric layer is applied by dip-coating in polyimide, followed by the semi-conductor 6,13-bis(Triisopropylsilylethynyl) pentacene (TIPS-pentacene) layer equally put on by dip-coating. Finally, the top contacts, source and drain, are deposited by drop-casting or ink-jet printing. In this framework, the dielectric layer and the semi-conductive layer are the main focus of investigation. Since the top electrodes are a prerequisite for the final transistor function as well as for characterising the layers applied, they are also discussed in a separate chapter. The experimental challenge lies in applying materials from electronics onto a cylindrical substrate and in optimizing each layer by using manufacturing processes suitable to the textile industry.

In comparison to the gate layer which is conductive, the dielectric layer should electrically insulate the gate layer from the semi-conductive layer. At the same time it should be as thin as possible since its thickness influences the voltage to be applied to the gate. The gate voltage (V_{GS}) which serves to switch the transistor on or off, like for other microelectronic devices, should be kept low. In addition,

the dielectric layer should be as smooth as possible to reduce leak current and therefore a potential decrease in performance of the transistor. Furthermore, the roughness of the dielectric layer influences the growth of the semi-conductor which is subsequently applied. The dielectric layer was solution processed from polyimide resin and an aromatic solvent. The solution concentrations as well as two different solvents, namely 1-methyl-2-pyrrolidone (NMP) and dimethylformaldehyde (DMF), have been tested for their influence on the morphology of the dielectric layer. Furthermore, the influence of dip-coating speed and environmental humidity was investigated. Results show that highest insulating properties at minimum layer thickness could be achieved by dip-coating at a speed of 50 mm/min, and a solution of polyimide and NMP at a concentration of 15w%. The roughness was reduced to 0.375 nm which is a comparable value in common microelectronic application.

The active, semi-conductive layer was made from TIPS-pentacene solved in toluene. Also here the morphology of the layer was investigated, whereas the crystallisation of the material was the focus of this part of the research project. To find the right characterization technique obstacles were dealt with in detecting the crystals on the substrate but also in the practical conduction of electrical characterization. The solution concentration and the solvent was held constant in this part of the research project determined by the availability of the material. However, the influence of the dip-coating speed on the layer morphology was investigated. The semi-conducting material crystallized in defined arrangements when dip-coated at low speeds (5 mm/min). Large crystals were envisaged to reduce the amount of grain boundaries. Furthermore, the drying process of the layer has been assessed, because of the sensitivity of TIPS-pentacene to light and humidity, a better morphology was generated when the layer formation took place in dry conditions.

The electrical characterization of the layers required the application of top-contacts. Different process techniques have been tested for applicability of the source and drain electrodes on the semi-conductor. The semi-conductor is very sensitive, therefore non-contact process techniques were preferred. Drop-casting of silver

conductive screen printing ink and nano-silver ink-jet printing ink, evaporation of silver and aluminium, sputtering of gold as well as ink-jet printing of nano silver conductive ink were evaluated. Best results in matters of accuracy and positioning of the electrodes have been achieved with ink-jet printing. Accuracy and positioning are imperative because the active channel is defined by the location of the electrodes. They should be located in a distance of maximum 100 μm , with a clearly defined outline of the electrode in the channel region. Even though ink-jet printing showed a superior results, drop-casting was the final method of choice for practical reasons.

In conclusion, a dielectric layer with good insulating properties, being as thin as possible and sufficiently smooth has been generated. In addition, the application of TIPS-pentacene has been assessed and a crystalline layer has been deposited. Various process techniques for depositing the top-contacts have been defined and investigated. Although, the transistor function as a switch has not yet been achieved as yet. Choice of materials and process techniques might need further thought and changes will have to be made accordingly. The obstacles to successfully establishing the transistor function related to each layer are discussed in this dissertation.

Samenvatting

Het domein van intelligent textiel is multidisciplinair in al zijn facetten. Textiel, chemie en elektronica hebben een evenredig aandeel maar materiaalkunde en fysica winnen eveneens aan belang. Door de betrokkenheid van uiteenlopende wetenschappelijke domeinen heerst er grote verwarring in de definities. Dit doctoraat bespreekt intelligente textielsystemen, d.w.z. met een elektronische functie. Deze elektronische functies kunnen op verschillende niveaus geïntegreerd zijn in het textiel. Om de obstakels op een wetenschappelijk-technologische basis te omschrijven, moeten de integratietechnologieën vergeleken kunnen worden. Bijgevolg werd het technische niveau van de integratieconcepten beoordeeld. Het intelligent textiel landschap, omvattende commerciële producten, patenten en onderzoek, werden daarom beschreven en geanalyseerd. Om technologieën te kunnen vergelijken werd een set van vijf integratieniveaus ontwikkeld. De niveaus houden verband met de integratie van een elektronische functie gaande van rigide elektronica die via het ontwerp kan geïntegreerd worden, gevolgd door rigide en flexibele micro-elektronica aangebracht op/in het textielsubstraat; tot “textronica” die volledige integratie toelaat. Vanuit textielloogpunt vormt textronica het hoogste integratieniveau. Het betreft textielsubstraten waarop of waarin de elektronische functie rechtstreeks wordt gegenereerd. Dit kan gebeuren op het niveau van het weefsel (vlak), de vezels of garens (cilindrisch) of op het niveau van het materiaal waaruit het textiel gemaakt is. In dit laatste geval zijn de elektronische functie en het textielsubstraat onafscheidelijk. Dit is een belangrijk punt wanneer men textronica vergelijkt met rigide of flexibele elektronica die verwijderd kan worden van het textiel en individueel kan functioneren.

Een voorbeeld van textronica is een OFET (*Organic Field Effect Transistor* of organische veldeffecttransistor) aangebracht op een polyesterfilament. De belangrijkste productietechnieken voor textronica zijn dunne-film technologieën.

Een OFET is een elektronische component met drie terminals, d.w.z. hij omvat drie elektroden. In de BGTC (*Bottom-Gate-Top-Contact*) transistor architectuur is de *gate* rechtstreeks aangebracht op het

substraat. Om deze *gate* elektrisch te isoleren van de rest van de structuur wordt een diëlektrische laag gebruikt. Vervolgens wordt de halfgeleidende laag aangebracht op de diëlektrische laag. In tegenstelling tot anorganische veldeffecttransistoren bevat de halfgeleiderlaag van een OFET geen anorganisch materiaal zoals silicium, maar is het van organische aard. Tot slot worden de *source* en *drain* elektroden (topelektroden) aangebracht op de actieve halfgeleidende laag op een welbepaalde afstand van elkaar, hierbij een “kanaal” vormend. Afhankelijk van het materiaal van de actieve laag, kan de transistor hetzij p-type of n-type zijn. Wanneer een elektrische spanning aangebracht wordt op de *gate*, zorgt het elektrische veld ervoor dat het actieve materiaal in het kanaal de elektrische eigenschappen wijzigt. De geleidbaarheid van de halfgeleider in het kanaal wordt hetzij verhoogd (p-type) of verminderd (n-type) en vormt aldus een elektrische schakelaar.

In dit werk wordt de transistorarchitectuur aangebracht op een polyesterfilament door middel van verschillende dunne film-procestechnologieën. In eerste instantie wordt het filament gecoat met koper via een chemisch depositieproces om zo de *gate* te verkrijgen. Vervolgens wordt de diëlektrische laag aangebracht door middel van dipcoating in polyimide, gevolgd door de halfgeleidende 6,13-bis(triisopropylsilylethynyl) pentaceen (TIPS-pentaceen) laag eveneens via dipcoating. Tot slot worden de topelektroden (“*source*” en “*drain*”) afgezet met behulp van *drop-casting* of inktjet printen. De diëlektrische laag en de halfgeleidende laag vormen de kern van het onderzoek in dit werk. Vermits de topelektroden een voorwaarde zijn voor de uiteindelijke transistorfunctie en voor het karakteriseren van de aangebrachte lagen, worden ze in een apart hoofdstuk besproken. De experimentele uitdaging ligt in het toepassen van materialen uit de elektronica op een cilindrisch substraat en in het optimaliseren van elke laag door gebruik te maken van procedés die geschikt zijn voor de textielindustrie.

In vergelijking met de *gate* die geleidend is, moet de diëlektrische laag de *gate* elektrisch isoleren van de halfgeleidende laag. Terzelfdertijd moet deze laag zo dun mogelijk zijn vermits de dikte ervan de elektrische spanning beïnvloedt die op de *gate* aangebracht

moet worden. Deze *gate* spanning om de transistor aan en uit te schakelen moet laag gehouden worden, zoals ook het geval is voor andere micro-elektronische apparaten. Daarnaast moet de diëlektrische laag zo glad mogelijk zijn om lekken en aldus vermindering van de transistorperformantie te vermijden. Verder beïnvloedt de ruwheid van de diëlektrische laag de vorming van de vervolgens aangebrachte halfgeleidende laag. De diëlektrische laag werd vervaardigd uit een oplossing van polyimidehars en een aromatisch solvent. De concentratie van de oplossing evenals twee verschillende solventen, met name 1-methyl-2-pyrrolidone (NMP) and dimethylformaldehyde (DMF), werden getest op hun invloed op de morfologie van de diëlektrische laag. Ook werd de invloed van de dip-coating snelheid en omgevingsvochtigheid onderzocht. Resultaten tonen aan dat de hoogste isolatie-eigenschappen bij minimale dikte van de laag bereikt worden met dip-coating aan 50 mm/min uit een oplossing van polyimide en NMP bij een concentratie van 15w%. De ruwheid werd gereduceerd tot 0,375 nm wat een vergelijkbare waarde is in gebruikelijke micro-elektronische toepassingen.

De actieve, halfgeleidende laag werd gevormd uit TIPS-pentaceen en haar morfologie werd bestudeerd. De kristallisatie van het materiaal vormde een belangrijk aspect in het onderzoek. Hiervoor moesten obstakels overwonnen worden door het vinden van de juiste karakteriseringstechnieken, het detecteren van kristallen op het substraat maar eveneens door het uitvoeren van elektrische karakterisering. De invloed van de dip-coatingsnelheid op de morfologie van de laag werd onderzocht. Het halfgeleidend materiaal kristalliseerde bij lage dip-coating snelheden (5 mm/min). Grote kristallen werden beoogd om de hoeveelheid korrelgrenzen te verminderen. Verder werd het droogproces van de laag beoordeeld terwijl omwille van de licht- en vochtgevoeligheid van TIPS-pentaceen een betere morfologie gegenereerd werd wanneer de vorming van de laag gebeurde in droge omstandigheden.

Elektrische karakterisering van de lagen vereiste het aanbrengen van een *source* en *drain* elektrode. Verschillende productietechnieken werden getest met het oog op de geschiktheid van de elektroden. De halfgeleidende laag is zoals reeds vermeld, zeer gevoelig en

bijgevolg werd de voorkeur gegeven aan contactloze technieken. *Drop-casting* van geleidende inkt voor zeefdrukken en nano-zilver inkjet inkt, verdamping van zilver en aluminium, sputteren van goud evenals inkt-jet printing van nano-zilver geleidende inkt werden beoordeeld. De beste resultaten voor wat betreft nauwkeurigheid en positionering van de elektroden werden bereikt met inkt-jet printing. Nauwkeurigheid en positionering zijn zeer belangrijk in dit verband omdat het actieve kanaal gedefinieerd wordt door de locatie van de elektroden die zich op een afstand van maximum 100 μm moeten bevinden met een welbepaalde aanduiding van de elektrode in het “kanaalgebied”.

Kortom, in dit werk werd een diëlektrische laag gegenereerd met goede isolerende eigenschappen, die zo dun mogelijk en voldoende glad is. Daarnaast werd de aanwending van TIPS-pentaceen beoordeeld en een kristallijne halfgeleidende laag werd afgezet. Verschillende procestechnieken voor het aanbrengen van de topelektroden werden gedefinieerd en onderzocht. Echter, de transistorfunctie als schakelaar werd nog niet gerealiseerd. De keuze van materialen en procestechnieken zal eventueel herbekeken moeten worden. De obstakels voor het tot stand brengen van de verschillende lagen van de vezelvormige OFET werden in dit doctoraatsonderzoek behandeld.



Part I Textronics

Chapter 1 introduces smart textiles, which leads up to a suggestion for the development of a classification system for e-textiles and the active electronic components identified in chapter 2 and 3, thereby delineating the field of textronics. The scientific challenges in the classes relevant to the experimental work in Part II of this dissertation are given in chapter 4.

1

Setting the Scene

The idea of integrating electronic functions into textiles has been present in product development and design for decades. In 1932, the concept of electrically heated clothing for police officers was introduced [9]. In 1966, the designer Diana Dew integrated light into fashion items [10, 11]. At the time, when the first smart textile system products were developed, the concept of smart textiles did not exist as yet. Over the time, besides smart textiles many other applications all pointing in the same direction were invented. The uncoordinated nature of these inventions lead to a bewildering use of terminology, which tended to obscure and confuse researchers. This chapter reviews terminology and identifies the need for developing a classification scheme for comparing technical concepts.

The concept of smart textiles is an established buzz word in research and development. It is said, that smart textiles will both contribute to the quality of people's life's and at the same time strengthen the competitiveness of the industry in Europe and worldwide [12]. Not only in textile related fields, but also in electronics and in material science, smart textiles are unavoidably linked to huge expectations in view of market opportunities. Since smart textiles carry this incredible potential, it is essential that all those involved with different scientific backgrounds understand the multidisciplinary field so that definitions are clear and a common terminology can be used. The following paragraphs engage in describing the characteristics of smart textiles, discussing which technologies and functions are related to this emerging technology, before moving on to the experimental part of the dissertation.

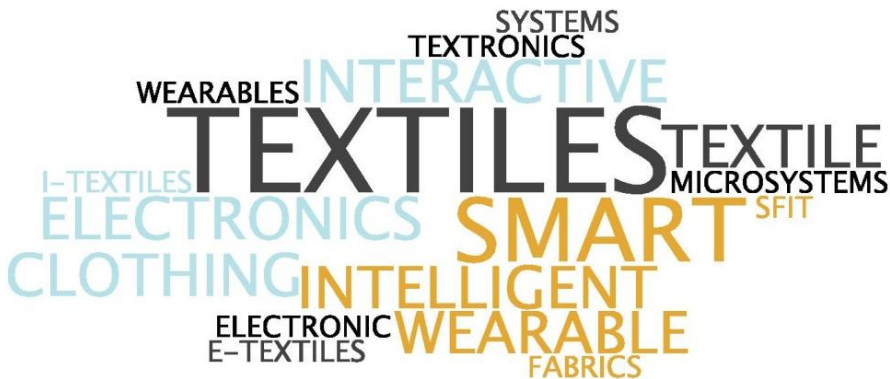


Figure 1 Commonly used terminology in the field of smart textiles

Smart textiles, intelligent fabrics, e-textiles, intelligent clothing, smart fabrics, wearable electronics, interactive textiles, wearable microsystems, i-textiles, textile electronics, electronic textiles, textronics, SFIT, interactive textiles, smart textile systems, wearables, are common terms used in the world of smart textiles (Figure 1). Since smart textiles' existence, various players in research [2] but also in industry [13] and even official organizations [1, 14, 15] are attempting to further summarize or define the field by fitting smart textiles into various schemes. A systematic definition of concepts has not been achieved as yet and distinguishing between a range of definitions remains problematic. Other organizations, which might not

be as involved in technically aspects, do not necessary understand the specific meaning of the terminology, but might have to use the wording in an applied context [16]. Consequently, confusion is inevitable.

The way terminology is used is derived from the personal perspective. Here, one aspect is the influence of commercial interest. The wording smart textiles or its equivalent is used depending on the industrial context. Smart textiles belong to a new product range and therefore, each industry tries to make smart textiles a part of their own product portfolio. Samsung and Peratech, for example, are companies in the electronics industry, which have become involved in the textile business [17, 18].

Especially within the European textile industry, high tech products like smart textiles might be a the last ditch attempts to compete, before production is moved to countries which offer lower production costs [10]. Hence, the textile itself has a higher or lower degree of importance in the smart textile structure in comparison with electronics, for instance. Here, the textile itself is sometimes downgraded, even to the extent that it is only seen as a “dumb” substrate type [13] whereas, in the textile industry it is the most important component. It is noted that this practise is not only found in industry, but also in research. Textile research entities, concentrate on the full integration of electronic functions into the textile and in electronics the general approach is to embed electronics either on a micro scale or by attaching flexible substrates onto the textile. This will become clearer in chapter 3 (see p. 75 of this dissertation).

For quite some time, smart textiles cannot be ignored in research as being only important on the conceptual level. Where precisely smart textiles should pigeonholed in is still up for debate. The CEN (European Committee for Standardization) working group on smart textiles uses the term smart textiles as an equivalent to intelligent textiles [1]. Organizations like the Organic Electronics Association (OE-A) have listed smart textiles in the roadmap for application areas of organic electronics as part of integrated smart systems (2013) [19] and also in the Canadian technology roadmap for its textile industry (2008) [20] intelligent textiles are listed as one of the future trends. A

market size of US\$ 250 million in 2004 and US\$ 640 million in 2008 has been mentioned at the time of reporting. In this particular roadmap even a new textile category like those are used at the international trade fair TechTextil was invented and named smarttech. This seems to point to market studies covering different segments of smart textiles.

The smart textiles field and its market potential is huge. Based on a report from Venture Development Corporation (VDC) in 2007, Textiles Intelligence Limited (2008) published the following market data [21, 22] (Figure 2).

Table 1: Smart fabrics and interactive textiles (SFITs): sales by manufacturing segment, 2006-10
(US\$ mn)

	2006	2007 ^a	2008 ^a	2009 ^a	2010 ^a	Annual average % change 2006-10 ^a
SFIT input components ^b	121.7	137.9	157.7	182.1	213.8	15.1
Intermediate SFIT components ^c	221.5	258.3	318.4	431.7	678.1	32.3
Finished SFIT-based textiles	26.0	44.6	77.4	133.5	237.5	73.8
Total	369.2	440.9	553.4	747.3	1,129.5	32.3

NB: numbers may not sum precisely due to rounding; percentage changes are based on rounded data.
^a Forecast. ^b Described by VDC Research as enabling components. ^c Described by VDC Research as SFIT-based modules.
 Source: *Smart Fabrics, Interactive Textiles and Related Enabling Technologies*, Third Edition, by Venture Development Corporation, November 2007.

Figure 2 Smart fabrics and interactive textiles (SFIT) sale by manufacturing segment, 2006-2010 [in million US\$]

In January 2014, Grand View Research estimated the overall size of the global smart textile market as US\$ 289,5 million in 2012 with strong expected increases until 2020 to US\$ 1,500 million [23]. Besides the trend for increasing market size, all those market reports have one aspect in common: they are not completely clear which exact product range is considered in their analysis. This makes it difficult to understand and compare market data. In spite of this, a general conclusion can be made. Even if the data above is not comparable, smart textiles are a rising star at the horizon.

Today, smart textiles easily become linked to other hypes, in particular the hype of wearable technology. According to Jupiner Research, the market of wearable business is expected to reach the US\$ 1,5 billion mark in 2014 [24]. The well-known conference series Smart Fabrics picked up on the trend of wearable technologies and renamed their popular conference Smart Fabrics to Smart Fabrics and Wearable Technology [25]. As stated in a report from the

company Ohmatex (2014) [13], wearable technology can be any electronic device which is small enough to be worn on the body. Due to the overwhelming hype of wearable technology, smart textiles are increasingly perceived as a subcategory of wearable technology. This is shown, for instance in the ABI Research report on Global Wearable Computing Devices [13]. In this report, the essential property of smart textile products, being the inseparable link between textiles and electronic functions, is ignored. In some reports on wearable technology, like a paper by Armstrong-Smith (2014) [26] textiles are not even mentioned as an option for integration. A distinction between wearable technology and smart textiles can easily be made. This will be demonstrated in the following paragraphs. Also it will be shown that e-textiles are a part of smart textiles. Textronics as a subclass of e-textiles will be investigated in detail.

Referring to the report from Ohmatex again, some more definitions are given, e.g. Interactive Textiles being wearable technology that is integrated into a garment or controlled by an integrated panel or button. This definition is rather limiting since an interactive textile does not need to be wearable but also could be a curtain or a carpet. Furthermore, in the market report titled E-textiles: Electronic Textiles from IDTechEx Ltd (2014), so-called e-textiles are depicted as part of wearable electronics and smart textiles but also being a part of soft circuits (Figure 3) [27].

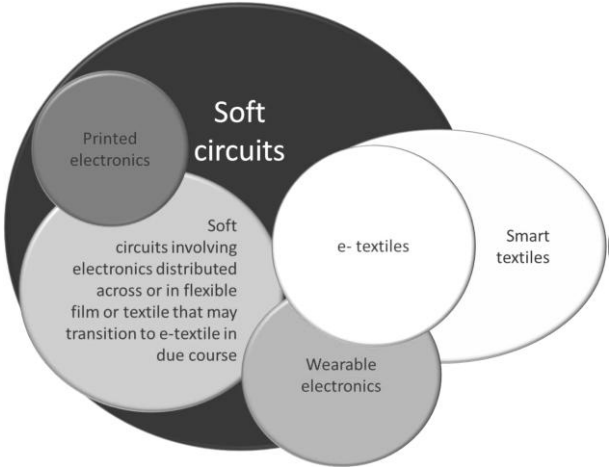


Figure 3 Schematic classification of e-textiles in market report from IDTechEx (E-Textiles: Electronic Textiles, 2014) [27]

When revising the scheme in Figure 2, e-textiles are shown as part of soft circuits and smart textiles. Printed electronics can be a part of soft circuits and e-textiles. Wearable electronics also can be a part of printed electronics and soft circuits. Electronics are therefore a major part of e-textiles which is further analysed in this study. Figure 4 does show a variation of Figure 3.

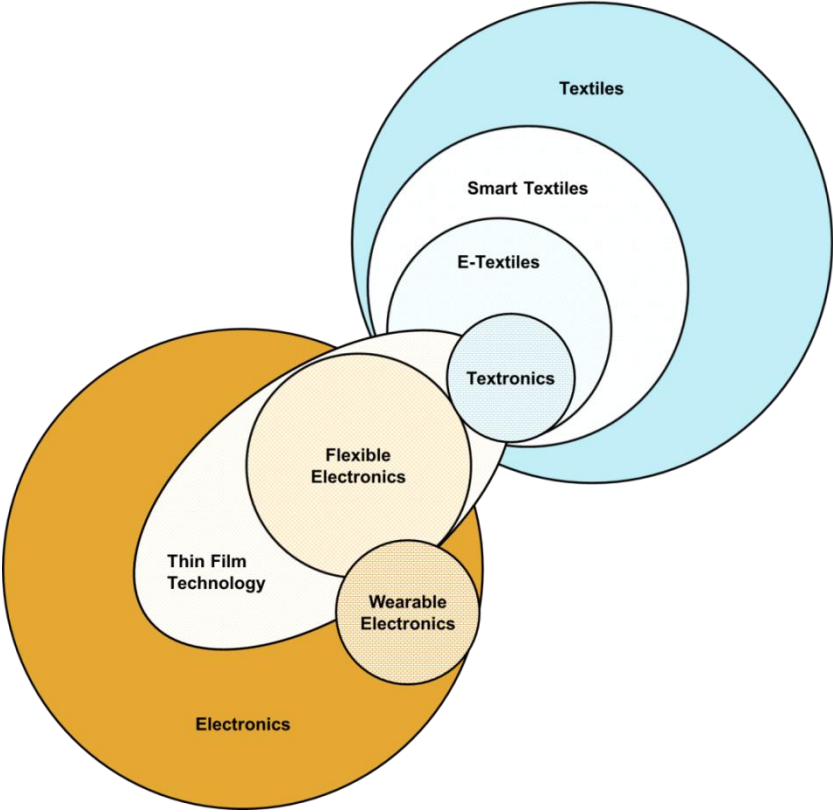


Figure 4 Revised schematic classification of e-textiles based on market report from IDTechEx (E-Textiles: Electronic Textiles, 2014) [26]

One reason, why smart textiles are being placed the same category as wearable technology might be the inherent conceptual difficulty that textile substrates pose regarding the integration of electronics (Definition 1).

Definition 1: Electronics

The field of electronics includes electrical circuits and interconnection technologies. Electrical circuits comprise active electrical components such as transistors, diodes and integrated circuits, whereas interconnections are of the passive kind. Generally, electronic devices involve circuitry consisting mainly of active semiconductor devices in combination with passive elements [6].

For industry, producing wearable devices with functions that could be linked to smart textiles e.g. sensors, seems to be the most accessible market. With easy access, consideration of costs and time to develop and commercially introduce products with an integrated electronic function, come into play. The more research is required, the costlier this process becomes for industry, constituting a major drawback. Incremental product development, e.g. for making an existing device wearable, does not compare to the associated costs of bringing new products to the market. The latter is related to disruptive product development, which in this context indicated a need for fundamental extensive research, specifically targeting textile integration.

During the course of the following sections, this will also become clearer, in particular comparing research in terms of integrating or attaching electronic functions. A sub-group of smart textiles, so-called e-textiles, are textiles with an electronic function. In the following chapters, only this sub-category of smart textiles is further investigated. The electronic function (Definition 2) is the main property of e-textiles.

Definition 2: Electronic Function

An electronic function is generated by an electronic component, for instance wires conduct current, batteries supply electrical energy, switches allow current to flow, resistors restrict the flow of current, transistors amplify current, capacitors store electric charge, Light Emitting Diodes (LED) transfer electricity into light. Electronic components can be part of an electronic circuit [4, 7].

Figure 5, shows examples of common electronic components



Figure 5 Examples of common electronic components: wires, batteries, resistors, transistors, capacitors, LED (from left to right) [28]

The component can either be active or passive depending on the materials used in its construction (Definition 3).

Definition 3: Active and Passive Electronic Components

An electronic component is either active or passive. Active components are based on a source of energy, they most often need electricity to function e.g. transistors and diodes. Passive components do not actively use electricity to function, they rely on the voltage applied to the circuit e.g. wires or antennas [5].

The electronic function might also be the reason why e-textiles and smart textiles in general often are connected to Information and Communications Technologies (ICT). It shall be noticed that research funding schemes focusing on smart textiles and e-textiles are non-existent and are often covered by ICT and material related funding

schemes or schemes with certain objectives for instance with applications for ageing population.

In the European project SYSTEX (as described in the Annex A.2.), smart textile research projects were analysed according to the process technologies applied for generating the smart textile function. Within SYSTEX, this classification was developed for roughly clustering the various existing research projects.

In the present context, this list of process technologies does not serve in bringing more structure into the field i.e. making the different concepts comparable. The list is too extensive to draw conclusions. It rather reflects the complexity of the field and the difficulties in finding definitions. In

Table 1, an excerpt of this list as revised within the project SMARTpro is given. A description of the project can be found in the Annex A.4. of this document.

Table 1 Process technologies used in smart textiles

Process Technologies	
atomic layer deposition	felting - non-woven
braiding	knitting
chemical vapour deposition (CVD)	laminating
coating - dip	plasma - corona
coating - spin	plasma - other
cutting - blade	printing - 3D
cutting - hydro	printing - digital
cutting - laser	printing - inkjet
cutting - ultrasonic	printing - roll-to-roll
electro-spinning	printing - screen
electrostatic charging	soldering
embedding/encapsulation	sol-gel
embroidery	spinning - rotor
engraving	weaving
evaporation	welding
extrusion - melt	other

As for the collection and classification of products in the framework of the project SMARTpro other priorities for classification have been chosen. These include:

- Application areas e.g. medical, sports, or protective
- Complexity level, e.g. system, component, or material
- Item maturity e.g. product, prototype, research, or material

Also these additional properties in classifying were not designed for making technological concepts comparable but only added to the detail of product information collected.

Obviously, in research the need for more structure in the increasing field of smart textiles has been recognized and an effort in classifying research projects and products has been made.

The European Patent Office (EPO), does evaluate patent applications based on their technological content. To ensure that intellectual property can be granted this assessment also includes comparing new technologies to existing ones. Therefore, over the years an international patent classification system was developed. This classification is continuously adapted to the needs i.e. in case new technology got invented and does not fit into the existing scheme, new classes or subclasses are added. It requires hardly any imagination to see that the number of classifications is vast to date and it is difficult to achieve an overview. In addition, patent assessment and classification is strongly related to the patent examiner and his or her experience in interpretation of the system. Hence, a full systematic approach is not established and relevant classes have to be screened in their description for a potential fit of the patent. Thorough analysis will lead to classification in very specific subclasses, less detailed analysis to classification in the main classes. In both attempts, it is evident that locating a patent for comparison involves more effort than it would, if it were classified in a more structured way. It shall be noted that patents can be filed on a national, European (EP) and international level. In relation to this dissertation, nationally filed patents (FR, DE, US, UK, JP, KR) as well as European and internationally filed patents have been analysed. International filed patents are indicated as PCT patents (Patent

Cooperation Treaty) and filed at the World Intellectual Property Organization.

Currently, at the European patent office, patent applications believed to be related to smart textiles are classified in the existing scheme. Based on their analysis in this dissertation, the reality shows that the set of categories used at EPO to classify potential smart textile patents does not entirely cover patents in the field of smart textiles. The collection of patents was classified by the EPO in 85 different categories, showing huge variations. Only 16 categories were used more than two times in classifying the patents. Of those 16 classes, only 6 were listed as categories in which smart textiles are generally classified. Based on this information it can be indicated that fitting the new inventions into the existing scheme is not satisfactory. As shown above, because there are no dedicated categories for smart textiles, the patents have to be classified either in a very broad or very narrow sense. There has been discussion on how to handle patents related to smart textiles in the future in view of the existing scheme and development of a more comprehensive means of evaluation [15].

A common system of classification and for comparison of smart textile technologies would unify the fields of research and consequently, ease and speed up transfer of knowledge between the industrial players, leading to faster commercialization of products. Many attempts have been made to unravel the smart textile entanglement, still a common basis for technical communication was not found. In chapter 1, a range of these attempts for classifying smart textiles were shown. None of the above mentioned schemes is perceived as suitable for making technologies comparable. Logically, if technologies cannot be compared, technological challenges reappearing in different conceptualisations are less easy to detect. It therefore seems, that even after decades of the existence of smart textiles, there is still a need for further definition.

To establish this common ground, it should be recalled how smart textiles are defined today. A breakdown of the smart textiles system to the specific component will enable developing a systematic approach to classification of e-textiles as part of smart textiles. This

will enhance general understanding in the field and clarify which technological approaches are followed in producing smart textiles as well as indicate challenges to be met when integrating the electronic function into the textile.

2

Smart Textiles

Chapters 2 and 3 develop a classification system according to integration levels based on a set of five questions. In addition, chapter 2 reviews a range of definitions and background information in order to understand the field of smart textiles and, in particular e-textiles, and their variations in integration levels.

To develop the analysis of the field of smart textiles further, it is useful to look at their application. This leads to the most visible level: existing smart textile products. Before doing so, one needs to decide which items can actually be considered as smart textiles or e-textiles and which should be excluded from the analysis. This is achieved by asking a set of 5 questions as described during the course of this and the succeeding chapter. Initial point of the analysis is imagining a device, product or item, to be investigated. Referring to the list of terms used for smart textiles, the first of five questions can be asked to determine if the item or product is relevant in the field of smart textiles.

Q1: Is the item covered by one of the terms used for smart textiles (see Figure 1)?

If the answer to the question is **negative**, i.e. there is no evidence of terminology used for smart textiles which might be related to the item, the item will be excluded from further analysis. Examples of those items to be excluded are telephones, all sorts of white goods or cars (Figure 6).



Figure 6 Examples of items not related to smart textiles

If the answer is **positive**, i.e. the item is covered by one or more terms, it merits further analysis. A second question is designed to gain further information:

Q2: Is the electronic function of the item related to a textile substrate?

A textile substrate could be everything from the material to spin the fibre, the fibre or filament, the textile structure, being for instance

knitted, non-woven or woven to the final textile product, e.g. carpets, curtains or clothes. Textiles can be found in many applications and some are not perceived by the end-user as textiles. This includes composites, membranes and filters but also materials used in building and construction, like thermally insulating glass fibre material [29]. These items therefore are considered and question 2 can be answered **positively**.

Surprisingly already at this point, a distinction between smart textiles and wearable technology can be made. Here, we exclude all the rigid items from watches, belts and jewellery to Global Positioning Systems (GPS) and calorimeters.

Definition 4: Wearable Technology

Wearable Technology is technology that is incorporated into things worn on a day-to-day basis. This can be everything from smart watches, augmented reality glasses or health monitoring bracelets [4]. The concept of wearable technology is derived from the concept of wearable computing. A computer worn on the body collecting and processing data [8].

If the item belongs to the field of wearable electronics, question 2 should be answered **negatively** and therefore the item would be excluded from further analysis. Some examples of wearable technology (Definition 4) products are shown in Figure 7.



Figure 7 Examples of Wearable Technology Polar belt (left), Google glasses (middle), Nike fuelband (right)

In general, all rigid accessories worn on the body could be wearable technology, and perceived as rigid ware when compared to smart textiles or e-textiles being the flexible or drapable ware. As stated in

chapter 1, the link or relation to the textile substrate or element within the system is of crucial importance to define the product as belonging to the category of e-textiles. After narrowing down those items relevant to the smart textile field, the definition of smart textiles and e-textiles which are also used for Smart Fabrics and Interactive Textiles (SFIT) can be used for further analysing the device or item in question [13] (see Definition 5).

Definition 5: Smart Textiles

Smart textiles are textiles with the ability to react to different physical stimuli; mechanical, electrical, thermal and chemical etc. [1].

Initially, electronics were integrated into textile structures on a low-tech level by simply attaching rigid microelectronic devices [30]. After some time and many unsuccessful (or even failed) products [30], it became clear that customers are not satisfied with unreliable gadget-like items. They demand more advanced solutions, i.e. electronic devices which are invisibly integrated into their surroundings [31]. Today, research and industry strive for truly integrated electronic functions. Therefore, research is trying to find ways to construct electronic devices directly onto (added-on) or into (built-in) the textile substrate like fibres or filaments. Integrating electronic functions on the textile level leads to a new category of smart textiles (**Error! eference source not found.**) as part of e-textile: textronics.

As previously outlined (see chapter 1, p. 43), the CEN standardization working group of smart textiles is one of the entities working on a more structured approach for defining smart textiles. Based on the work completed in the European FP7 project Clevertex, the CEN working group established a scheme for defining external stimuli and their response in smart textile systems. It should be noted that the table concerns materials used within the smart textile system, so-called smart textile materials (Definition 6).

Definition 6: Smart Textile Materials

Smart textile materials are part of functional textile materials. These materials do interact actively with their environment, i.e. respond or adapt to the stimuli received from the surrounding [1].

A smart textile material is always functional, whereas a functional textile material is not always smart. For instance, the anti-microbial finishing on textiles leads to a functional textile, but is not smart since it does not interact with the environment. In comparison, phase change material integrated in textiles does react to external stimuli like temperature and therefore belong to the field of smart textile materials. Smart materials can be used in components of a smart textile system.

During this study, it showed that the active electronic components (Definition 3) were not completely covered by the table the CEN working group established. For example, the electronic function of a capacitor or a transistor is generated by combining different materials which in themselves are functional but not necessarily smart. This combination leads to a stimulus-response function. Both components can be perceived as responding to an electrical stimulus by for example storing the electrical stimulus or by amplifying it. Consequently, this effect is similar to the controlled release effect and was as such added to the table at the intersection of electrical stimulus and electrical response (see Table 2). It is debatable whether more effects have to be added when thinking of other smart textile system components. The supplemented collection of stimuli response effects is shown in Table 2.

Table 2 Overview of stimuli response effects [1]

STIMULUS						
RESPONSE	magnetic	thermal	electrical	chemical	mechanical	optical
optical		thermochromism thermo-opacity	electrochromism electroluminescence electro-opacity	chemiluminescence solvatochromism halochromism	piezochromism	photochromism
mechanical	shape- memory magnetostriktion		inverse piezoelectricity electrostriction electro-osmosis shape-Memory	shape-memory sup-absorbing sol/hydrogel	dilatant thixotropic auxetic	
chemical			controlled release	controlled release		
electrical		seebeck effect pyroelectric	"controlled release"		piezoelectricity	photovoltaic photoelectric effect
thermal			joule coulombic heating peltier effect	exo/endothrm reactions	friction	

This dissertation, when referring to smart textile systems, a system is meant that is composed from a number of components (see Figure 8). These components are connected and are functioning in relation to each other. For example a sensor senses an increase in temperature; this information is transferred to the data processing unit which communicates via an antenna to a remote station. There a decision is taken how to respond to the increase in temperature. This decision is communicated and an actuating unit, for example a cooling unit, is activated. All this is powered by a battery within the system.

Definition 7: Smart or Intelligent Textile Systems

Smart or intelligent textile systems are responsive and/or adaptive and/or interactive textile system

An intelligent or e-textile system consists of two main elements, actuator-sensor combinations and a data processing unit. Furthermore, they can be classified based on their ability to communicate with the surrounding (external) and/or if they need a power supplying unit e.g. a battery [1, 2].

A smart textile system (Definition 7) reacts to stimuli from the environment but includes more than one component functioning as one system. As mentioned above (p. 43), the CEN working group on standardization for smart textiles (TC248 W435) does also differentiate between smart textile systems with/without energy and/or a communication component. This study solely refers to electronic functions being integrated into the textile, or better still, components with electronic function within the smart textile system. Consequently, electricity is an important part of the smart textile or e-textiles system. In this dissertation it is immaterial how the energy is supplied e.g. using a magnetic coil, a photovoltaic cell or battery.

Returning to analysing the item which passed the first two questions of the assessment for smart textiles, there are other options for further investigation of the item's first nature. It has been mentioned that smart textiles have electronic functions, therefore it is crucial to

detect first which electronic component merits further analysis. It is a precondition to assess each single component in order to understand the nature of the smart textile system entirely and to assess its technological level further.

A smart textile system can comprise five main components, being sensors, actuators, communication devices, data processing units, or energy components. Often the interconnections, connecting the various components are listed as part of the smart textile system, too (Figure 8).

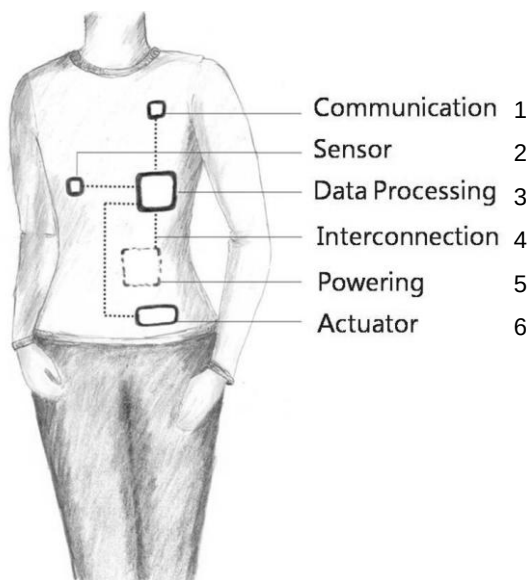


Figure 8 Smart Textile System Components: sensors (1), actuators (2), data processing unit (3), interconnections (4), communication devices (5), and energy components (6) [32]

Only e-textile systems and in particular the active components carrying an electronic function within the system are considered, however smart textile materials are excluded from this particular study. Therefore, although interconnections are an important part of the system itself, they are not considered since they do only have a passive function. A passive function is for instance being electrically conductive (Definition 8) or in case of optical fibres being optically

conductive, e.g. for transferring signals. Interconnections are passive in nature and therefore do not actively respond to external stimuli.

Definition 8: Electrical Conductive Textiles

Electrical conductive textiles have one main property: being conductive. This property can be used to conduct electricity or shield from electromagnetic field. Electrical conductivity can also be used for heating and supplying antistatic properties [3].

This leads us to question 3 in the systematic approach.

Q3: Which smart textile component generates the function?

If question 3 was answered **negatively (i.e. none)**, the previously given answers have to be revised. It might be that the item does not belong to the field of smart textile systems if a previous question was not answered affirmative. On the one hand, this is a kind of control question, to double-check the current status of evaluation, on the other, this question leads to a clear decision which component within the smart textile system should be included for further analysis.

If the electronic function is generated by one of the five smart textile system components the question was answered **positively**. It is useful to examine the variety of components within the system in greater depth. To recapitulate, a smart textile system is composed out of 5 main components (see Figure 9), namely sensors, actuators, communication devices, data processing unit, and energy components. Interconnections play a passive role within the system [32].

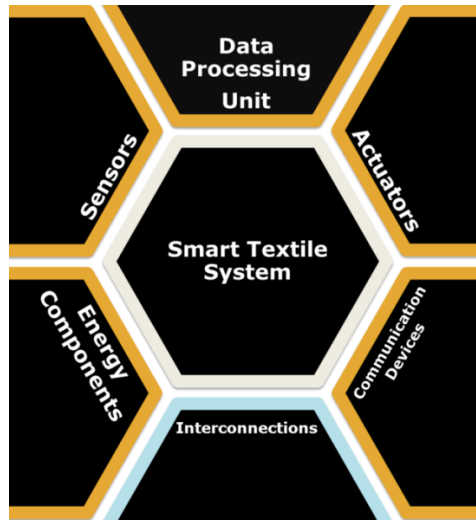


Figure 9 5 + 1 Components within the Smart textile system

During this study, it became evident that the scheme needed to be updated by including the connector as an additional part within the smart textile system. It has been acknowledged that the link between the interconnection and the component itself is difficult to achieve. Connectors are linking the component and the interconnection, and therefore, are located where components and interconnections meet. The scheme shown in Figure 10 visualizes the concept of the connector.

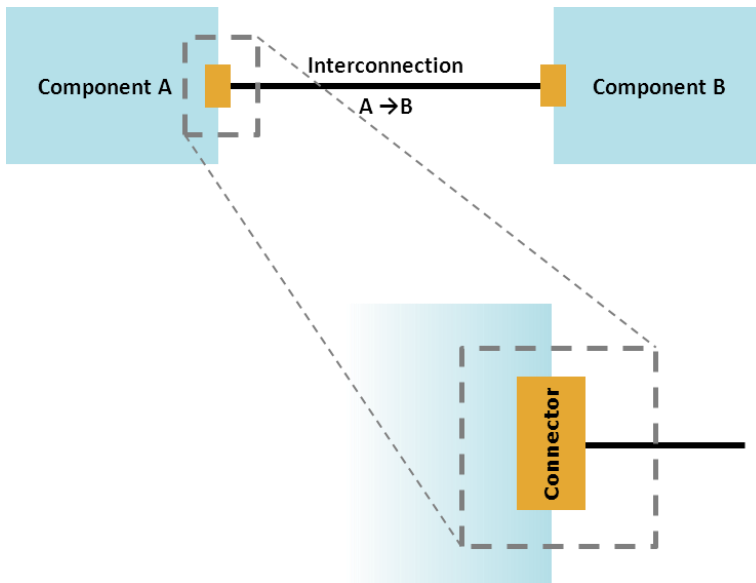


Figure 10 Connector linking component and interconnections

Currently, a wide variety of joining techniques are applied for connecting the various components and interconnections. Soldering, using glue or pressure button are some of those. This added material does not only influence the handle of the textiles to a great extent, but also the quality and reliability of the joint itself. Research as well as industry are attempting to find more effective ways of connecting the different parts within the smart textile system [13]. Examples for textile connectors are shown in Figure 11 and Figure 12.



Figure 11 Washable textile connector OHMATEX [33]

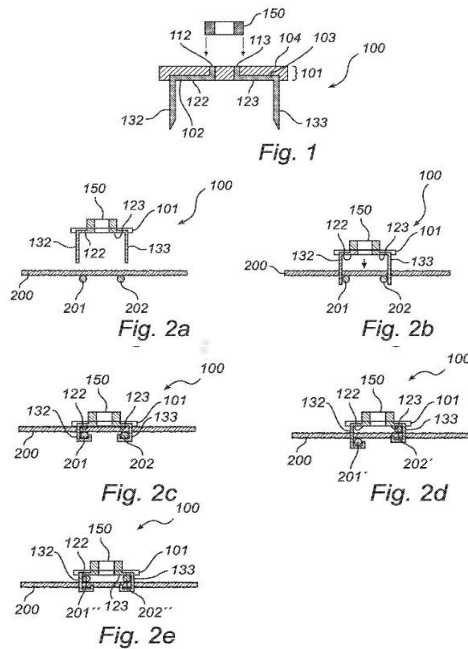


Figure 12 Submount for electronic components (WO2008007237), technical drawings [33]

Figure 13, shows the updated scheme of 5 + 2 smart textile system components, indicating related types of components. As for the sensors, the first order categories are shown, the actuator categories describing the type of response are listed as well. The energy component does refer to both energy storage, and energy harvesting. Some technologies for interconnecting the components are listed, in addition, to the options for connectors. The data or central processing unit (CPU) is a more complex endeavour. The CPU includes a combination of passive and active devices arranged in a logical circuit. To our knowledge, apart from conceptual studies, there are no applied attempts of full textile integration of the data processing unit. This component might more appropriately addressed by the electronics industry in terms of a less advanced level of integration Components related to communication do include all kinds of antennas; some are listed in Figure 13.

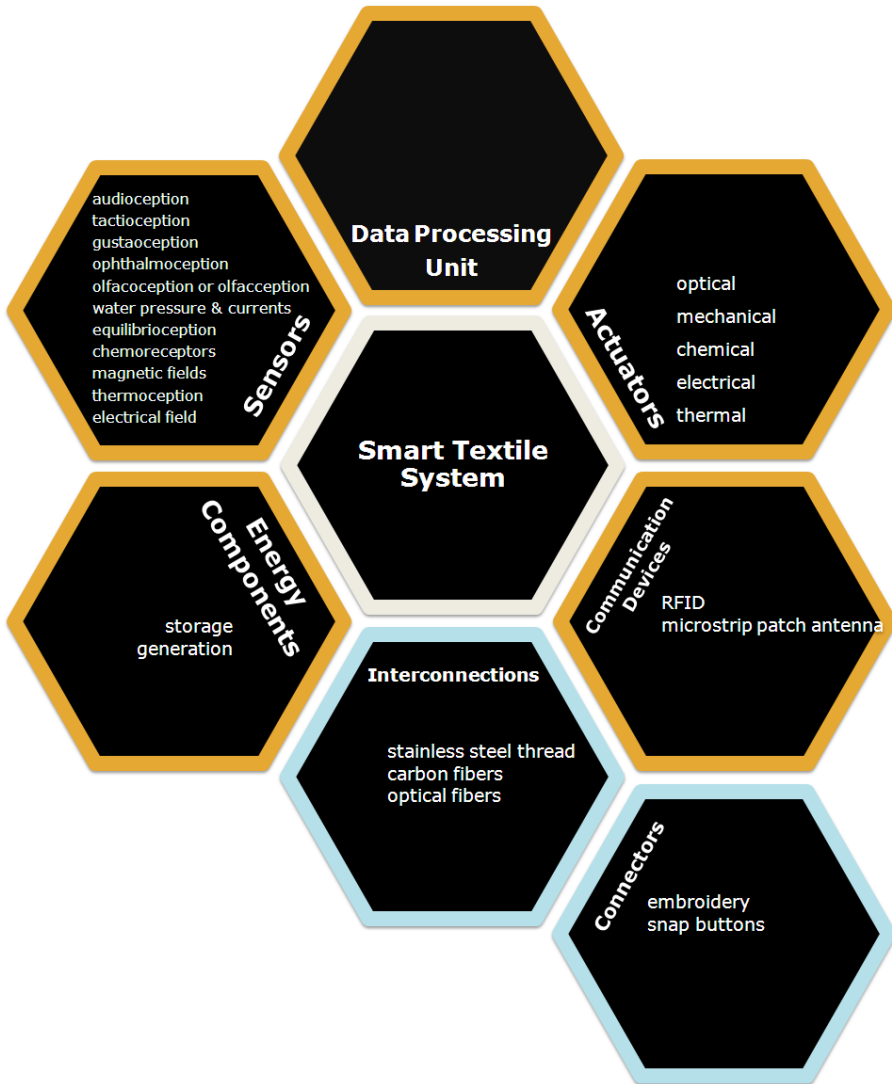


Figure 13 Updated 5 + 2 smart textile system components

As shown in chapter 1 above, in the course of the European funded FP7 project SYSTEX, a classification system for publicly funded projects in smart textiles was established. This system was taken a step further during the course of the IWT-VIS funded project SMARTpro (IWT-120779 – project number. 201-1577; “Slim Textiel en draagbare intelligentie: Van intelligente prototypes naar industriële en bruikbare producten). Short project descriptions of SMARTpro and SYSTEX can be found in the Annex A.2. and A.4. Within SMARTpro,

the classification was used for collecting information about smart textile products and further narrowed down and combined with the table for stimuli and response [1]. As mentioned in an earlier section (p. 43) of this dissertation, the outcome was a more elaborate scheme as shown in Table 2.

Smart textile system components can be classified according to their function within the system itself. Based on this study, two of those components, namely sensors and actuators received subcategories due to the extensive character of the category. In detail, sensors were classified according to the commonly known senses in humans. Hence, besides the basic five senses which are sight, hearing, taste, smell and touch, a number of senses like temperature, balance, and chemoreceptors (e.g. CO₂ content in blood), kinesthetic sense, and sense for pain were added. The latter two were not considered any further as these senses are solely relevant in relation to animate objects and therefore do not play a role regarding electronic components. Instead, three other categories of sensors were added which also exist in the animal world, the senses for electric or magnetic fields and the sense to detect water pressure and currents. The outcome was a list of sensors in exactly 11 categories. This new information was combined with existing one. Table 3 lists all 11 sensor categories.

Table 3 Classes of sensors and examples in application

sensors	SIGHT (ophthalmoception)
	light, imaging, photon
	proximity, presence
	navigation/location
	HEARING (audioception)
	acoustic, sound, vibration
	TASTE (gustaoception)
	chemicals
	SMELL (olfacoception/olfacception)
	gases
	TOUCH (tactioception)
	pressure/strain
	moisture, humidity
	Temperature (thermoception)
	temperature (thermal change, heat), heatflux
	BALANCE (equilibrioception)
	acceleration, position, angle, displacement, speed
	CHEMO (chemoreceptors)
	ionizing, radiation, subatomic particles
	ELECTRIC (electrical field)
	electric current, electric potential,
	MAGNETIC (magnetic fields)
	magnetic, radio
	PRESSURE/FLOW (water pressure and currents)
	flow, fluid velocity
	Other

Also the list of actuators has been revised and adapted to a new scheme based on the table for stimuli and response shown earlier. Five main classes have been identified comprising 28 sub-categories of first order and 10 sub-categories of second order. The extensive list of actuators is shown in Table 4.

Table 4 Classes and subclasses of actuators

actuators	optical	
		colour changing
		solvatochromism
		halochromism
		electro-opacity
		photochromism
		piezochromism
		electrochromism
		thermochromism
		thermo-opacity
		light emission
		electroluminescence
		chemiluminescence
	mechanical	
		dilatant
		thixotropic
		auxetic
		shape-memory effect
		super-absorbing
		sol/hydrogel
		inverse piezoelectricity
		electrostriction
		electro-osmosis
		shape-memory
		magnetostriction
		sound (vibration)
	chemical	
		controlled release
		electrolysis
	electrical	
		photovoltaic\photoelectric effect
		piezoelectricity
		seebeck effect
		pyroelectric
		“controlled release” (transistor, memory, battery, capacitor)
	thermal	
		friction
		exo/endotherm reactions
		joule
		coulombic
		heating
		peltier effect
		phase change
	other	

The other three smart textile system components have already been mentioned earlier and will not be further explained here.

Based on question 3, it has been determined which smart textile system electronic component needs further analysis, the following question will lead to identifying the perspective which determines which component merits further investigation.

Q4: On or in which substrate is the component's smart textile electronic function generated? (Textiles or Electronics)

Today many commercial attempts in producing smart textiles originate from the micro-electronics industry. Here, electronic components in rigid or flexible form are attached-on or built-in the textile substrate. This means, the function actually is generated by the electronic component which then can be combined with the textile. If this is the case, the smart textile function or electronic function is generated by the electronics, not by the textile. Consequently, if the important relation to the textile (Q2) is missing, the item would fall into the category of wearable electronics, since also here the actual function is separable from the textile substrate.

In reverse, if the function is generated by the textile itself, it means that the function is not generated if the textile is absent. Hence, the textile and the function are inseparable. In the scientific review paper of Carpi and De Rossi (2005) [34], the author confirms the importance of the degree of device integration. In this study, a clear distinction has not been made but more a subjective evaluation of the degree of device integration has been chosen to determine level of advancement.

Therefore in order to clarify the difference between the integration levels, the wording for adding a function to the textile substrate should be revised (Definition 9).

Definition 9 Incorporating, Embedding, Integrating

Incorporating is the action of uniting (one thing) with something else already in existence, for example attaching electronics onto textiles. Integration levels 1 to 3 (added-on) are related to incorporation.

Embedding is becoming an integral part of a surrounding whole, for example weaving an electronic tape into the textile structure. Integration Levels 3 (built-in) to 5 refer to the action of embedding [2].

Integrating is the action of bringing all parts together to unify them into a whole. The combination of the electronic function with the textile in generally, is called integration.

Based on this dissertation's research for adding the electronic function into the textile, five integration levels can be defined (Figure 14). The levels do also include those techniques not directly related to integration but also to embedding and incorporation. Starting at the lowest level of integration these are:

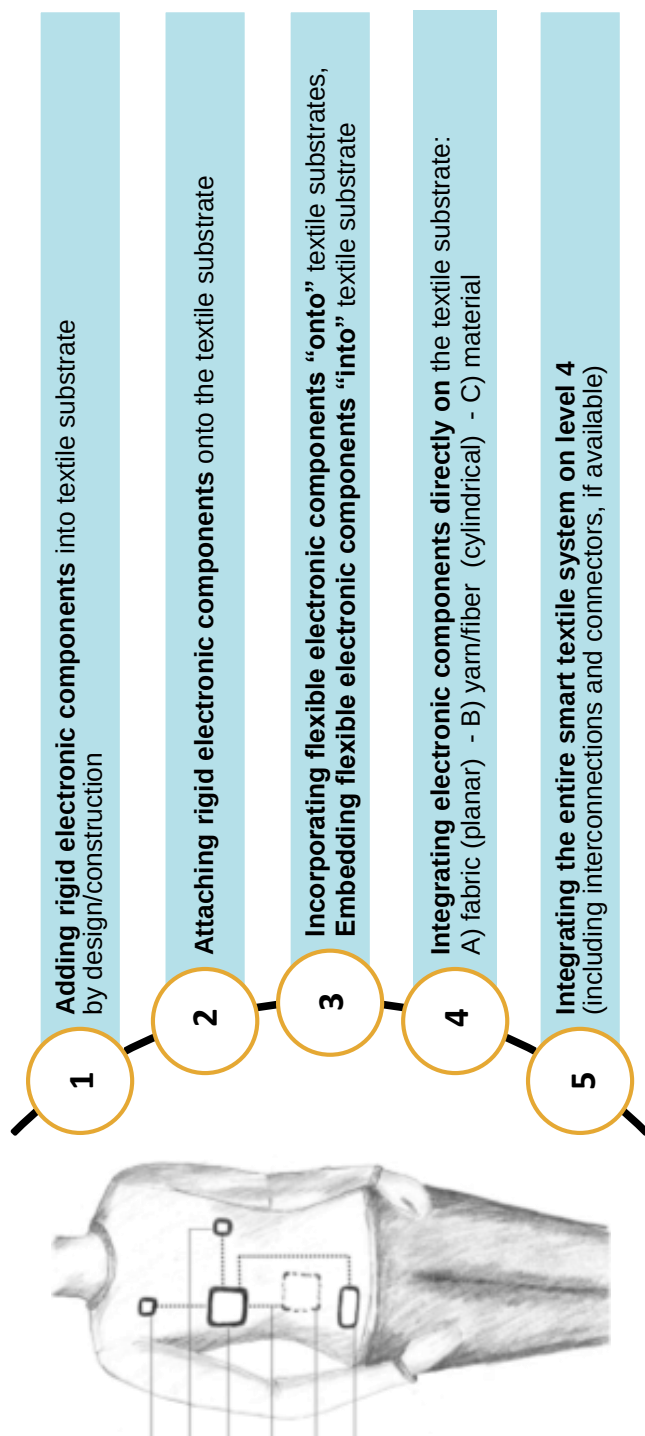


Figure 14

Smart textile system component integration levels

As one can imagine, the latter is the most sophisticated level of integration and challenging research for invisibly merging the two fields: textiles and electronics into textronics. The final product truly integrates textiles and electronics, making separation impossible. Consequently, if answering to question four with “electronics”, integration levels 1-3 have to be taken into consideration, in terms of further analysing the component. If the textile is the base for integration, level 4 is of concern. Level 5 can be reached in both ways, in textiles this would be full integration of the entire system into textile substrates, in electronics, something like electronic skin could be an option [35]. Up to date, systems on integration level 5 are none existent for both substrate types. To visualize integration level 5 and with reference to Tanaka (2003), at this point of integration, the electronic function should be integrated so that the electronic device (smart textile) can be handled “like a handkerchief” [36].

It is worth noting, that smart textile products are systems. There is a good chance that the single e-textile components of the system are integrated on different levels. The highest level of integration, level 5 relates clearly to the entire smart textile system and not to the single e-textile component. Therefore, it is evident that integration level 5 only can be reached if all components do fulfil these preconditions. For the single component the highest integration level that can be reached is level 3 or alternatively level 4 (textronics).

To visualize integration levels 1-4 and distinguish between them, examples from the commercial side shall be given in the following chapter. Also, the various concepts in research and related patents for integration levels 1-4 will be addressed in the following chapter

3

Screening the landscape of smart textiles

This chapter reviews applied research in the field of textile electronics. For each integration level, a review of the literature was undertaken to select examples per products in the field of textile (micro) electronics, intellectual property (patent applications) and up-to-date research. It was not always possible to identify appropriate examples since current state-of-the-art products, patents and research do focus on different levels of textile integration. The examples should make the conceptual distinction between the various textile integration levels explicit. The concepts were chosen for their capacity to illustrate the specific type of integration level; additional examples will be shown in the Annex B.1. of this dissertation. Technical challenges per integration level, based on the listed concepts, are identified and summarized in chapter 4.

3.1. Integration level 1

The first products were commercialized at current integration level 1 more than a decade ago. With progress made in research and development, over time, lower integration levels have become obsolete, once suitable technologies for integration for large scale or mass production have been developed, industry will lose no time to adopt these processes. To recapitulate, integration level 1 means the electronic function is integrated by adding the actual electronic device to the construction of the textile e.g. into the pockets of a garment (see Figure 15).

Examples of products at integration level 1



Figure 15 Levi's ICD+, cooperation between Levi's and Philips with Fibretronic soft controls (2000) (left) [37] and Scottevest jacket with attachable solar panel (2006) (right) [38]



Figure 16 KOYONO BlackCoat Jackets line with washable textile keypad from Eleksen (2006) [39]

Figure 15 and Figure 16 show how the integration of the electronic function is made by adding rigid electronic devices to the textile or garment. This integration is completed on basis of the design and pattern construction. The devices have to be removed from the garment before washing or maintenance. They are rigid and easy to identify, both visually and by touch. Current research is no longer prioritising in this type of integration. This type of integration level was very popular in the early stage of smart textiles (Definition 10). These days, complying with increasing customer demand and improved process technologies, products are situated in a higher integration level (see, paragraphs 3.2 and 3.3 below).

Definition 10: Integration Level 1

Integration level 1 shows rigid electronics being visibly added into the textile product on basis of design or pattern construction. The devices generating the electronic function are not washable, and are easy to recognize within the textile product.

3.2. Integration level 2

Integration level 2 shows similar rigidity of integrated electronic devices, although here the form factor plays a different role. At this integration level the devices attached to the textile surface are less bulky than in integration level 1. Especially planar electronics are attached to the textile structure. Often parts of the electronic devices need to be removed before washing. Some of the inventions are washable but still rigid and visually easy to identify. Examples are shown in Figure 17 to Figure 19.

Examples of products at integration level 2



Figure 17 NYX clothing, range of customized jackets with built-in flexible display screens that connect to a Palm OS PDA or smart phone (2006) [40]



Figure 18 T-Qualizer - Raver Equalizer Shirt (since 2006) (left) [34] and Digital Clock T-Shirt (2006) (right) [41]



Figure 19 Zegna Freeway Jacket' with iPod and Bluetooth controls or Solar panels in the collar (2009) [35]

Based on the above the following definition can be confirmed in Definition 11.

Definition 11: Integration Level 2

Integration level 2 shows rigid electronics being visibly integrated in textile products which are washable to a limited extent and still possess a high degree of recognizable integrated electronic function. Simple attachment technologies are applied. Integration level 2 relates to integration which is recognisable to touch, but flexible and washable to certain extend.

3.3. Integration level 3

Integration level 3 displays greater complexity with regard to currently available options for the development of solutions. Two main options were pursued: the integration of electronics added-on or built-in the textiles substrate.

Integration is achieved by attaching the electronic device using the medium of glue or pressure buttons etc. or by embedding it into the textile substrate, e.g. by weaving electronic devices manufactured on plastic tapes into the fabric. At integration level 3, the device itself is a stand-alone-component, which in order to function does not necessarily need to be connected with the textile structure (excluding the aspect of being interconnected, see Definition 12).

Definition 12: Integration Level 3

Integration level 3 describes integration in two manners. Either the electronic function is added-on or built-in. This means that either an electronic component is attached to the textile substrate or the electronic component is a crucial part of the textile substrate. Integration level 3 relates to an integration which is still recognisable to touch but flexible and washable. Integration level 3 relates to an integration which is still recognisable to touch, flexible and washable.

To date, some commercial products are available which utilise level 3 integration techniques. On-going research is vigorously pursuing the

improvement of available techniques. Examples for integration concepts in products at integration level 3 (added-on) are shown in Figure 20 to Figure 22.

Examples integration level 3 (added-on)

Examples of integration concepts in products at integration level 3 (added-on)

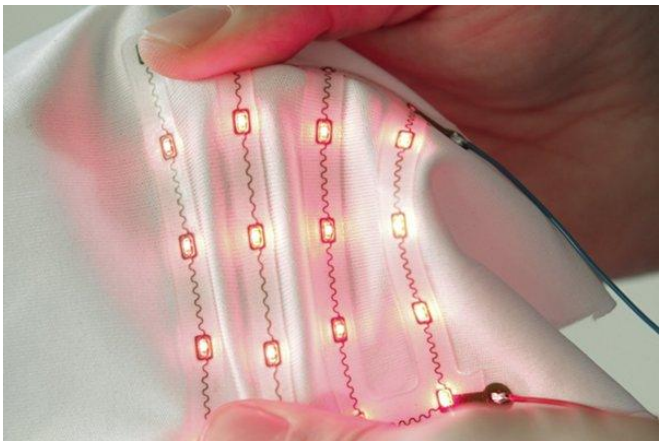


Figure 20 Light Emitting Diodes (LED) on textiles (2013) [39]



Figure 21 Sporty superhero, system includes LEDs, sensors, an on/off switch and a rechargeable battery (2014) [42]



Figure 22 CuteCircuit Twinkle Collection (left) [43] and Cute circuit technology (right) [44]

Examples of integration concepts in patents at integration level 3 (added-on)

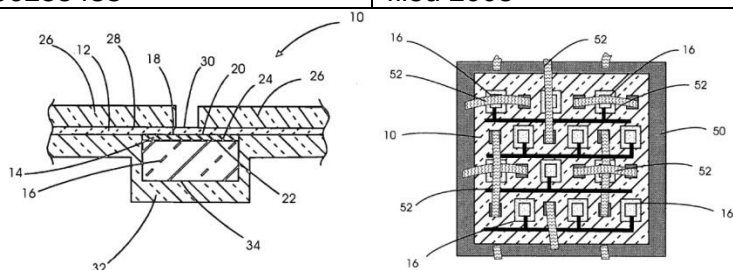
<i>Drapable Liquid Crystal Transfer Display Films</i>	
WO2005072455	filed 2005
Production of a flexible display that can be laminated to a flexible or even drapable substrate (12). Besides glass, metal, paper, textiles and fabric are identified as potential substrates. Here, a substrate is defined as a layer that has a thickness of at least 20 μm. The device itself is composed of a stack of layers on a polymer film e.g. polyvinyl or polyester. The composition of the materials used and architecture applied depends on the substrate in use. The layers listed are: electrode layers (20), liquid crystal-layers (18), protective layers (28),	

insulating layers (22, 24) and light-absorbing layers (16). The display film is able to interact with other components mounted or laminated onto the substrate. The film carrying the electronic function is produced on a so-called release liner (12). After production, it is removed from the liner and can be laminated onto any kind of substrate. Interconnecting electrodes can be, either already incorporated into the substrate or added onto the substrate before lamination.

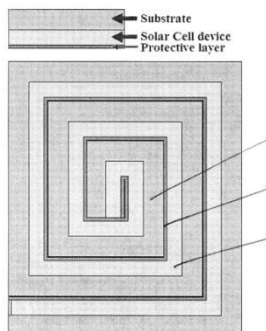
Intelligent Textile Technology Based on flexible semi-conductor skins

US2006255433

filed 2005



The patent describes the invention of a semi-conductor-containing flexible skin (10) for application in intelligent textiles. Here, two flexible polymer layers (26, 32) (e.g. Polyimides, polyetherimide, fluoropolymers, nylons, parylenes, and combinations thereof) sandwich a metal layer (12) (e.g. copper, silver, aluminium, chromium, gold, titanium, platinum), an insulating layer (14) (e.g. insulating oxides, parylene, polyimide) as well as one or several semi-conductive islands (16) (e.g. silicon, germanium, gallium arsenide). The patent does cover weaving as an integration technology. However in this context, the definition does not refer to the basic concept of weaving, but to a weaving technique which is similar to the concept of sewing, whereby a thread fixes the semi-conductor skin to the textile substrate. The textile substrate itself offers the base structure with holes through which the thread is pulled. It is not indicated which device would be attached to the skin, the definition of the concept leads the assumption that transistors might be one of the potential devices.



The application of an electronic film on a textiles substrate is illustrated. This invention comprises a photovoltaic cell and at least one substrate layer and one protective layer. The photovoltaic cell includes at least one semi-conductor, a high work-function electrode and a low work-function electrode. The layered construction is wrapped up forming a e.g. cylinder-like shape. As for the substrate, it is indicated that glass or polymer fibres are suitable as long as they are transparent enough to not disturb the function of the solar cell. Furthermore, it is said that the woven substrate could house the metal electrode.

Examples of integration concepts in research at integration level 3 (added-on)

Bonfiglio *et al* [42] take the first step into flexible micro-electronic device fabrication for textile integration by developing an organic field effect transistor (OFET) in 2003 (Figure 23).

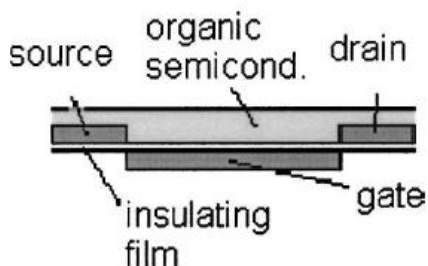


Figure 23

Field effect transistor (OFET) on film [42]

The substrate, a poly-ethylene terephthalate film is the insulator itself therefore makes other rigid substrates redundant. The transistor is processed with a one-mask optolithographic discontinuous process in which the semi-conductor pentacene is evaporated as the active layer. In 2005, Bonfiglio investigated how the performance is influenced [45] when the transistor as described above is glued onto a textile ribbon with a width of 3.5 mm (see Figure 24).

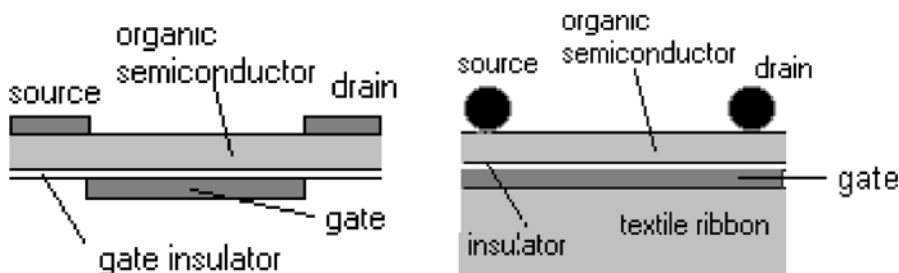
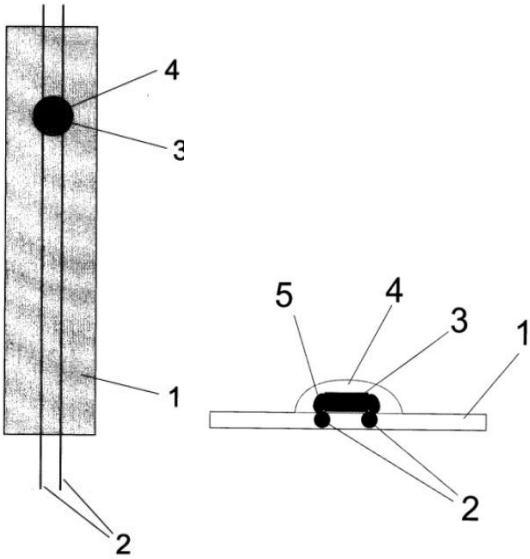


Figure 24 General scheme of a top contact thin film transistor (left) Structure adopted for the device on a textile ribbon (right) [45]

Alternatively, the gold top contacts are placed to define the semi-conductor channel. Here, the transistor showed a lower performance. Cosseddu et al. (2006) [43] tested the effect of applying an organic conductor (Poly(ethylene-dioxythiophene)/polystyrene sulfonate (PEDOT:PSS)) gate electrode by spin-coating. The same organic conductor has been used as top contact generated by soft-lithography. Pentacene was vacuum sublimated as the active layer. The second research paper is not being linked to textile applications but is integral to the present research into this particular substrate.

Examples integration level 3 (built-in)

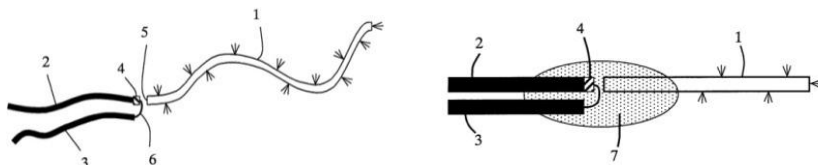
Examples integration concepts in patents at integration level 3 (built-in)

Textile based LED system is described	
2396252 (UK)	Filed 2002
	
SMD LEDs (Surface Mount Display Light Emitting Diodes) (3) are mounted on a textile substrate (1) and encapsulated (4) for durability and washability. The SMD LEDs are small and have a low profile, therefore are suitable for integration on textiles. The textiles substrate itself needs to be equipped with conductive textile tracks (2) by textile processing e.g. weaving, knitting, braiding, embroidery or alike. The LEDs are mounted on those tracks and attached with electrically conductive adhesive (5) (silver filled silicon or epoxy resin). Having attached the LEDs successfully, the entire track is covered with an encapsulation layer of textile silicon sealant, textile or polymer coating for additional durability	

Lichtemittierende Anordnung (light emitting arrangement)

DE10323472

Filed 2003

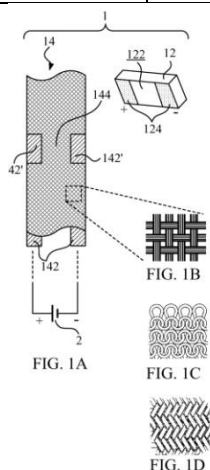


To emit light, a LED (4) is connected via conductive yarns (2, 3) and placed in direction of the cross-section of an optical fibre (1). The LED is attached to electrically conductive threads with conductive glue or by soldering (7). The size of the LED is about $250 \times 250 \mu\text{m}$, at the junction point of the integration; the thickness of such arrangement is approximately 1 mm. The conductive thread is composed of several conductive filaments to keep the overall resistance at a minimum, guaranteeing a stable potential. The light emitted is captured by the optical fibre and transported along the length of the fibre exiting at predefined points.

Illuminating Textile Article

US20100259925

filed 2009



This patent relates to the integration of light. Here, the so-called coupling yarn, a yarn (1A) composed out of conductive and insulating threads is woven (1B), knitted (1C) or braided (1D) into a textile substrate, following LEDs are attached by means of a certain arrangement with two contact points (124) per single LED. There is no indication as to how the LEDs are fixed on the substrate.

Examples of integration concepts in research at integration level 3 (built-in)

Originating in the field of microelectronics, integration level 3 works with flat plastic substrates which can be cut into tapes resembling tapes or lamella. These can be processed by common textile production techniques like weaving, knitting or braiding which, for example are commonly used in the field of geotextiles. Because in weaving, positioning within the textile substrate is most exact, stable and controllable [45] the utilisation of this integration technology is preferred.

The concept for integration of electronic functions into woven structures was proposed as early as 2002 [44]. In 2003, the practical application of the concept by slit-film technique was presented [46]. The material, commonly used in the microelectronic industry, was amorphous silicon. Critical in this integration was a reliable electrical contact (aluminium) between fibres within the woven structure. The contact was generated only by mechanical contact pressure even at fabric drape; therefore the tape was equipped with a curved surface of stressed Silicon Nitride to improve electrical contact [46]. These tapes which are also defined as fibres do carry different micro-electronic components which then can be woven into a fabric with spacer fibres, and conductor fibres. A 50 μm thick polyimide foil (Kapton) was cut into tapes and equipped with stresses Silicon Nitride by Plasma Enhanced Chemical Vapour Deposition (PECVD). Following, the architecture of a Thin Film Transistor (TFT) was applied onto the tape (Figure 25).

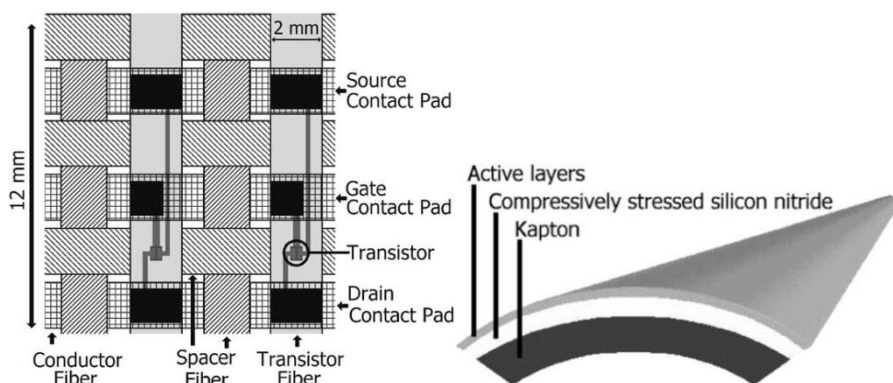


Figure 25 Fibres that are used in the e-textile woven together in a basic pattern (left) desired curvature for the fibres (right) [47]

Kuniyoshi and Tanaka (2003) [48] developed a concept for integrating other components like the field effect transistor (FET) and a photovoltaic cell (PV) taking a similar approach. Micro-electronic components are placed onto plastic tapes which then are woven together with other patterned tapes into a circuit. This concept was further elaborated in 2005 but this time transferred to a kumihimo braided structure with eight threads (square-shaped). The structure resembled a Field Effect Transistor (FET) in which an oxidized, tantalum, wire and gold contacts as well as a layer of phthalocyanine was evaporated. Within the proposed braided structure, gold coated plastic fibre is used to contact the device [49]. Figure 26 shows the braided structure. It is unclear if this structure has been applied.

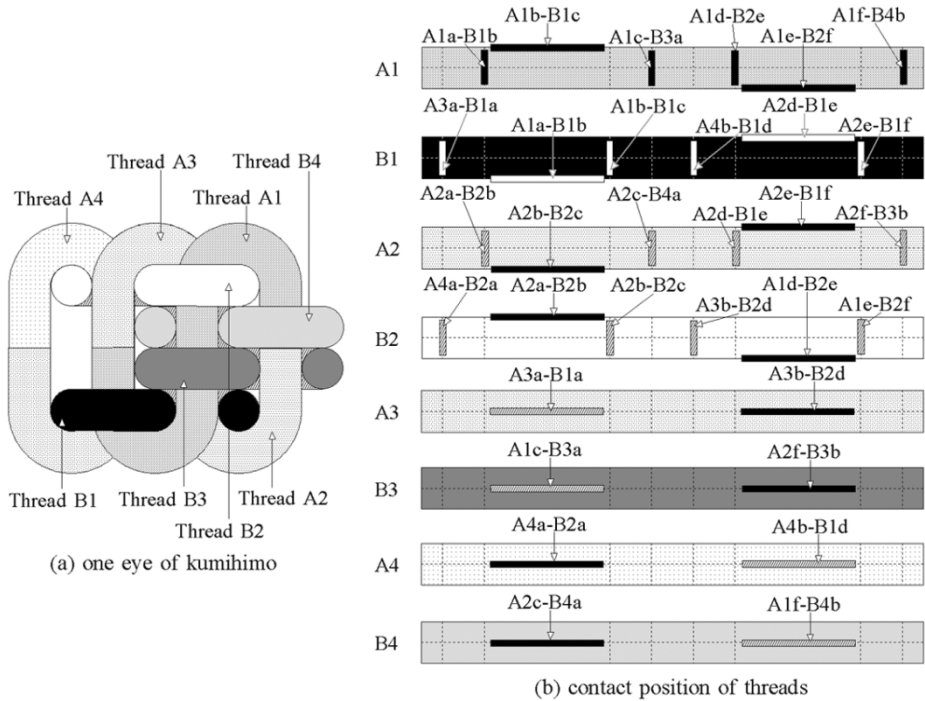


Figure 26 Arrangement of the thread in one eye of kumihimo (left) and single components of this construction indicating contact areas within the kumihimo bread (right) [49]

The integration of tapes or lamella into a woven structure also was successfully pursued by Cherenack *et al.* (2010) [50] in manufacturing an OFET and by Kinkeldei (2011) [51] in making a CO sensor. The substrate was a Kapton E foil (DuPont) onto which the components were mounted and encapsulated. This substrate was then subsequently cut into tapes for integration by band weaving. Both devices were developed with widespread techniques used in micro-electronics industry for producing organic field effect transistors. As for the transistor, chromium (Cr) is used in the gate layer. The dielectric layer is formed by aluminium oxide (Al_2O_3) by atomic layer deposition (ALD). The active layer is amorphous indium-gallium-zinc-oxide (a-IGZO). Gold was used for source and drain electrodes, or alternatively, copper wires were glued with conductive epoxy resin onto the surface of the component. Finally another passivation layer of aluminium oxide (Al_2O_3) was covering the semiconductor region (Figure 27).

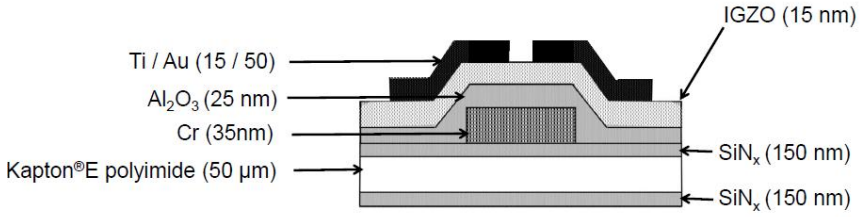


Figure 27 Scheme of smart textile architecture [52]

After processing the flexible lamella devices are integrated by band weaving in Atlas (1/7) pattern. The final structure has been tested for effects on performance during and after bending [52]. The smart textile architecture is shown in Figure 28.

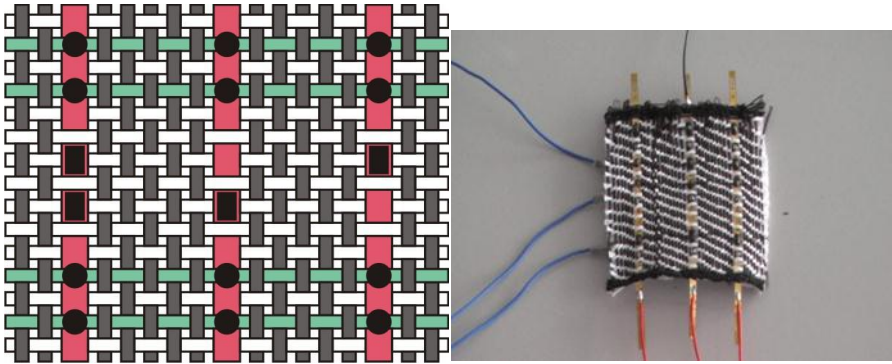


Figure 28 Drawing and image of smart textile architecture[52]

A sensor to detect CO in the environment was integrated in the same manner, by Kinkeldei in 2011 [51]. Polyaniline was used in the sensor's active layer. Furthermore Muenzenrieder (2011) [53] and Kinkeldei (2011) [51] discuss the effect of bending in illuminated conditions in comparison to the effect of bending in dark conditions with regard to transistor performance. The findings show that illumination as well as bending and in combination with each other, do influence the transistor performance. Furthermore, Muenzenrieder emphasises the crucial importance of encapsulating the mounted devices. Zysset *et al.* (2012) [54] show the application of LEDs in the same structure forming a display matrix of 3 by 3 pixels. For this, the

substrate was prepared as described above with addition of SMD (Surface Mount Display) stiffened low current LEDs by conductive adhesive.

Integration level 3 shows flexible electronics being built-in or onto the washable textile material and decreased recognition by touch or sight of the integrated electronic function.

3.4. Integration level 4

Level three demonstrated that the function of the single components is not strongly related to the integration apart from functioning as the interconnections within the circuit. After closer examination of the integration of the function by rigid and flexible electronics, the integration in the textile itself, the so-called full integration will be expanded. The focal point of this section is integration level 4. As the textile product sometimes undergoes a long production chain, there is an opportunity to integrate the electronic function at specific points within the production chain. Answers to question 5 will yield further refinement of the definition of the concept of integration of electronic function, including definition of the level within the e-textile subcategory textronics.

Q5: At which point in the textile production is the electronic function integrated?

There are numerous opportunities to integrate the electronic function at any point in the production chain, from the moment the material is spun into a fibre or filament, to the processed fibre and to the textile structure. As it still concerns a textile substrate, subcategories of integration level 4 have been developed for further analysis.

At integration level 4, a separation of three different types of integration is made:

- A. in/on the textile structure which is a planar substrate;
- B. in/on the fibre or filament i.e. a cylindrical substrate;
- C. in the material, e.g. for spinning the fibre.

The concepts for integration level 4 A-C are mainly evident in research and in patents. No commercial products, based on integration level 4, have been developed date.

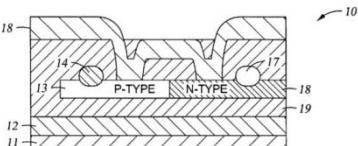
Definition 13: Integration Level 4

There are three different types of integration in Integration Level 4. The electronic function can be integrated in/on the fibre or filament i.e. a cylindrical substrate, in/on the textile structure which is a planar substrate and in the material, e.g. for spinning the fibre. Integration level 4 relates to an integration which is unrecognisable to touch, flexible and washable.

3.5.Integration level 4A

Following the work regarding integrating electronic functions on tapes being flat filament-like substrates, research has developed the electronic function by making the textile substrate an important part of the actual structure. The level 4A is defined by integration into the textile structure by common textile processing technologies like weaving or knitting or simply intertwining. The basis here might be thought of as integration on a planar level, i.e. the fabric.

Examples of integration concepts in patents at integration level 4A (planar)

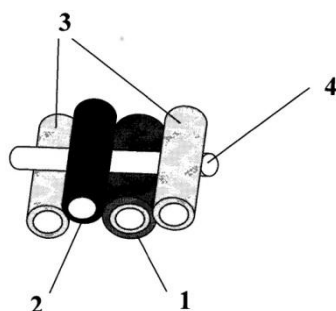
<i>Woven Polymer Fibre Video Displays with Improved Efficiency and Economy of Manufacture</i>	
US6229259	filed 1998
	
This patent describes use of Electroluminescent (EL) fibres in a display concept. The flat-panel display consists of dielectric (19), conducting (14) and semi-conducting fibres (13, 18) that are woven into a fabric. The EL polymeric fibre creates the pixel. Red, green	

and blue EL semi-conductor polymers are used; metal fibres are applied to create the gate. The entire structure is encapsulated ensuring advantageous optical interface parameters with the Luminescent face of the pixels.

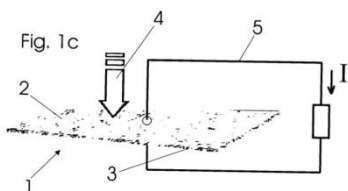
Textile Solarzellenanordnung (Textile Photovoltaic Arrangement)

DE10305162

filed 2002



Description of the application process of a photovoltaic cell in a textile substrate: The electrodes and functional layers are integrated into or onto the textile substrate, i.e. fabric or fibre. The components are a photo electrolyte fibre (1) and an electrolyte fibre (2) which form the photo electrode. The opposite electrode is added in sequence forming one solar cell unit the photo electrode. The pattern is repeated as many times as required. The warp threads (4) in the final woven structure do not have any function in the device but should be optically transparent to support the performance of the integrated PV. Possible materials for the electrodes i.e. conductive material are silver, gold or platinum applied by galvanization, as for the semi-conductor, zinc-oxide (ZnO) is suggested. A redox electrolyt layer is applied as an intermediate layer. The architecture can also be applied to one single filament and will be further described in the section for integration level 2B single.



The invention relates to textile photovoltaic cells. In comparison to earlier inventions in which fibres are combined in one textile structure to generate the function, this patent describes the combination of two textile structures (2, 3) or layers that combined into one textile structure and at least partly connected. The two textile layers represent the carrier layers and are made of different materials, one is a photovoltaic acceptor material, the other a donor material. The suggested preferred carrier material is silicon carbide (SiC) because of the properties of transparency, chemical and thermal stability and hardness. The active material is applied in a film-like fashion i.e. wetting or coating onto the woven or non-woven structure. The active material or semi-conductor consist of, for instance. Zinc Dioxide (ZnO₂) or Tin dioxide (TiO).

Examples of integration concepts in research at integration level 4A (planar)

Hamedi *et al.* (2007) integrated an electrochemical transistor (ECT) into a woven structure [55]. In this particular ECT, the transistor channel consisting of poly(3,4-ethylenedioxythiophene (PEDOT) is switched through a reversible redox reaction with electrolyte i.e. a mechanism of doping and de-doping. To target textile integration, the architecture is applied onto a wire (wire ECT or WECT). One option for constructing the WECT is the crossing of two PEDOT coated fibres and adding the contact of electrolyte at the junction. Two Polyamide, Kevlar or polyester monofilaments drop-cast coated (in longitudinal direction by gravity) with PEDOT doped with poly(styrenesulfonate) (PSS) at a layer thickness of about 300 nm are crossed. A solid polymer electrolyte from solution creates the ionic contact.

For comparison, a planar micro-ECT was manufactured and I-V characteristics compared. Those were shown to be similar to the WECT. The similarity is explained by the fact that performance is defined by interface of the conductor and the electrolyte. Since the electrolyte covered the entire circumference the potential was similar to the planar architecture. Also in ECTs the operating voltage is determined by the distance between the active channel and the gate layer. This WECT has a number of clear advantages in comparison to conventional field effect transistors, such as, independence

- in dimension
- from displacement
- shape or amount of electrolyte
- local geometry of the substrate

It creates a redundancy of geometry stability and position [55] which meets the demands of textile processing. Furthermore, the technique as described above makes costly patterning processes like lithography superfluous.

Moreover, the nature of the filament allows placing several transistors in a row and therefore varying the size of the devices. The structure is able to serve as simple interconnection if a polymeric conductor is applied at a fibre junction instead of the electrolyte. The disadvantage of this concept, being the switching speed, was successfully resolved in 2009 [56] (Figure 29).

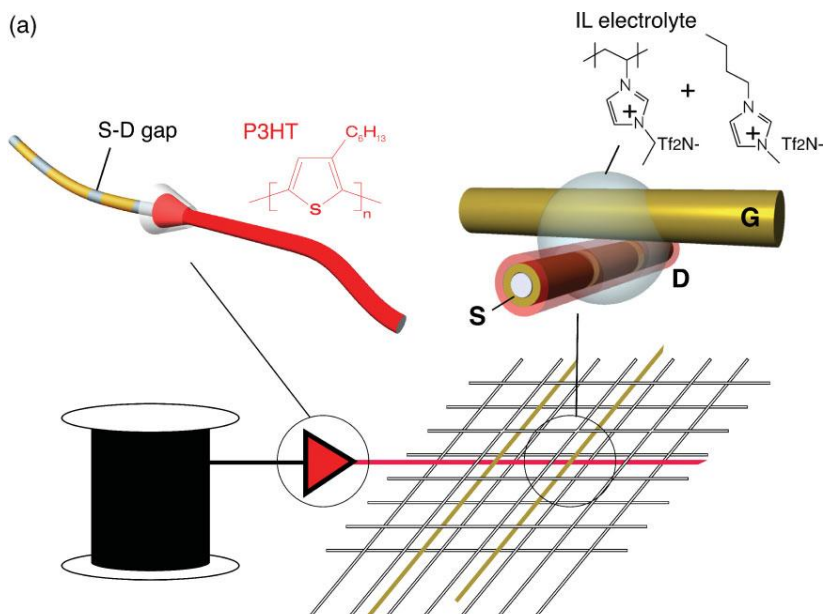


Figure 29 Schematics of: P3HT coating on top of fibres, with pre-patterned source-drain gaps weaving of electrolyte-gated OTFT (top-left). Transistor formed at a fibre junction connected by an IL electrolyte (top-right) and weaving of transistors/devices using different fibres (bottom) [56]

Interconnections between the different conductive filaments are generated by other conductive fibres, as described previously, solid electrolyte is applied onto the junction. In this architecture, source and drain electrodes are manufactured by applying evaporated gold onto a woven polyamide structure in which covering fibres serve as mask for the channel to be formed on the underlying filament. The patterned filament is removed from the woven structure for further use as patterned yarn. Poly(3-hexylthiophene-2,5-diyl) (P3HT) is dip-coated onto the gold coated filament. The solid ionic liquid (IL) electrolyte is a mixture of 1-butyl-3-methylimidazolium bis(trifluoromethanesulfonate) ([bmim][Tf₂N]) and the polymer ionic liquid poly(1-vinyl-3-methylimidazolium bis(trifluoromethane sulfonimide)) (poly(ViEtIm) [Tf₂N]) [56].

In this context the electrolyte is used as a gate dielectric layer allowing flexibility in fibre arrangement e.g. distance between gate and channel. Figure 30 shows microscopic images of two transistors.

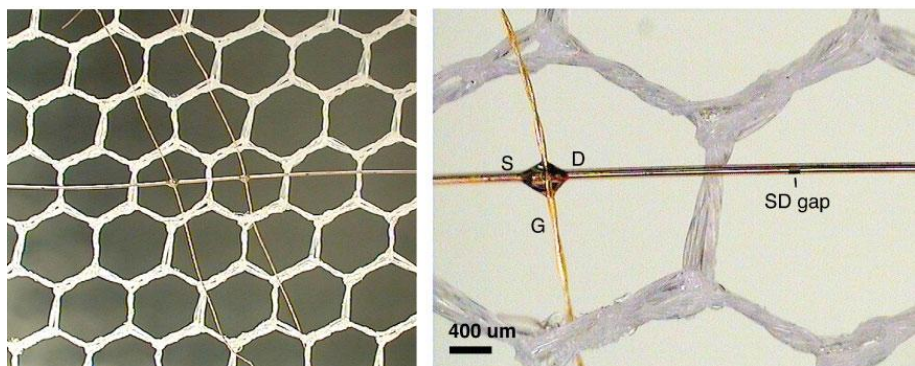


Figure 30 Microscopic image of two transistors created along the horizontal fibre, all woven in a tulle (left) and a close up of a fibre transistor (right) [56]

The concept of WECTs also has been tested on silk (*Bombyx Mori*). Mueller (2011) [57] reports a dip-coating process on a silk yarn composed out of several monofilaments by submersion in the conductor material poly(4-(2,3-dihydrothieno[4-b]-[1,4]dioxin-1-yl-mthoxy)-1-butanefulfonic acid (PEDOT-S). Also in this architecture the active channel is defined at the crossing region of two yarns by drop-casting the electrolyte from IL:PIL as described above. The silk fibre-based ECT is shown in Figure 31.

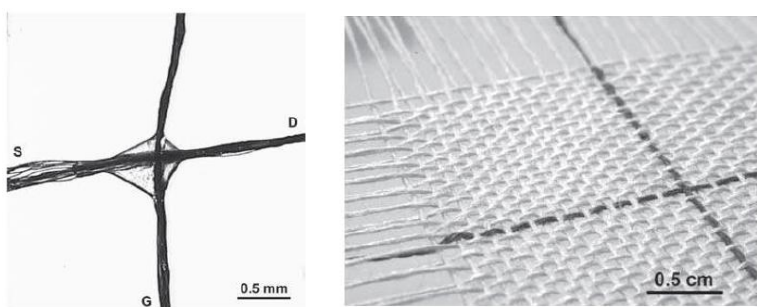


Figure 31 Microscopic image of a silk fibre-based ECT devices with source (S) drain (D) and gate (G) (left) and a photograph of a basket-weave fabric manually woven with pristine as well as PEDOT-S stained silk thread (right) [57]

At the application of sufficiently positive gate voltage (V_{GS}) the PEDOT:PSS, the reverse redox process changes conductivity in the channel region by doping and de-doping. In this architecture the switching speed does seem to be problematic because the timing is influenced by the electro-chemical response time and the area of the channel. Faster de-doping could be achieved by increasing the contact area of the coated fibres by allowing the electrolyte to cover the areas between the fibres within the multifilament, this penetration or increase in area to volume ratio, has been tested [58]. A solution with higher viscosity decreased the switching speed considerably (Figure 32).

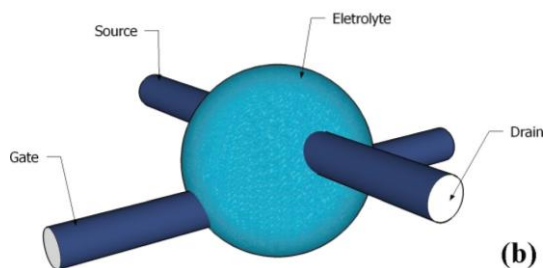


Figure 32 Topology for a wire electrochemical transistor (WECT) [58]

In 2011, Mattana *et al.* [59] present an ECT by combining cotton threads with different conductivity. A cotton thread is subsequently soaked in aqueous PEDOT:PSS and for the purpose of encapsulation, in ethylene glycol (EG). This semi-conductive yarn is inserted with a needle in a gel from KCl in ionized water and with gelling agent (Bacto Agar). The gel bridges the gate and semi-conductive channel. The semi-conductive yarn is then knotted on each side to each one conductive yarn. These conductive yarns are cotton yarns with a coating of highly packed density Au Nano particles (Au NP). A thin layer of tosylate-doped PEDOT (PEDOT:tos) was applied to on top of the gold coated yarn. For this process, a solution of isopropanol, Fe(III)-tosylate and pyridine was prepared in which the yarn was soaked [59]. The scheme of an OECT on cotton yarns is shown in Figure 33.

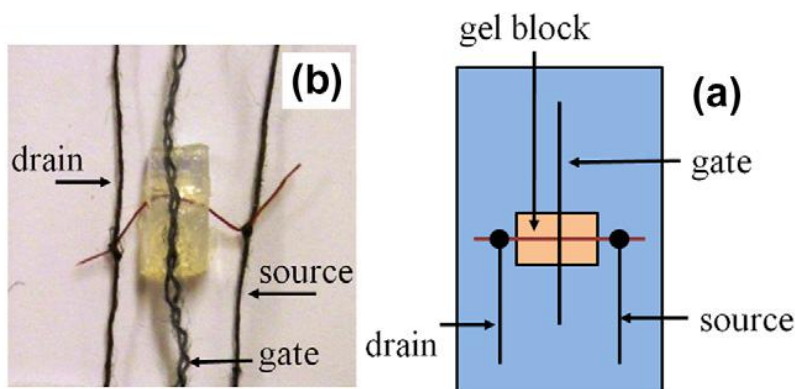


Figure 33 Scheme of an OEET on cotton yarns (left) and realisation (right) [59]

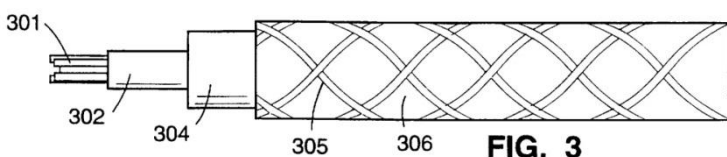
The two conductive yarns act as source and drain electrodes. An additional gate conductive thread is added on top of the surface of the gel in which the semi-conductive yarn was placed. Transistor effects have even been achieved at non optimal ratio between on and of currents (I_{ON}/I_{OFF}).

3.6. Integration level 4B

Level 4B addresses concepts dealing with cylindrically shaped substrates. This can be filaments or fibres but also yarns. Fibretronics as such are part of textronics which is a subgroup of e-textiles within the field of smart textiles.

Examples of integration concepts in patents at integration level 4B (cylindrical, multiple parts)

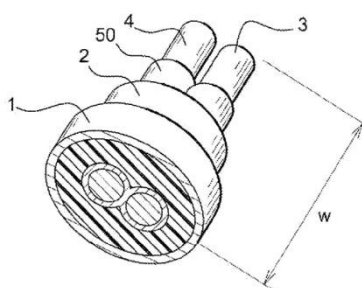
<i>Electroluminescent Filament</i>	
WO9724015	filed 1996
A conductive multifilament (301) is surrounded by an insulating layer (302), followed by another conductive layer (304) and a layer of electroluminescent phosphor is applied (306). Optionally, another insulating layer can be applied on top of this construction into which the braided outer electrode is embedded or onto which the braided electrode is placed (305). The braided outer electrode covers about 50% of the surface. This is only an example of the concept, material and architecture can be adapted as appropriate.	



Transistor a source et drain filaires

EP2209146

filed 2010



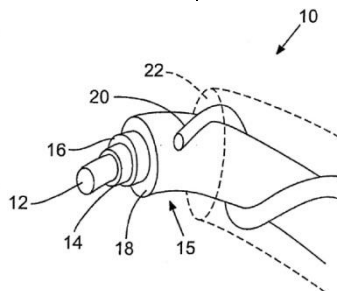
The architecture of the transistor fibre resembles a Top-Gate Bottom-Contact architecture commonly applied in the field of micro-electronics. The source and the drain are two separate fibres e.g. silver wires (3-4), each made of conductive material and coated with a semi-conductor (50). These two fibres are then placed next to each other and coated with an insulating layer (2). On top of the insulating layer, another conductive material is applied to build the gate layer of the transistor (1). As for manufacturing techniques, spin-coating and lithography are discussed.

Fibre-Based Electric Device

US20090103859

/ 2011 /2008

US20110308077



Core different electric components could be manufactured depending on which layered architecture is applied on top of the elongated fibre. As examples photovoltaic (PV) devices are mentioned, as well as, Light Emitting Diodes (LED) or thermoelectric (TE) devices.

Furthermore, an example of the various layers to be deposited onto the core is given. The core should be either an aluminium fibre (12) or an aluminium coated fibre, followed by an anode (14) which also could be a conductive polymer, an organic semi-conductor (16), and a cathode (18). In addition, it is pointed out that some devices require an additional conductive wire to be wound helically around the coated fibre core. This wire serves as electrical contact to the cathode. Addition of the extra conductive wire, merits classification in integration level 4B multiple since more than one substrate is combined to generate the function of the device.

Examples of integration concepts in research at integration level 4B (cylindrical, multiple parts)

Also Tao (2011) has conducted research regarding the option of applying electrolyte as gate dielectric layer in an Electro Chemical Transistor (ECT) architecture. Two PEDOT:PSS solution coated Kevlar filaments are intertwined like in a yarn representing the gate, source and drain electrodes [58] (see Figure 34).

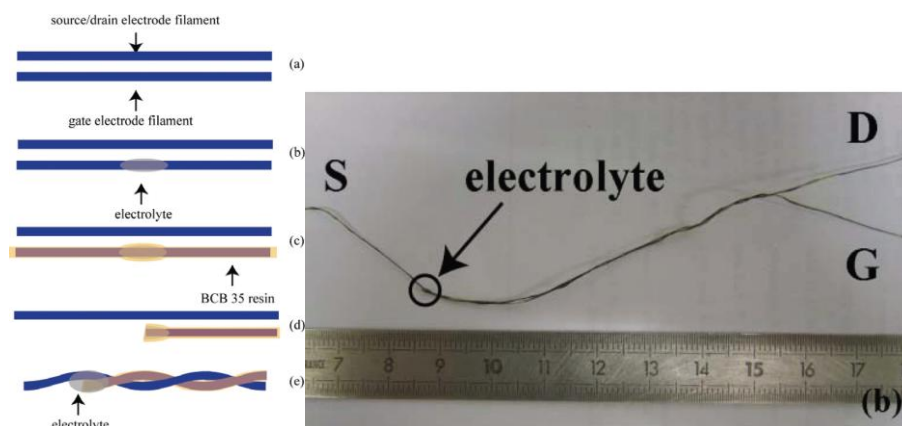
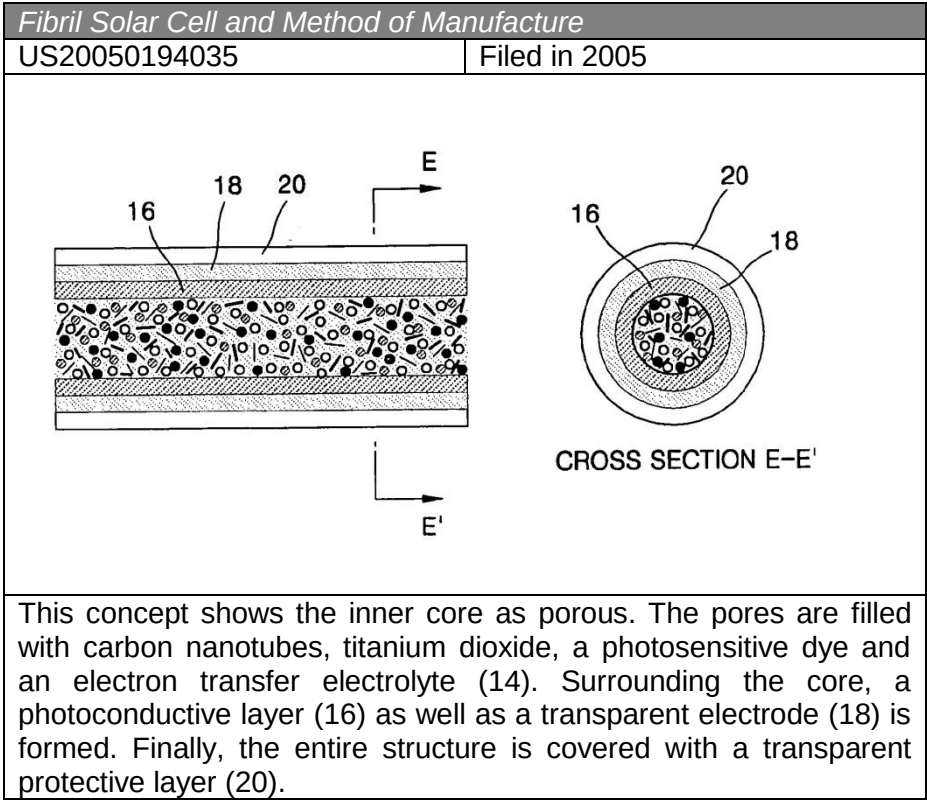


Figure 34 The scheme of WECT construction in form of a thread (left) and the image of twisted wire electrochemical transistor (right) [58]

The electrolyte, here a mixture of PSS, glycol and D-sorbitol, water and NaClO_4 , is applied by drop-casting to one spot on the gate filament. Subsequently, the gate filament is covered by dip-coating in Cyclotene 3022-35 resin (BCB35) for additional insulation. After the gate filament is cut in the middle of the electrolyte, the two filaments are intertwined. The cut end of the gate filament is glued with another drop of electrolyte on top of the source-drain filament, resulting in Y-shaped geometry. Besides showing the general advantaged of ECT in contrast to Thin Film Transistor (TFT) architecture. Inflexibility of resin and electrolyte changing the handle and drape of the textile substrate, however, might be disadvantageous.

Examples of integration concepts in patents at integration level 4B (cylindrical, one part)



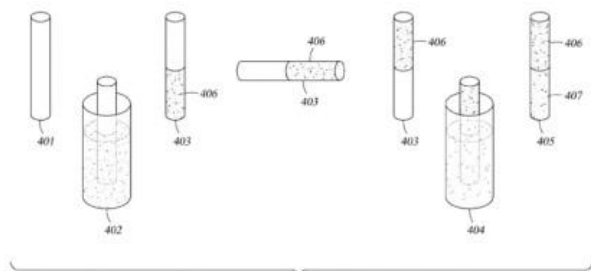
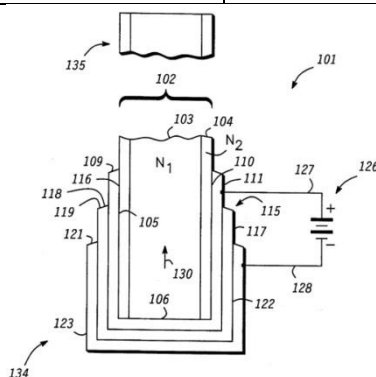


Fig. 4

A variety of so-called embodiments or concepts are addressed. For application as photovoltaic cell, a conductive layer (402) is deposited onto an optical filament (401). Between the second electrode and the first, a continuous semi-conductive layer (406) is added. This semi-conductor absorbs electromagnetic radiation turning it into an electrical signal. Whereas two types of materials are used in the semi-conductor region (407). In particular, dip-coating is mentioned as one production technique used to manufacture the component.



A conductive layer (109) is deposited on an optical fibre (101), following a light emitting layer (115) and a second conductive layer (121). The conductive layers are applied by sputtering, the semi-conductor by evaporation. As semi-conductor material tris(8-hydroxyquinoline)aluminium (Alq3) is used in the emission layer, diamines, Phthalocyanines and oxadiazoles in the hole transport layer, indium titanium oxide is applied for the first electrode layer.

Examples of integration concepts in research at integration level 4B (cylindrical, one part)

The concept of the power fibre a solid-state thin-film rechargeable electrochemical battery was first presented in 2001. In 2003, Neudecker *et al.* show the application of the battery architecture on a variety of substrates and materials by vacuum deposition (magnetron sputtering or electron-beam evaporation) [60]. Figure 35 shows the power fibre and composite.

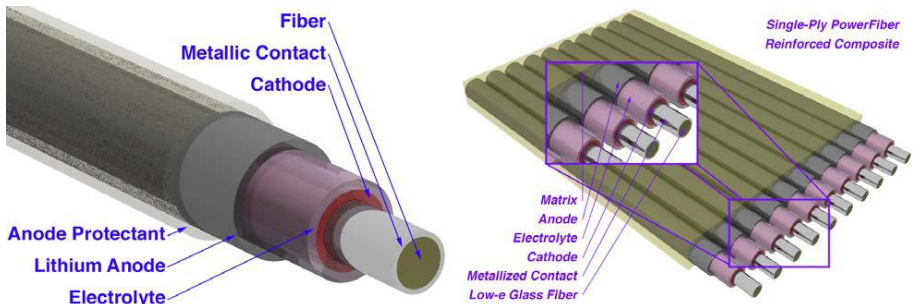


Figure 35 Individual PowerFiber (left) and PowerComposite (right) [60]

Tested Substrates included sapphire, SiC, carbon, borosilicate glass, Cu, stainless steel, Inconel, NiTi shape memory polymer and Ti6-4. The various configurations comprised Li-free, inverted Li-free, Li-ion, inverted Li-ion and Li-metal. In most cases the electrolyte was lithium phosphorus oxynitride (Lipon). The positive cathode material (nanocrystalline $\text{Li}_{1.6}\text{Mn}_{1.8}\text{O}_4$, nanocrystalline $\text{Li}_2\text{V}_2\text{O}_5$ or crystalline LiCoO_2) determined the choice of cathode current collector (ccc) material, namely, Cr, Cu or Au. Most promising results have been achieved with nano-crystalline cathodes $\text{Li}_{1.6}\text{Mn}_{1.8}\text{O}_4$ and $\text{Li}_2\text{V}_2\text{O}_5$,

A fibrous transistor was presented by Lee and Subramanian in 2003 for the first time. Al wires were used as gate which was insulated with a low temperature oxide (LTO) gate dielectric [61]. The semiconductor pentacene was evaporated onto the dielectric surface. Finally, the source and drain contacts were applied by evaporation of gold. Curvature or increased roughness of the layers did not affect transistor performance. In general ordering of the crystallisation in the

film defined the performance of the layer. Decreasing surface roughness by using a polished stainless steel fibre in addition to smaller contact areas of source and drain resulted in higher dielectric quality (Figure 36).

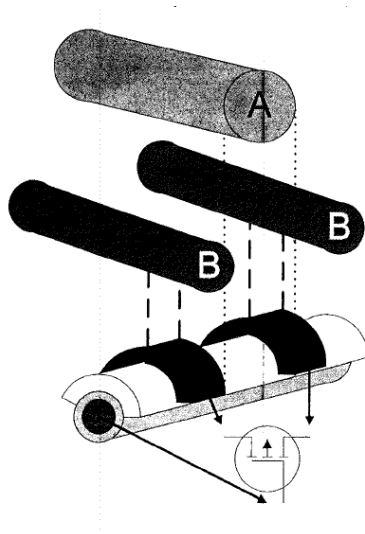


Figure 36 Transistor generated by combination of multiple fibres [61]

The described architecture was further elaborated by Lee (2005) [62]. The gate dielectric was substituted with cross-linked Poly-4-vinylphenol (PVP) on the one hand to avoid CVD which is not textile process-compatible and on the other hand to decrease gate leak current.

In addition to a review of materials (2006) [63] within the EC funded FP6 project ProeTEX, in 2007, a range of concepts for developing transistors on fibres were described [64]. In addition to the concepts cited above, i.e. previously shown configuration of the transverse electrode, the longitudinal electrode, and the spiral electrode configurations is suggested. Each configuration has its advantages and disadvantages related to channel dimensions, textile processability and ease-of-use after integration (Figure 37).

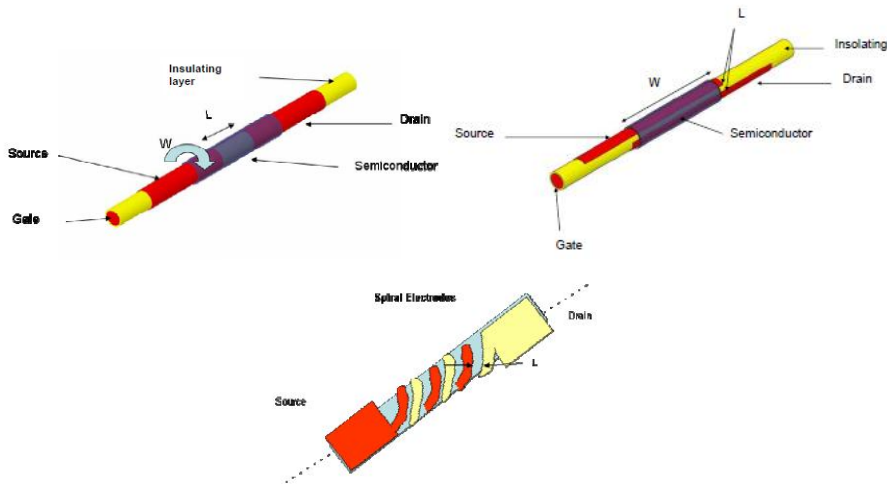


Figure 37 Variation in contact electrode arrangement: transverse (top-left), longitudinal (top-right), spiral (bottom) [64]

The research group at University of Cagliari also examines the application of an OFET on one single fibre. Maccioni *et al.* (2006), showed the top-contact bottom-gate architecture of a wire which represents the gate electrode within [65]. The wire is equipped with a dielectric of polyimide (Elektrisola). The organic semi-conductor pentacene is thermally evaporated onto the structure and serves as active layer. The substrate has not been rotated during evaporation and therefore, only approximately half of the wire's circumference is covered. As for the source and drain electrodes gold is either evaporated using masking fibres for defining channel dimensions with less precision or by applying PEDOT:PSS through a soft lithographic process with greater precision.

Since 2007, the research group at Ghent University has been working on applying the bottom-gate-top-contact transistor architecture in transverse electrode configuration onto a filament. The substrate in this context is a polyester filament that is first coated with copper by electroless-deposition to generate the gate. Subsequently, the gate dielectric is applied by dip-coating in a solution of polyimide [66, 67]. The organic semi-conductor is applied using the same process technique, dip-coating a solution from TIPS-pentacene. In addition to the results on the polyimide layer, current work and the semi-

conductive layer and application of nano-silver source and drain electrodes by drop-casting or ink-jet printing is also subject of the technical part of this dissertation. Promising results though on the dielectric layer as well as on the active layer and electrodes are discussed in Part II of the dissertation.

In 2011 Mattana *et al.* present research regarding TFTs on a cotton fibre in which the core is a cotton thread subsequently soaked in an aqueous solution of PEDOT:PSS and ethylene glycol (EG). Although this is a semi-conductive layer it will act as gate electrode because its resistance per unit length ($2 \times 10^3 \Omega/\text{cm}$) allowed considering the layer as conductive at the voltage used for operating the transistor [59]. Figure 38 shows the structure of an OFET on a cotton yarn.

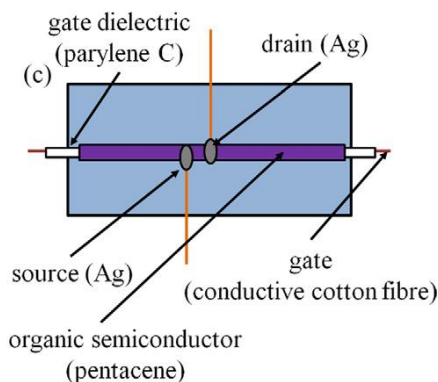


Figure 38 Scheme showing the structure of an OFET fabricated on a cotton yarn [59]

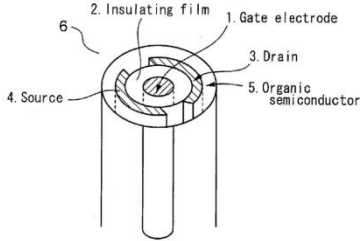
In addition, this semi-conductive layer shows a lower roughness than conductive cotton fibres (Au NP + PEDOT:tos) and is therefore a more effective prerequisite for subsequent deposition of the dielectric layer. The gate dielectric with an approximate thickness of $1.5 \mu\text{m}$, is formed by chemical vapour deposition (CVD) of poly(chloro-p-xylene) (Parylene C) onto the entire surface of the fibre. The semi-conductor pentacene is then applied by thermal evaporation. It is uncertain how coverage of the entire fibre by CVD or evaporation has been achieved. Two droplets of conductive silver paint form source and drain electrodes and are applied with a very sharp needle. There is no detailed description of circumferential application of the source

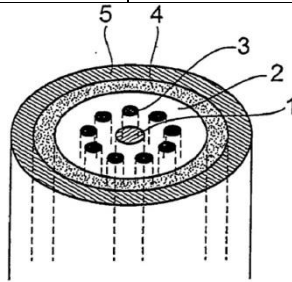
and drain as well as how the contacts have been contacted to enable further measurements [59].

3.7. Integration level 4C (material)

Integration level 4C deals with an electronic function within the material itself. Only a combination of materials generates the active electronic component’s function. This level targets the point within the textile supply chain in which material is transformed into cylindrical substrates. Here evidently, spinning of man-made fibres illustrates the process. A variation of material is combined by spinning into a cylindrical substrate. It might be also argued that this finally is a cylindrical substrate and should belong to integration level 4B. The rational for clearly defining this level is that before spinning the materials into one cylindrical substrate, there textile substrate is non-existent, whereas in level 4B the substrate exists and is either coated or combined with other parts.

Examples of integration concepts in patents at integration level 4C (material)

Line Element and Method of Manufacturing the Line Element	
US20050253134	Filed 2003
	
The patent describes the method of continuously producing the line element being e.g. photovoltaic cell diodes or transistors. Depending on the device to be manufactured, the extruded filament has a number of different sections and materials. Several cross-sections are presented, the extrusion die can be chosen accordingly. This patent belongs to integration level 2A since the materials are extruded as one component, subsequent coatings or alike are not necessary.	



The devices are integrated into on so-called linear elements which may be combined into a planar light-emitting device by for instance knitting. This patent is related to the processing technique.

Examples of Integration Concepts Used in Research at Integration Level 4C (material)

Research regarding microelectronic components on materials level has not been found. It is emphasized again, that sensor materials as such e.g. shape memory polymer, are excluded from this analysis. In this dissertation, the focus is on electronic devices e.g. transistors, light emitting diodes, photovoltaic cells, etc.

More information about the material used in the sandwich architecture of the components identified above (p. 109) will be furnished as part of technical section of this dissertation (see section: Materials – chapter 6).

4

Challenges

The aim of Part I of this dissertation has been to develop a scheme which enables classification of concepts at the same technological level i.e. integration level. Chapter 4 completes the classification, summarizes the findings and generates the link to the experimental work in Part II of this dissertation. Based on chapter 1-3, challenges related to the technical field of textronics (integration level 4) have been identified and are listed in chapter 4. This overview introduces to the complexity in the experimental work shown in chapter 7-10.

To complete the review of smart textile systems with five components, this scheme has been supplemented with an additional scheme for evaluating the addition of interconnections and connectors.

In today's smart textile products, textile interconnections are used as standard in combination with all component integration levels. Non-textile interconnections are marked with - symbols, for example, interconnecting wires lead to an addition of a -. The symbol is added to the final level, e.g. 4B⁻ (non-textile interconnections) vs. 4B (textile interconnections). If there is only wireless interconnection, the integration level remains untouched.

The connectors are entered into the scheme last. The symbol ° is added for non-textile connectors to the interconnections achieving integration level 4B° (non-textile connector). For example, level 4B containing non-textile connectors and interconnection would be classified within level 4B°. The sequence of question for defining the integration levels is shown in Figure 39 and Figure 40.

If interconnections and/or connectors are present, their textile nature is prerequisite for integration level 5.

Definition 14: Integration Level 5

Integration level 5 can only be reached if all components within the smart textile system are classified in integration level 4. In addition, also the connectors and interconnections need to be of textile nature. Alternatively, integration level 5 can also be reached with a technical concept like electronic skin. The entire system should not be recognizable to touch, flexible and washable.

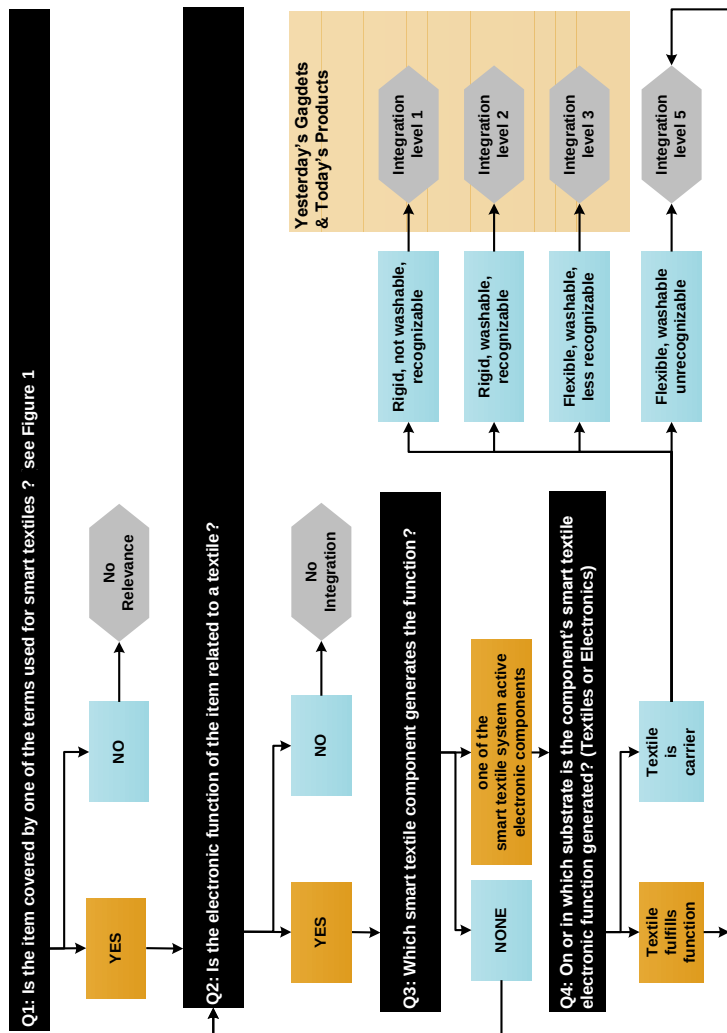


Figure 39 Sequence of questions for defining integration levels (1/2)

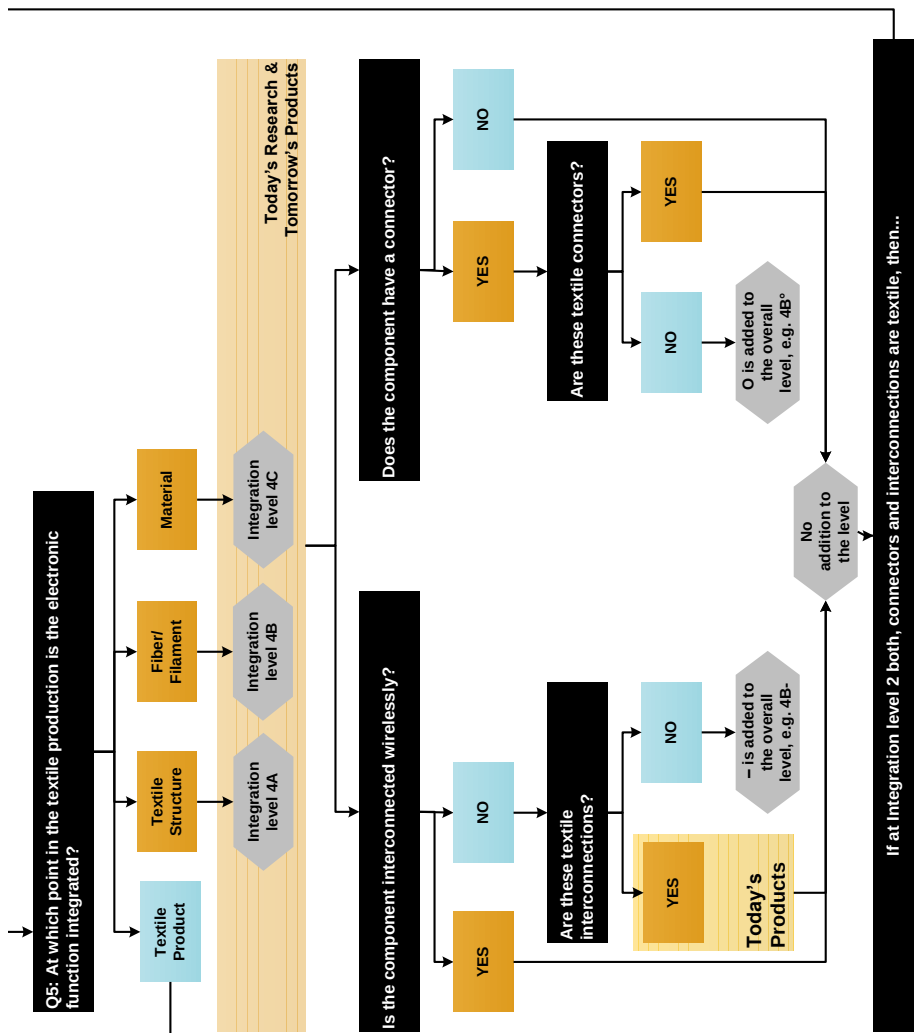


Figure 40 Sequence of questions for defining integration levels (2/2)

The classification according to integration levels for making existing technology comparable was tested and verified in chapter 3. Here, a variety of items from products to patents and research were analysed.

In addition to reviewing products and research papers at each integration level, a total of 175 patents were analysed as well of which 52 patents were identified as related to the field of smart textiles (excluding wearable electronics). Regarding integration levels, of those patents related to smart textiles, eight were classified as belonging within integration level 3, eight within level 4A, 35 in 4B and two within 4C (see Figure 41).

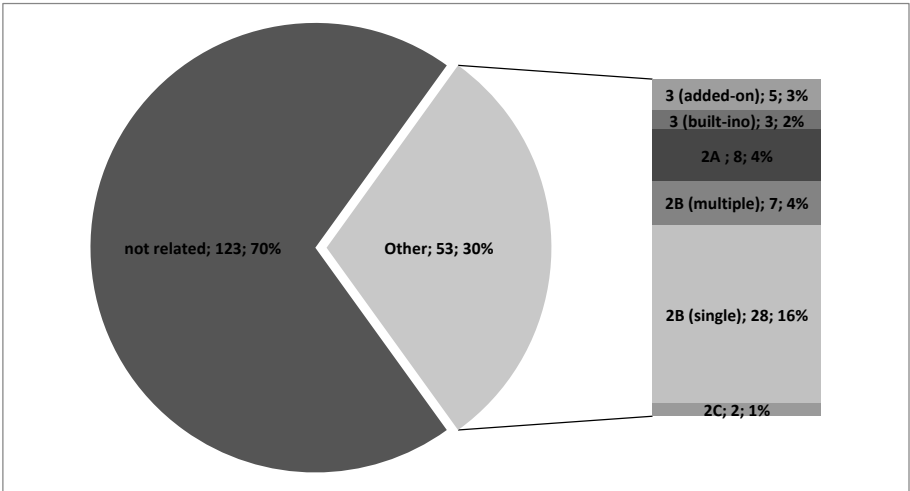


Figure 41 Patents categorized according to their integration level

For the total number of patents analysed, see: Annex B.4. of this dissertation.

The analysis of products, research papers and patents identified following challenges for further research at the various integration levels.

The challenges in the integration levels 3 and 4 (A-C) are:

- reliable electrical contacts in woven structure
- positioning for making contacts within the system
- one-mask opto-lithographic discontinuous process on flexible substrate

- low performance, due to dimensions of the channel and contact resistance
- sensitivity of organic materials
- bending behaviour
- effect of environmental conditions

In research as well as in industry the integration levels are apparent. However, the lack of a universal classification system for smart textiles was impeding progress of applied research. The utility of the development of a new universal classification system is shown, based on verification and finding of this dissertation.

Having established a share conceptual level, this new, universal classification system of integration levels can be used as a guideline in comparing technologies. The new classification includes only e-textiles or textiles bearing an electronic function. It enables a better understanding of the concepts themselves, and even more important the identification of challenges at the different levels of integration. Part II of this dissertation will use the collected data of the related level to derive answers to technical questions related to fibrous transistors, based on the analysis undertaken in Part II of the dissertation.



Part II Fibrous organic field effect transistor

In Part I, the smart textile system with e-textiles as a sub-group has been reviewed. Based on a comparison between the active electronic components, technological concepts were related based on their technical integration level. Part II covers the experimental aspect of this work. It describes the production of a fibrous Organic Field Effect Transistor (OFET). The integration of the electronic function is completed at integration level 4B single, i.e. the integration on fibre level. The fibrous OFET is therefore allocated to the field of textronics.

5

Experimental endeavour

Chapter 5 introduces the concepts of different transistors, their working mechanism and way of manufacturing a field effect transistor. In addition, the translation of the architecture of a planar organic field effect transistor (2D) onto a cylindrical fibrous substrate (3D) is explained.

The area of smart textiles is highly multidisciplinary and therefore, includes aspects from the scientific fields of textiles and electronics. Material science, as well as physics and chemistry have an increased relevance. In addition to academia, industry research also aims to develop truly integrated textile electronics [28-30]. True integration points at a textile substrate incorporating an electronic function, invisibly integrated and undetectable by touch. To achieve this level of integration, the textile substrate itself needs to act as an electrical component, and should independently fulfil the electronic function of a resistor, capacitor or transistor. Referring to Part I, this relates to integration levels equal to level 4 or higher.

Items classified in integration level 4 belong to the category of textronics. To manufacture textronic components, often deposition of multiple layers with different functionalities is required. In this respect, manufacturing techniques from the electronics industry need to be adapted to the textile substrate's versatile properties, such as flexibility or elasticity [31-34] and surfaces with curvature. In integration level 4B (single), substrates are on the whole cylindrical in shape. If materials are deposited onto this three-dimensional body, they respond to the curvature in different ways and for example, the layer's adhesion or crystallisation [35] is susceptible to influence. It is essential to know how to transfer materials used in electronics onto textile substrates to generate a basic electronic function. The transistor serves as an electrical switch or an amplifier. Once the techniques are understood, this knowledge will serve as base for the further development of sophisticated smart textile system active components, including the futuristic concept of the wearable computer.

5.1. Nerve cell of information technology

The transistor is one of the most important discoveries in the 20th century. Bell Laboratories demonstrated the first transistor on December 23, 1947 [68]. The name transistor derives from the combination of two words: transfer and resistor - a transforming resistor - a transistor. In 1947, a semi-conductor was incorporated in the transistor. This semi-conductor could change its properties from being insulating to being conductive. Because of this feature, when it

was integrated into a transistor, the transistor could serve as an on/off-switch and as an amplifier for electrical signals [69].

In 1956, the Nobel Prize in Physics was awarded jointly to William Bradford Shockley, John Bardeen and Walter Houser Brattain "for their researches on semi-conductors and their discovery of the transistor effect" [70] (Figure 42).

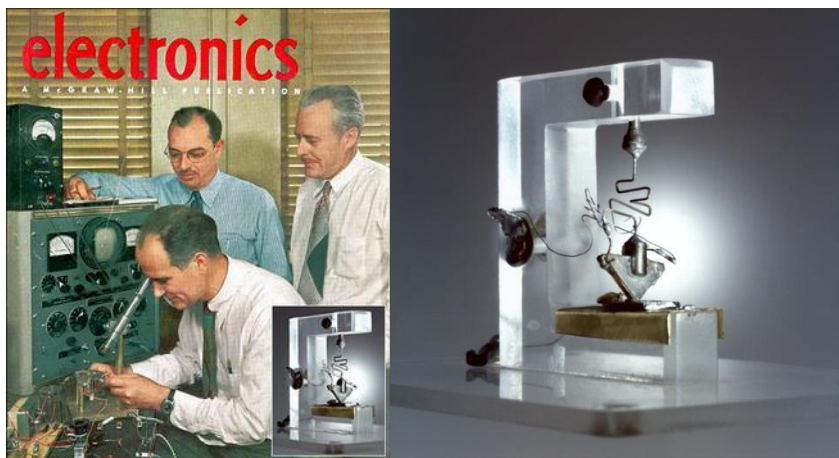


Figure 42 William Bradford Shockley, John Bardeen and Walter Houser Brattain (left) [71], the first transistor (right) [72]

There are plenty of examples of transistors in objects used in daily life. One of the first devices containing transistors was the transistor radio. Before its commercial introduction, many persons laid claim to being the inventor of the transistor and there have been many prototypes were produced. Truth is that the first transistor radio Regency TR-1 was commercially produced by the American companies: Instruments of Dallas, Texas and Industrial Development Engineering Associates (I.D.E.A.) and brought on the market in 1954. It contained exactly 4 transistors [73]. Figure 43 shows the Regency TR-1.



Figure 43 First transistor radio the Regency TR-1 at the exhibition of the San Francisco Airport “The History of Audio: The Engineering of Sound [68]

Until the 1950's, radios contained vacuum tubes as amplifier elements instead of transistors. Once the transistor was discovered, radios could be made much smaller, needed less power (lower voltage), and were more shock-resistant. Also, with transistors the radio could be used immediately, in comparison to vacuum tubes which had to warm up beforehand [68].

The transistor radio was also called the crystal radio since it contained a crystal to replace the vacuum tubes used previously. The crystal was composed out of a semi-conductor material like galena (lead sulfide), iron pyrite (fool's gold), zincite (zinc oxide) and germanium or silicon. Based on the impurities within the semi-conductors, the detection and amplification of radio signals became possible.

In 1954, the Regency TR-1 was available for US\$ 49.95 (today's equivalent of US\$ 435) and sold about 150,000 times. This radio was not only a huge scientific success but also from the commercial point of view a historical milestone. These days, transistors are mainly used in integrated circuits (IC) which are crucial for the function of computers. Therefore, the transistor is also called “the nerve cell of the information technology” [69].

Logically, thinking in terms of full integration of electronics into textile material, the transistor is one of the major components to be

transferred from rigid electronics to flexible textronics. Once this is achieved, this process can be repeated with less effort using other components which are built in a similar fashion i.e. in thin layers. Finding means of integration will be ground breaking and pave the way for further research in the field of textronics.

5.2. Transistor function

A transistor is an active electronic component which can be connected to other electronic components like resistors, capacitors, inductors, or diodes (see also Definition 3 in chapter 1). To understand the mechanism in transistors, it is crucial to understand the mechanisms in diodes first. A diode is a component that blocks current in one direction while letting current flow in the opposite. Electronic devices that use batteries often contain diodes to protect the device from potential current leaving the battery, in case the battery would be inserted in the wrong direction. This way the diode protects the sensitive electronics in the device [74].

Basically, diodes are made out of a low and a high resistance material. This combination of materials enables blocking of the current flow in one direction, as described above. In contrast to diodes, transistors are made from three layers, a low resistive material sandwiched between two layers of higher resistive materials or vice versa. This way the transistor has more than two levels of resistance i.e. the resistor's value is changeable based on the input signal. It can transform its resistance. In general, diodes and transistors have a great deal in common. For instance, the Junction Field Effect Transistor (JFET) resembles two diodes placed in parallel, one in forward and one reverse mode (Figure 44).

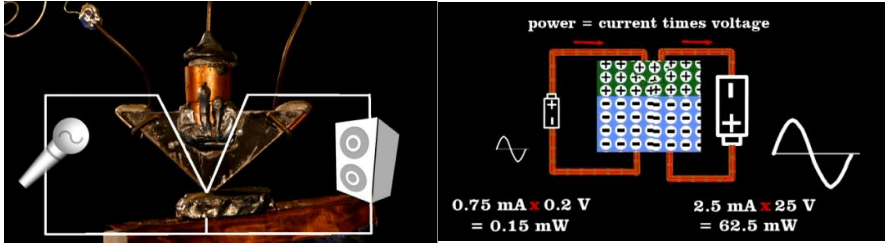


Figure 44 Contact point transistor (left) and concept of two diode place in opposite direction (right) [75]

Besides the JFET, there are many other transistor concepts, for instance FinFET (fin (thin silicon) field effect transistor) or VMOS (V-groove shaped metal oxide semi-conductor transistor). Figure 45 illustrates various transistor types. The name of each transistor either does relate to its working mechanism or the materials used in its architecture.

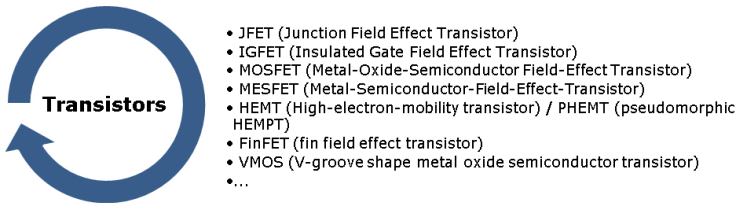


Figure 45 Variety in transistors [76]

A common feature is that the transistor architecture allows two statuses. Depending on the material combination, the transistor allows current to flow either when it is inactive or when it is active. The status can be altered by applying an electrical field which in turn changes the electrical properties of the semi-conductor within the transistor architecture from active to inactive and vice versa.

The first transistors were contact point transistors [77], rather large in size and difficult to produce on mass scale. A piece of germanium was placed on a copper plate, and a triangular plastic was pressed onto the germanium with help of a spring. Preceding this processes, both sides of the triangle were covered with a gold foil (Figure 44).

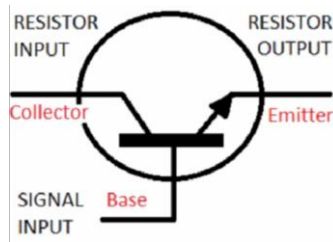


Figure 46 Electronic symbol for an npn-transistor [75]

A transistor is a three-terminal electronic device as demonstrated in Figure 46. It is possible to control the electric current or voltage between two of the terminals by applying an electric current or voltage to the third terminal. This is what allows the development of an amplifier for electrical signals, like in the crystal radio mentioned in 5.1. Also, transistors serve as electric switches. Used as a switch in logic circuits, functions can be switched on or off. Compared to a mechanical switch, transistors do not contain any moving parts and therefore are more damage resistant. The transistor is operated by an electrical current which enables a much faster switch between on/off compared to a mechanical switch.

Faster switching speed enabled the development of modern computers. Switching from off to on or vice versa matches the two binary states 0 and 1 of modern computing and therefore, is crucial for today's computers' function. Since the first transistor radio, which contained exactly four single transistors, the number of components in electronic devices and computers increased enormously. Today's computers contain several thousand, or even billions of transistors. Furthermore, those transistors are not single components anymore but densely packed in integrated circuits.

Electrical switches can be controlled by other electrical switches, consequently, when combining switches in a cascade fashion (switches that control switches that control switches, etc.) logic circuits can be build. Nowadays, it is possible to build a very compact logic circuit on a chip, which is a micro-electronic device that can be switched every one nano second or even less. Since the 1960's the number of transistors per unit area has been doubled every 1.5 years. [69]. George Moore was one of the early integrated circuit pioneers

and founders of Intel Corporation. Moore's Law, predicts this remarkable progress in circuit fabrication. Generally, the number of transistors fitted on a microprocessor is directly connected with the computing power. In 1981, the Intel 8088 microprocessor was used in the first IBM personal computer on which there were almost 100 times as many transistors per unit area as there had been on the 4004 microprocessor in 70s [78]. The development of transistors is shown in Figure 47.

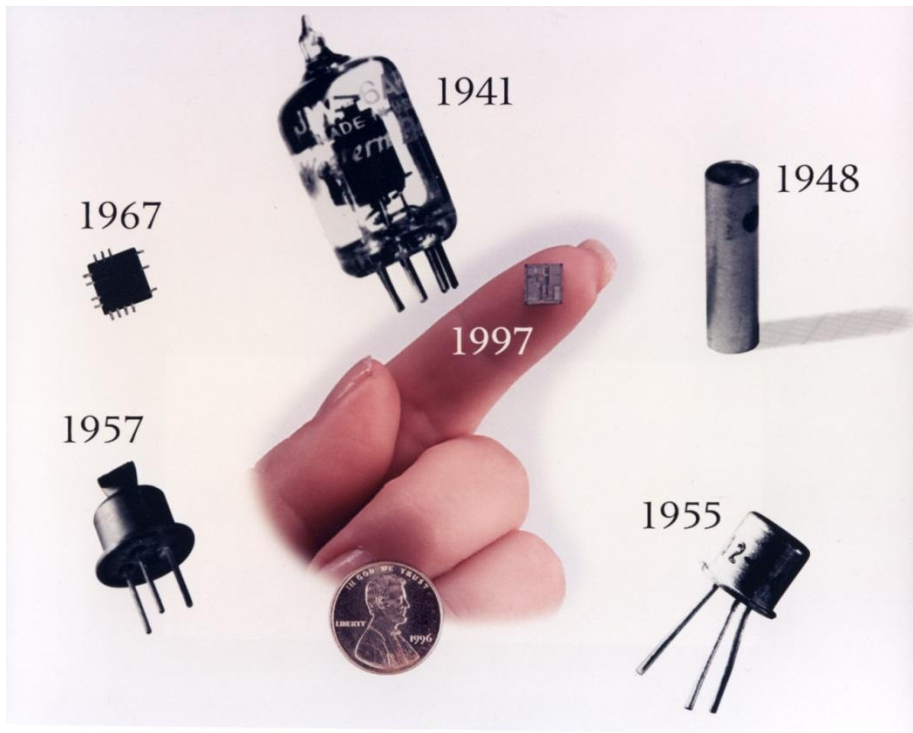


Figure 47 Vacuum tube in 1941 and development of transistor shape over time for different applications [72]

Today in electronic devices, mostly the concept of the field effect transistors (FET) is used. The MOSFET, the metal-oxide semiconductor field-effect transistor, will be used to explain the concept and its working principle of the field effect transistor.

The MOSFET is the basic element of all silicon integrated circuits [73]. The MOSFET is constructed differently than the contact-point transistor. The electrodes in the contact point transistor are called

emitter, collector and base. In the MOSFET, the electrodes are called source, drain and gate, as indicated in Figure 46. This particular architecture is made of silicon layers with two n-types and one p-type material comprising different kinds of doping. Doping is referring to impurities that have been introduced into the semi-conductor material to change or improve their electronic properties (see also chapter 6.1). Silicon has to be very pure when used (99.9999%) [79]. Doping generates two sets of semi-conductors: the negative charge conductor (n-type) and the positive charge conductor (p-type). The impurities when introduced disturb the crystal lattice of silicon. In the n-type semi-conductor the crystal structure is kept intact (four covalent bonds) and with one additional electron floating around. Within the p-type semi-conductor the impurity cannot offer sufficient electrons to close the four bonds of the lattice; therefore a hole is generated.

As for the transistor's mechanism, the current flowing from source to drain is controlled by the voltage applied at the gate. The gate is made from highly conductive material, possibly a polysilicon or metal. Silicon is less expensive than other semi-conductors and has physical properties better suited for use in current transistors, such as rather high degree of mobility or good level of processability [69]. The mobility of germanium (Ge) is twice as high as silicon but the material is sensitive to temperature and is very scarce.

To generate the function, the gate must to be insulated from the rest of the transistor e.g. with silicon-oxide (Figure 48). Many transistor architectures are symmetrical, therefore source and drain are interchangeable [80].

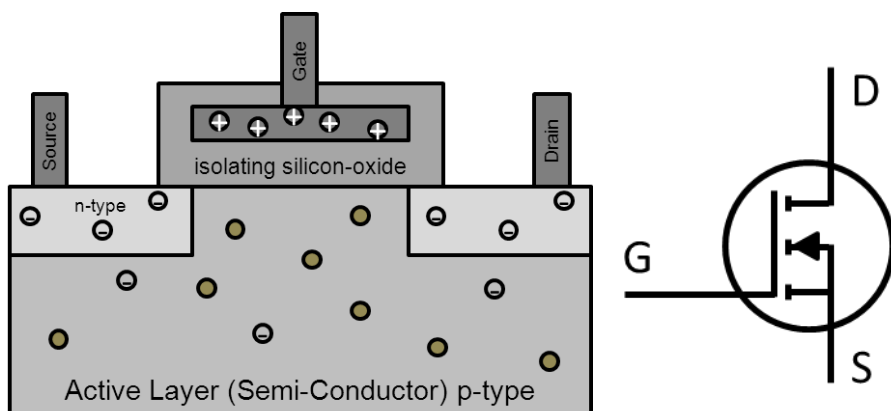


Figure 48 Top-Gate-Top-Contact architecture FET (left) and electronic symbol of a FET in integrated circuit design (right)

The active p-type semi-conductive material is located in the region between the source and the drain. This region is also called the channel. By increasing the voltage at the gate, the positive charge at the gate is growing. This charge attracts an increasing number of p-type material's electrons. In the active material, between the electrodes the electrons are accumulating and at a certain point enable flowing of electrons from source to drain.

The electrons will follow in proportion to the pull generated through the voltage applied at the gate electrode. Therefore, with the input signal to the gate one is able to increase or decrease the current from source to drain (output signal). Hence, the MOSFET is called a charge controlled device [81]. At peak voltage, the semi-conductor is in a status of full conduction, comparable to a metal.

In summary, with a small energy input at the gate side, the flow was initiated (opening) and the current got amplified with increasing voltage. In the literature, this mechanism is often compared to an ordinary faucet. Whereas the in-pipeline is the source, the faucet is the drain and the water tap is the gate which controls the water flow.

5.3. Thin film transistors

When looking at the architecture of today's field effect transistors (FET), for application in textile industry most suitable are those produced in thin film technology. The films or layers in thin film transistors are called thin because their thickness is mainly located in the nanometer range (up to some micrometers) [82]. In general, thin film deposition processes in which high resolution in the patterned film are applied are for instance, evaporation, printing or lithography [83]. Benefits deriving from using thin film technology are [84]:

- reduced production costs (material)
- smaller and more lightweight finished products
- increased flexibility

Manufacturing with thin film processes implies that different layers of thin films are successively deposited onto a substrate [85]. This construction or architecture is also called a stack. The substrate is of importance because the films are not self-supporting without the substrate. Also the substrate can have a function on its own e.g. being conductive. For the application in organic thin film transistors, substrate materials commonly used are glass or plastic. With increasing demand for flexible devices plastic substrates gain more and more importance, such as polyethylene naphthalate (PEN) [86].

There are four main architectures for building a FET. These are characterized by the location of the gate and source/drain electrodes, as shown in Figure 49.

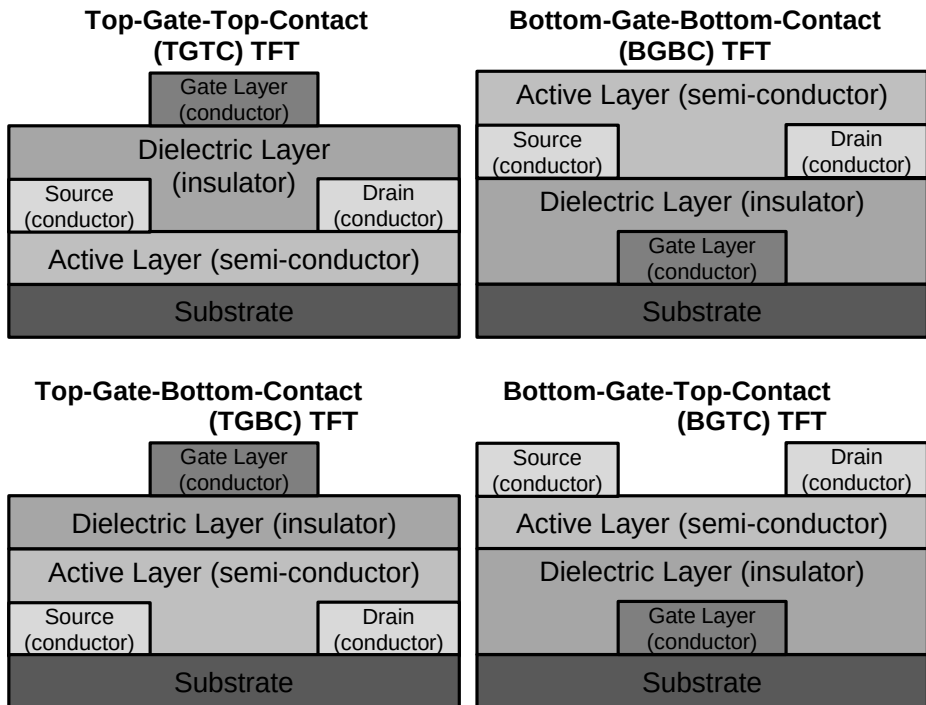


Figure 49 Variation in transistor architecture: Top-Gate-Top-Contact (TGTC) TFT (top left), Bottom-Gate-Bottom-Contact (top right), Top-Gate-Bottom-Contact (bottom left) and Bottom-Gate-Top-Contact (bottom right)

The choice which architecture is used depends on the final application and has a significant effect on handling i.e. contacting the transistor. For instance, TGBC offers a large injection-interface, but BGBC might be easier to produce since the sensitive semi-conductor is situated on the top of the device, and not like in TGBC in the bottom region. In this position, it can be easily damaged by the deposition process and involved chemicals of the subsequent layers.

The architecture has to be translated into a textile compatible outline and process technologies to apply the architecture need to be found accordingly.

5.4. Fibrous transistor

Entering the field of textronics, the process technologies for applying materials from the world of electronics onto the textile substrate have to be identified. Which technology is used depends to a large extent

on the choice made regarding the suitability to substrate and layer materials. Furthermore, it is of importance that process technologies are compatible to the processes in textile industry. Consequently, chosen process technologies should focus on low temperature application as well as the applicability for continuous processing, with high potential for up-scaling from lab batch to mass production. After due deliberation solution based processes seem to be the best choice for completing this task.

Bottom-Gate-Top-Contact (BGTC) architecture was chosen as the terminals are fairly easy to contact. As was pointed out in section 5.2, the transistor is a three-terminal device, with the electrodes: gate, source and drain. In the FET particularly, the gate electrode is insulated from the active material by the dielectric. In Figure 50, the architecture of the BGTC FET is shown.

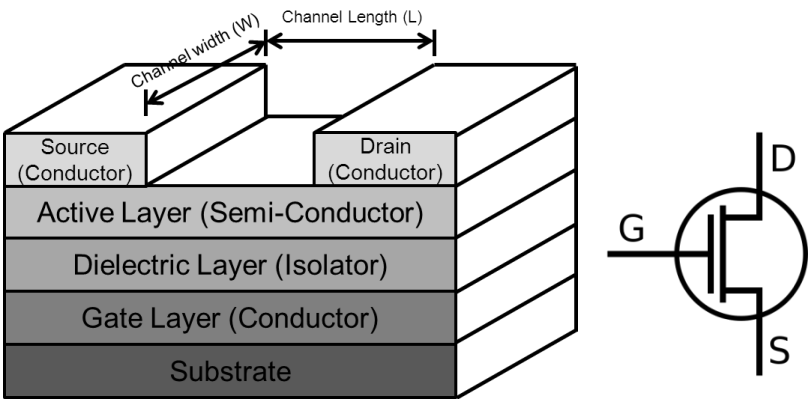


Figure 50 Architecture of a Top-Contact-Bottom-Gate Field effect transistor (left) and respective electronic symbol (right) [87]

This architecture was then translated into a textile version based on a filament with a cylindrical structure. Schematic drawings of the cross-section and of the fibre are shown in Figure 51 and Figure 52.

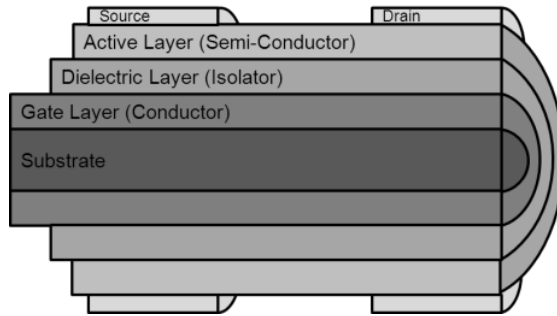


Figure 51 Cross section of OFET architecture on filament

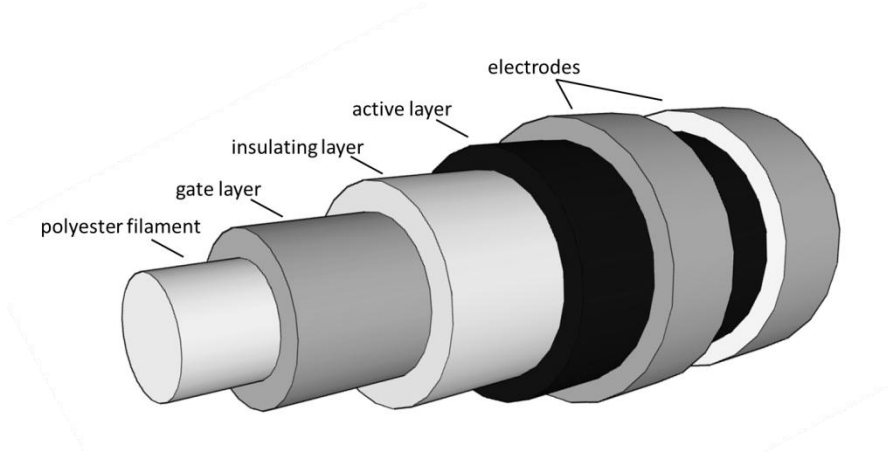


Figure 52 OFET BGTC architecture on a fibre

As is the case with flexible electronics, the properties that are inherent in the textile's nature e.g. having small dimensions or being flexible, stretchable or drapable and sometimes cylindrical, make a challenging assignment in terms of identifying the right process technologies and materials [88].

Chapter 6 describes the materials and process technologies applied in the experimental part in chapters 7 to 10.

6

Materials & methods

Chapter 6 provides an overview regarding materials and methods applied in the experiments (see chapters 7 - 10). It describes the materials used within each layer of a transistor fibre and explains their application method. Furthermore, the chapter supplies information regarding characterization methods of the various layers. It should be noted that the aim of Part 2 of this dissertation is to apply the developed conceptual framework of the fibrous organic field effect transistor (OFET), with the intention of facilitating the effectiveness of current interdisciplinary research and product development. Therefore, detailed collection of information and data seamlessly describes and illustrates the fibrous OFET production process.

6.1. Materials

The following sections outline the use of substrates and materials regarding the experimental part of this dissertation. Not all substrates or materials were used for the entire duration of the experimental work. Some were found unsuitable for further use in experiments, and therefore were excluded (see chapters 7 to 10 for a detailed criteria determining for exclusion).

A. Substrates

Thin films require a substrate to support the deposited layered architecture. In thin-film micro-electronic processing planar substrates are commonly used. To ensure the adequate translation of planar architecture onto the cylindrical substrate (see Chapter 5), experiments were initially conducted with planar substrates and followed up by experiments with cylindrical substrates. During the course of this set of experiments, four different substrate types have been investigated. Figure 53 displays the substrate types used in constructing the thin film architecture. Both, planar (2D) and cylindrical (3D) substrates were available in a rigid but also in a flexible version.

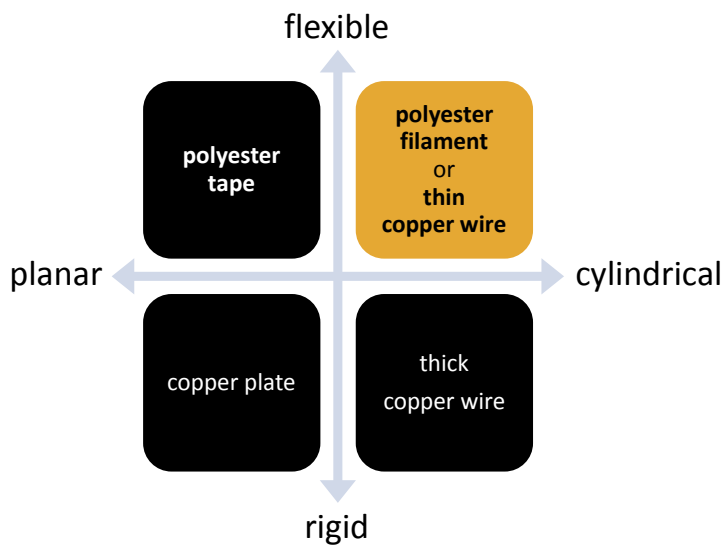


Figure 53 Variety in substrates used in experiments

i. Copper plate (planar-rigid)

A big copper plate with a thickness of approximately 1 mm was cut into smaller rectangles with the dimensions 50 mm x 25 mm, as well as, 50 mm x 5 mm.

The cutting process was completed with a mechanical shearing machine. Since the protective layer on the copper was already removed, and the cutting process did not allow gentle treatment of the substrate, the surface was somewhat scratched (Figure 54). In addition, it was not always possible to avoid deformation of the metal piece. The rectangles of 25 mm width were used in experiments related to the dielectric layer only, whereas the rectangle with a width of 5 mm was also used in semi-conductor application.

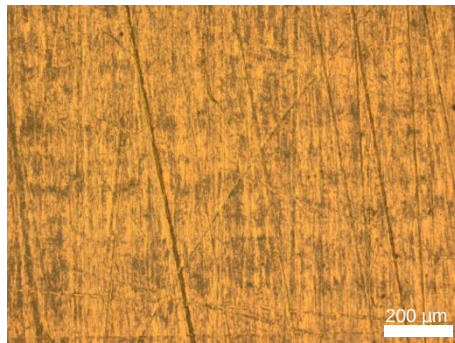


Figure 54 Copper plate surface

ii. Polyester tape (planar- flexible)

A polyester tape with a width of 1000 μm and a thickness of 40 μm was tested during the gate layer copper coating process. Regrettably, the source of the tape could not be identified.

iii. Copper wire (cylindrical-rigid)

The copper wire was purchased from Goodfellow and had a diameter of 1000 μm (99.9% pure, annealed, LS390684).

iv. Insulated copper wire (cylindrical-flexible)

The insulated copper wire was purchased from Goodfellow and had a diameter of 500 μm , the dielectric layer on the copper wire was a 25 μm thick polyimide.

v. Polyester monofilament (cylindrical-flexible)

Polyester filaments in two diameters of 800 μm (900C 4068, K335) and 888 μm diameter were purchased from Teijin.

B. Properties of the deposited layers

In addition, the electrical properties of the material deposited as thin films or layers in the organic field effect transistor (OFET) have been assessed. The final function is based on the proper combination of materials and their application i.e. suitable process techniques. The deposited layers are conductive, insulating or semi-conductive.

i. Principle of conduction

In the field of electronics, electrical conduction is one of the basic functions. Materials conduct an electrical current in many different ways. From a material perspective, good conductors are gold (Au), copper (Cu) or aluminium (Al), whereas, glass or wood are suitable insulators [89]. As the term indicates, a semi-conductor is a material that conducts electricity not fully but only to a certain degree. Its conduction value lies somewhere between a conductor and an insulator [73].

Conductivity is based on the electron flow between atoms of one or more materials. In conductive material, the atom's highest energy band is only partially filled with electrons (conduction band). This leaves *room* for the electrons to accelerate in order to gain energy. The acceleration energy is needed to transfer the electron to a higher energy level, enabling the electron to jump to a higher level (conduction band). In an insulator, the valence band is completely full occupied, hence there is no *space* for acceleration. In addition, the band gap which is the vacant space in between the valence and conduction band is very large in insulators. Because of the limited

space for accelerating the electron and the distance between the bands, the electrons will not be able to jump to the higher energy level, i.e. the conduction band.

Finally, in a semi-conductor said distance between the bands is smaller but its valence band is completely occupied. A semi-conductor often is sensitive to temperature. At room temperature, the electrons in the valence band start to vibrate and eventually some electrons escape to unoccupied positions in the conduction band.

However, at very low temperatures it reacts like an insulator since its valence band is completely occupied and does not vibrate. Therefore, free energy is unavailable. Still, this electron flow is so small that no significant current is able to pass [90]. A comparison of conductor, semi-conductor and insulator material is shown in Figure 55. The band gap is the distance between valence and conduction band. In general, semiconductors have a band gap (E_g) of between 2 eV and 5 eV, the band gap of metals is 0 eV, and insulators show a band gap of > 5 eV [90].

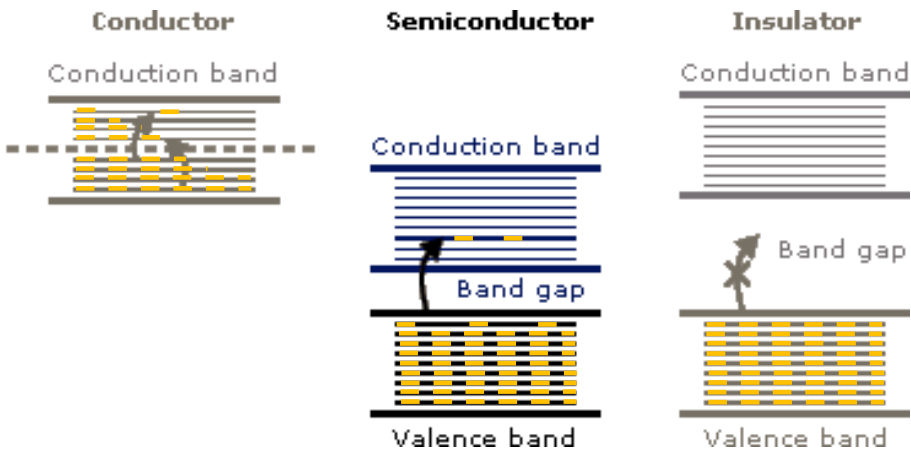


Figure 55 Scheme of transfer of electrons from valence band to conduction band in conductors (left), semi-conductors at room temperature (middle) and insulators (right) [90]

Depending on the type of semi-conductor in the active layer, the charge which flows between source and drain electrode, i.e. in the channel, is positive (dominated by electron holes) or negative

(dominated by electrons). Respectively, the semi-conductor is either of p-type or n-type material (see also chapter 5).

ii. Semi-conductor material

Both inorganic semi-conductors, (doped) silicon (Si) and germanium (Ge) have a crystalline chemical structure, termed diamond lattice. In this lattice, each atom builds a tetrahedron, i.e. it is linked with its four nearest neighbours. The atom situated in the centre combined with the four electrons form perfect covalent bonds with four neighbouring atoms. Electricity involves the flow of electrons. Metals most often have electrons that can move freely between atoms, hence, metals are good conductors. Silicon does not belong to the category of metals. In silicon, all of the outer electrons in the crystal are linked to each other in covalent bonds. Consequently, they cannot move around. Hence, pure silicon is almost insulating. Semi-conductors are available as either elements, such as silicon (Si) and germanium (Ge) or as compounds such as silicon carbide (SiC). Compound semi-conductor material enables engineering of a wide range of energy gaps and mobilities. Consequently, semi-conductors are also termed wide band gap semi-conductors according to the composition of their compound material.

Silicon often is found in combined form in nature e.g. in rocks and sand. To be able to use silicon as a semi-conductor, silicon has to be purified. It is the most frequently used in semiconducting material today [36]. Like silicon, germanium is another semi-conductor found in group 14 of the periodic table. As pointed out in chapter 5, in the 1950s germanium was preferred semi-conductor used in transistors. It is however, much scarcer than silicon and is therefore rarely used today. Lately, in addition to inorganic materials like silicon or germanium, organic semi-conductor materials are slowly becoming central to industrial production and commerce.

Organic semi-conductors do offer a set of properties that makes their combination with the textile substrate very attractive. These properties relate to:

- deposition as thin films with high flexibility

holes creates electron deficiencies, consequently the total negative charge is reduced.

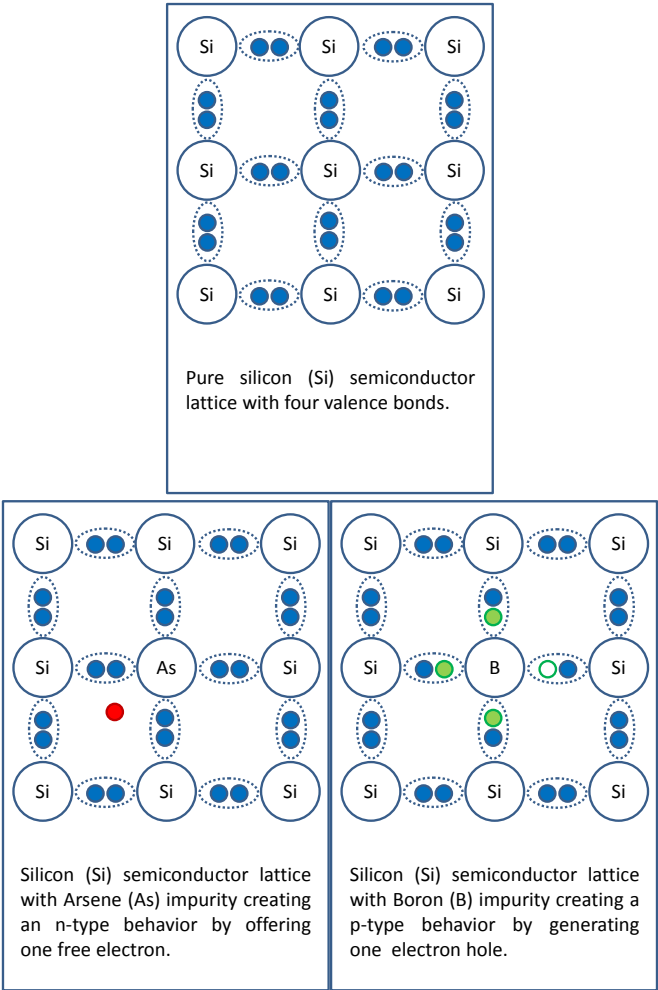


Figure 57 Examples for doping silicon (top) with n-type dopant arsene (bottom left) and p-type dopant boron (bottom right)

iv. Layers deposited

Four different layers were deposited on the fibrous substrate:

- 1) Gate electrode
- 2) Dielectric layer
- 3) Active layer
- 4) Source and drain electrodes

See sections below for additional information regarding each layer.

1) Gate electrode – conductive

Some of the substrates were already conductive i.e. the copper plate or copper wire, whereas others were insulating. The insulating substrates e.g. polyester tape and filament, received a conductive coating, representing the gate layer within the transistor architecture.

This was achieved by coating the substrate with a polypyrrole layer onto which subsequently, a copper layer was applied by electroless deposition. The gate layer was thoroughly investigated by Schwarz *et al.* (2010) [67]. This applied study focused on the characterization of the dielectric and semi-conductive layer, and top contacts. The properties of the copper layer, however, restricted it to its effect on the subsequently applied layers and the overall function of the transistor (See: subsequent chapters of this dissertation for extended discussion of effects and function). A description of the application procedure polypyrrole and copper layer can be found in Annex C (See: chapter 7 for further information regarding the process).

2) Dielectric layer - insulating

In this study, a polyimide (PI) resin, purchased from Alfa Aesar, was chosen to be applied as insulating dielectric layer onto the possibly copper-coated substrate. Figure 58 shows the chemical structure of polyimide resin.

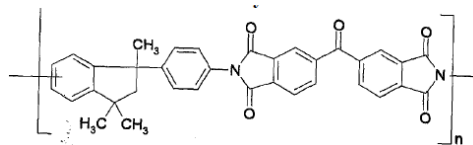


Figure 58 Chemical structure of polyimide resin [94]

The polymer can be solution processed from a limited number of solvents e.g. 1-Methyl-2-Pyrrolidone (NMP) [95-97] and dimethyl formaldehyde (DMF) [98-100]. A variety of concentrations was tested. For DMF, this relates to a range from 7.5w% to 17.5w%, within this range, the concentration was gradually increased at an interval of

2.5w%. For NMP solutions, the range was adapted related to the results from characterising the solution with DMF as a solvent.

Solutions were prepared by slow magnetic stirring for 24 h, inhibiting the trapping of air bubbles. An ultra-sonic bath was used to remove all air bubbles. This process resulted in a solution, which had honey-like viscosity and was reused for several coatings.

To improve the viscosity of the solution during its production, it was heated to 25°C which influenced the viscosity of the solution. In general, before dip-coating in the polyimide solution, the solution was heated to 15°C if stored at lower temperatures in the laboratory environment (8°C). At a later stage the solution was stored at room temperature in the clean-room where the dip-coater was situated.

Chapter 9 describes the deposition of polyimide as dielectric layer by dip-coating.

3) Active layer - semi-conductive

A 2w% solution was made from TIPS-pentacene purchased from Sigma Aldrich and from Ossila and toluene purchased from Sigma Aldrich. In order to entirely dissolve the content, the solution was made and frequently agitated at intervals of 10 min for 60 minutes. Optimally, the solution should be filtered after production. This process was completed by extracting the solution with a syringe, and subsequently filtered through a PET 45/25 filter with 25 µm pore size into the container ready for dip-coating. The solution was reused whenever possible (See chapter 10 for further information regarding the semi-conductor material 6,13-Bis(triisopropylsilylethynyl)pentacene).

4) Source and drain electrodes - conductive

Several materials have been tested for application as top contacts (source and drain electrodes). Aluminium, silver and gold were the main materials deposited.

Silver screen printing ink (Electrodag® PF-410) purchased from Acheson, and nano silver conductive jettable ink purchased from Suntronic U7790 (Solsys Jettable Silver, EMD5714, 40%) were used for drop-casting. The latter was also used for inkjet printing.

Aluminium and Silver were applied by thermal evaporation, gold by plasma sputtering.

See chapter 8 for further information regarding the depositing of the source and drain electrodes.

6.2. Production processes

The application of the polymeric and non-polymeric material as thin films or layers on a flexible, cylindrical substrate poses a number of challenges in terms of processing. This includes the entire process chain, starting from storage of the substrate to the final analysis of the deposited layer as shown in Figure 51.

In the following section, the main process techniques which were used in this study are explained (See: respective sections of chapters 7 to 10 for further information).

i. Dip-coating

Dip-coating has been chosen for depositing the dielectric and semi-conductive layer onto the filament substrate. The substrate is dip-coated in the solution at a controlled speed (withdrawal speed). When the substrate is withdrawn from the dip-coating bath, the polymer solution adheres to its surface and solidifies during subsequent drying [101]. The schematic drawing in Figure 59 shows a dip-coating device.

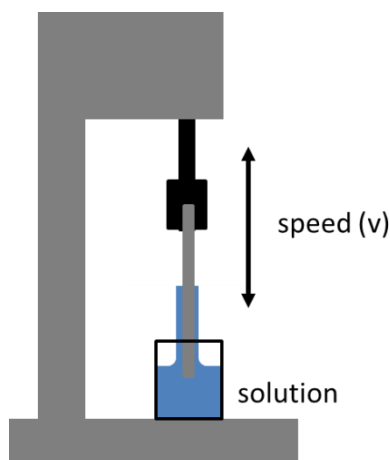


Figure 59 Discontinuous dip-coater (schematic drawing)

The dip-coating process allows up-scaling for continuous production to an industrial scale (see Figure 60). Continuous coating lines, also known as padding lines, already exist and are well established in current textile industry's production lines. The properties of the dip-coated layer in terms of thickness and quality are mainly determined by temperature, pressure, humidity and speed. Also the angle of withdrawal, pre-treatment of the substrate and the drying conditions play a significant role [102, 103].

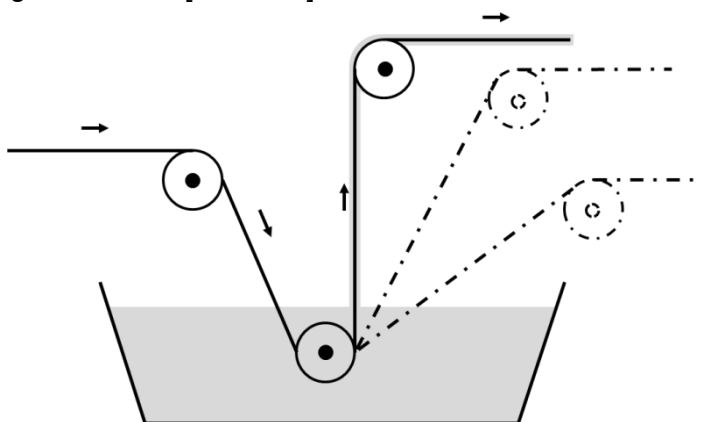


Figure 60 Continuous dip-coating process padding indicating the variation in withdrawal angles

In this dissertation, pre-treatment, drying conditions and dip-coating parameter speed were investigated. Withdrawal was undertaken at 90° to achieve an even layer surrounding the substrate. To avoid

layer heterogeneity and guarantee a constant thickness of the coated layer, a dip-coater located on a vibration free table in a clean-room was used. Dip-coating is commonly used for depositing thin films on filaments or substrates with a three dimensional shape.

The filaments were dip-coated in the solutions at a withdrawal speed between 1 mm/min and 150 mm/min. The speed during substrate immersion into and withdrawal from the solution was kept constant.

In the application of the dielectric and semi-conductive layer, other thin film deposition techniques like spin coating or vapour deposition were excluded from investigation. Current research focuses on textile applicable processes, which also means processes that can be applied on a cylindrical shaped substrate [33]. It is not optimal to use high temperature or vacuum processing techniques in textile production processes, therefore the entire circumference of the substrate should be covered. Moreover, the processes are difficult to up-scale because they are discontinuous and often conducted in a vacuum chamber.

ii. Evaporation

The top contacts were applied by thermally evaporating silver (Ag) or aluminium (Al) under vacuum. Here, the material in form of pellets is placed into a ceramic evaporator “boat” and is heated-up. The molten metal evaporates into a cloud above the boat and settles onto to the substrate which is placed above the evaporator. A shadow mask is used the process of evaporating a patterned layer. The contacts were evaporated at an evaporation rate of 10 Å/sec resulting in an approximate thickness of 100 nm.

Shadow masking using tape was employed to make contacts with a length of 20 mm. During the evaporation process the back of the fibres is not completely coated, unlike the top and the sides of the fibre. This process will yield a surface area of approximately 74 mm², assuming that 240° of the fibre’s circumference will be coated for fibres with an 888 µm diameter.

iii. Sputter deposition

Thin film deposition can also be achieved by sputter deposition which is a type of physical vapour deposition (PVD). A material, the target, is eroded and the atoms are deposited onto the substrate in the vacuum chamber. A gold (Au) layer with a thickness of 30 nm was deposited within approximately 90 seconds (Figure 61).

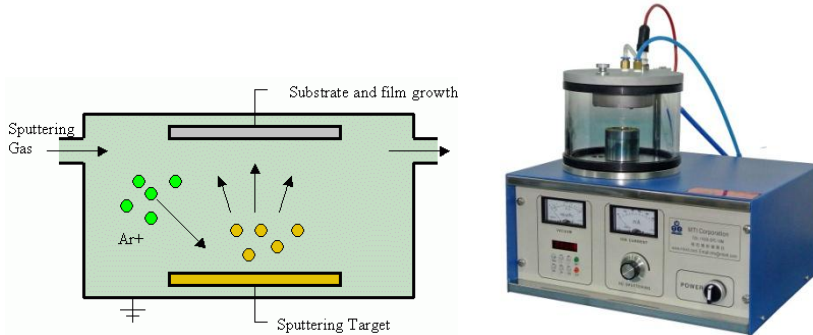


Figure 61 Sputter deposition scheme (left) [104] and example for Compact Magnetron Plasma Sputtering Coater (right) [105]

iv. Ink-jet printing

Thin film deposition was completed with a piezoelectric Drop-on-Demand inkjet printer (MicroFab Technologies, MJ-ABP-01). The system comprises a computer controlled XY positioning system. Nano silver conductive jettable ink was printed with a single nozzle printing head with a 30 μm orifice diameter at room temperature. Figure 62 shows a schematic drawing and a picture of the printer.

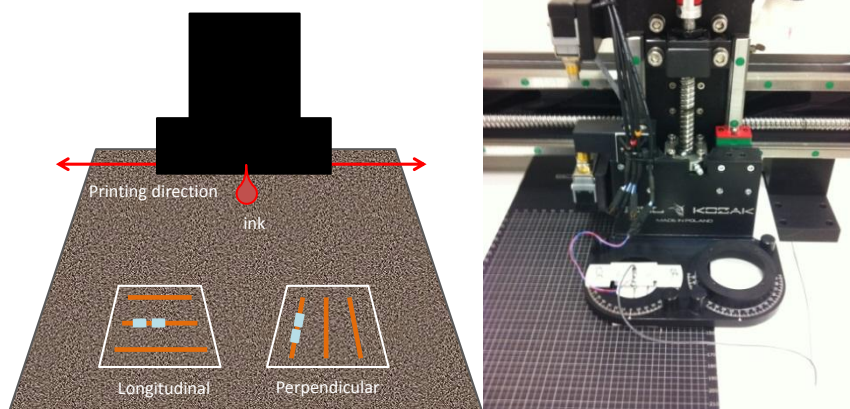


Figure 62 Schematic drawing of the printer (left) and a picture of ink-jet printer Microfab (right)

A multi-nozzle system, Dimatix materials (Fujifilm Dimatix Inc. DMP-2800), was tested with cartridges providing orifice diameters of 9 and 23 μm (~ 1 and 10 picoliter droplets). Figure 63 shows a schematic drawing and a picture of the printer Dimatix.

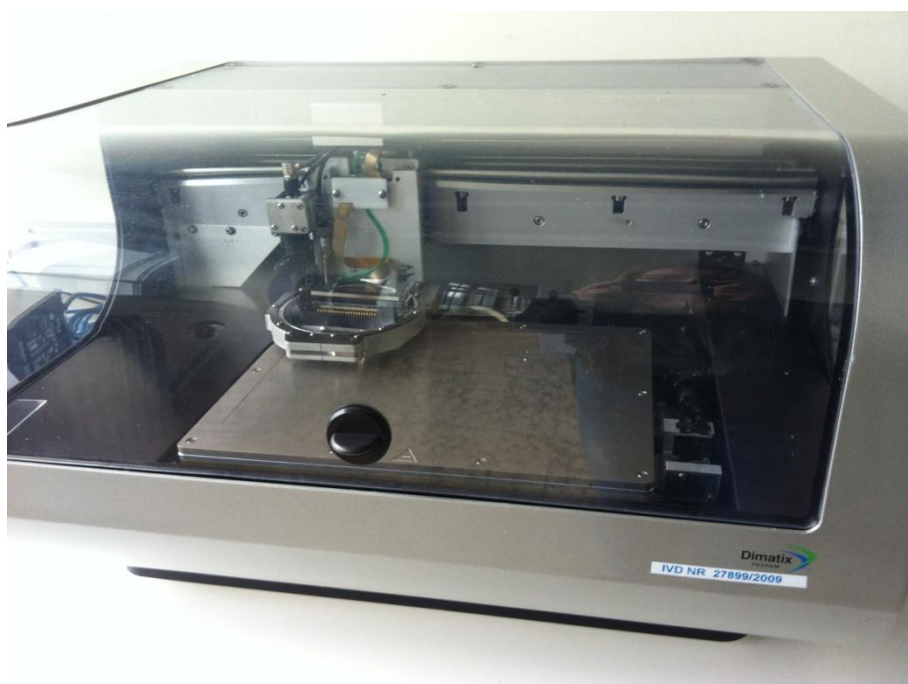
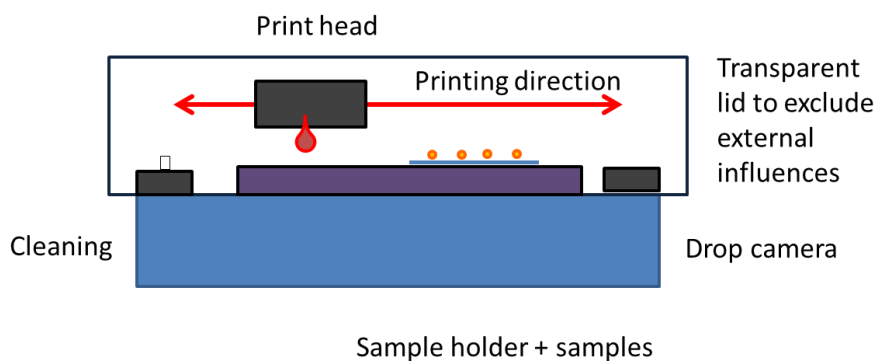


Figure 63 Schematic drawing (top) and picture of multi-nozzle ink-jet printer Dimatix (bottom)

6.3. Methods of characterization

Following depositing of layers, each layer was analysed with respect to surface and bulk morphology as well as to their electrical properties. This section describes the methods for characterising the different layers. It is as well to point out, that not all described methods were used for each layer but were applied as appropriate.

The substrate type played an important role in defining if the characterization technique was applicable. The remainder of this dissertation will furnish the rational for choosing specific methods of characterising layers.

A. Morphological characterization

The morphology of the coated layer is influenced by end effects at the top and bottom of the sample. To indicate position of the image taken, a ruler was positioned next to the filament on the stage of the microscope. Only the middle section of the image is suitable for analysis, as this section represents conditions which are similar to those achieved by continuous dip-coating and therefore is comparable across different layers and samples. In general microscopic pictures were taken in various locations of the samples, as described in section 6.2 (p.149). Using this method the shape of the crystals were observed across the entire length that was dip-coated. Furthermore, it should be born in mind that all the dip-coating as well as the morphological analysis was conducted in the dark with only a computer screen as light source.

The deposited layers were evaluated in respect to their morphological properties. The layer should be uniform, of certain thickness and eventually have a low roughness and have high crystallinity depending on the layer in question.

a) Surface Morphology

Samples were visually examined with an optical microscope (Olympus), scanning electron microscope (SEM, Fei Quanta 200F,

high vacuum mode, under high voltage of 20 kV) and, a Focused Ion Beam (FIB) analyser.

i) Optical microscopy

As for the dielectric layer, pictures were taken in the middle of the sample avoiding the influence of edge effects. For the semi-conductive layer, the use of normal microscopy was not suitable. The layer had to be investigated with help of a polarizer.

ii) Optical microscopy with polarizer

Best results were generated at a magnification of 25x. At lower magnification, the semi-conductive material could not be seen. At higher magnification the area to be analysed was too limited for interpretation due to the surface curvature on the filament. The samples placed on the graduated circular stage could be rotated through 360°. The samples were viewed in various rotation angles for example 45°, 90° and 180°. Pictures of up to 5 different locations on the sample were taken: at the lower end of the sample (0 mm), two in the middle (5 mm and 10 mm) and two at the top of the coating (15 mm and 20 mm). A scheme for defining locations of microscopy pictures is shown in Figure 64.

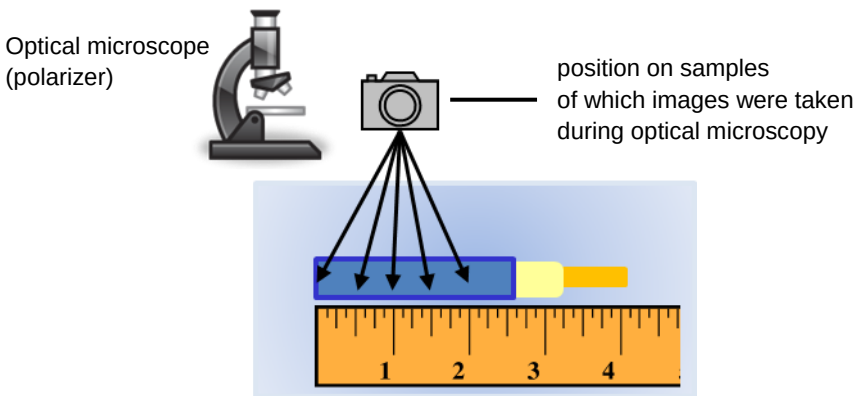


Figure 64 Scheme for defining locations of microscopy pictures. Images have been taken at a distance of 0 mm, 5 mm, 10 mm, 15 mm, and 20 mm from the filaments lower end.

iii) Roughness

The dielectric layer was analysed using Atomic Force Microscopy (AFM) in semi-contacted tapping mode measuring the value of roughness of the layer. AFM plots showed the number of events of an encountered height deviation in function of the value of that height deviation in nm. Roughness values were calculated using WSXM 4.0 software. The root mean square of this value was used to compare the value of relative roughness.

During collaboration with the SURF group at VUB (Vrije Universiteit Brussel), in particular the semi-conductive layer was analysed by measuring with an AFM in tapping mode with an ACTA tip from Appnano. Most scans were conducted on an area of $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ (256×256 pixels). Scans were taken at locations in the middle of the coating.

All images were flattened by a whole flattening procedures to remove waviness, with a maximum exponent of the polynomial of 3. Both topographical and phase images were generated. The value of roughness (R_q) was calculated after flattening using XEI, version 1.8.

b) Bulk morphology

Not only the surface properties but also the bulk morphology was investigated.

i) Thickness

For measuring the thickness of the PI layer, the coated samples were embedded in historesin (Leica). This way, compression of the layer is avoided when cutting it for cross-sectional inspection. Optical microscopy in combination with Cell[^]d software was used for defining the layer thickness on the filament's cross section.

A solution of 50 ml polymer solution containing (2-hydroxyethyl)-methacrylate and 0.5 g dibenzolperoxide was made. Following the hardener dimethylsulfoxide was added in a 12:1 ratio. After the substrates are immersed into the solution it takes about four hours for the solution to harden. A cross section of the coated fibres in the

hardened resin produced to measure the thickness of the various layers.

The thickness of the polyimide layer on a flat copper plate was evaluated by scratching the dielectric layer using another copper plate and measuring the height difference with a contact probe. Measurements were performed using the Talystep (Taylor-Hobson) profilometer. This technique measures the approximate thickness of the layer as the edges of the scratch can be deformed and this tends to impair the measurement of thickness, making it unreliable.

c) Other characterization techniques

i) Surface tension

The measurements were conducted on a DSA-30 Krüss setup, surface tension and contact angle were measured. For surface tension measurements (pendent drop), needles with a diameter of 1.259 mm diameter were used, for contact angle measurements needles with a diameter of 0.506 mm. Dosing was set to at 4 μl at a speed of 25 $\mu\text{l}/\text{min}$. The setup is shown in Figure 66.

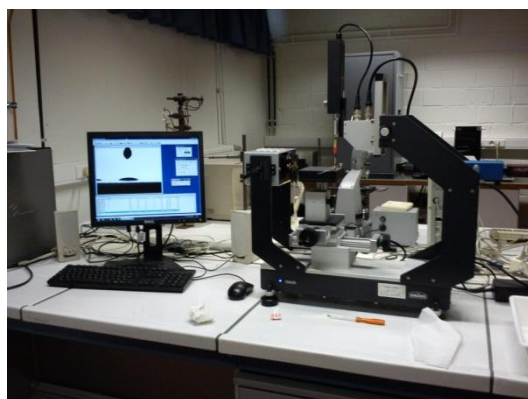


Figure 65 DSA-30 Krüss setup for measuring contact angle and surface tension

ii) UV/VIS in solution

The UV/VIS absorbance spectra of solutions was measured on a SHIMADZU (UV1800), the measuring glass cuvette was filled with a

diluted of TIPS-pentacene solution (3 ml toluene on 0.1 ml 2w%TIPS-pentacene toluene solution) and scanned in the range of 190 to 1100 nm. The absorbance of UV/visible light was detected.

iii) UV/VIS on film

The UV/VIS spectroscopy of films was completed on a Perkin Elmer LAMBDA 950 UV/Vis/NIR Spectrophotometer. The full range of visible light reflection from 250 nm to 750 nm was scanned resulting in % reflectance. Two angles were used 8° and 45°.

iv) X-Ray Diffraction (XRD)

Crystallinity of the layer was analysed by X-Ray Diffraction (XRD). A variety of positions of the sample on the sample platform have been tested. This included arranging the samples in electron beam direction and positioned in 90° to it. Furthermore, the height of the platform was adjusted according to the substrate's dimensions. Mostly it was measured from $2\theta \div 3-22$. Slit sizes were optimized to 1.5 and 2 at the emitter and 2 and 1 at the collector. The power was set to 45/40. See: chapter 10 for further information regarding the advantages and disadvantages of using this technique related to the crystallisation of the semi-conductor layer.

v) Thermographic camera

To evaluate the temperature of the sample during the dip-coating process, a thermographic camera (FLIR T420, 60Hz) was used. Both, a temperature measurement as well as an image depicting those measurements were obtained. The change in temperature on the substrate's surface before and during layer deposition was obtained.

B. Electrical characterization

Micro-voids in the layer can be detected by morphological characterization. They are likely to act as traps for the charge carriers and will have a negative effect on field effect mobility and the overall transistor performance. The quality of the dielectric and semi-conductive layer was evaluated by determining its insulating

properties by employing resistivity and leak current measurements. All measurements on the semi-conductive layer have been conducted in dark, ambient conditions.

i) Resistance

For evaluating the electrical properties of the layer, the four point probe resistivity measurement was applied. The four probes were applied on the filament in a linear fashion. The current was supplied on the outer probes, the voltage was measured between the inner probes. Across the inner probes a voltage drop was observed. Only the resistance of the layer itself was measured during this experiment,. Based on the measurements, the resistance or conductance was calculated by

$$R = \frac{\text{Voltage}}{\text{Current}} = \frac{U}{I} \quad (1)$$

An Ampere meter (Fluke 75 Series II multimeter) with a resolution of 0.01 A, a DC power supply (Tti PL601) and a voltmeter (Digi tool IEC 1010 Digi 16) with a resolution of 0.1 mV were used for measurement. Flat alligator clamps (RS Components) were used as probes which were connected to a holder at a predetermined distance ensuring constant distance during the resistance measurement. The distance between the outer probes was 35 mm. The two inner probes were placed at a distance of 25 mm. This custom made setup allowed reproducible resistance measurements (Figure 66).

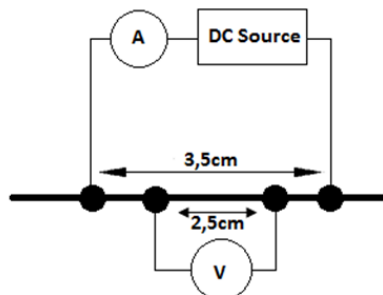


Figure 66 Image of a set up with four flat alligator clamps to make contact (left) and schematic representation (right)

ii) Leak current

The insulating properties were tested on three levels with increasing accuracy, up to pA with regards to the leak current of the deposited layer. The leak current indicates how much current is leaking through the dielectric material at increasing voltage.

1) Leak Current on dielectric layer and with 200 MΩ as upper limit

As to leak current measurements on the dielectric layer, two contacts were used on predefined locations on the sample. One alligator clamp was placed on the conductive copper layer of the samples at 10 mm from the point where the insulating coating starts. The other clamp was positioned at a distance of 20 mm, exactly 10 mm from the other side on the insulating layer, as indicated in Figure 67.

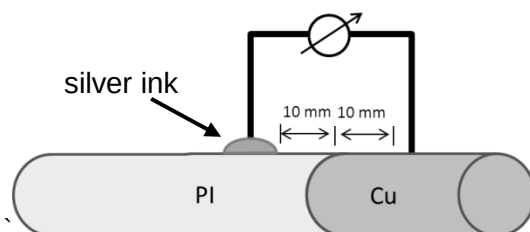


Figure 67 Representation of position of silver ink contact points for determination of leak current through dielectric layer scheme

Silver based conductive adhesive Shieldokit 3980, from the company Holland Shielding Systems, was applied on the samples to generate a good contact between clamp and polyimide layer, ensuring that the insulating properties arose from the dielectric layer and not from a bad contact. The threshold value indicating good quality for the insulating properties of the dielectric layer was a resistance of 200 MΩ [67].

2) Leak Current on dielectric layer and range up to pA

Those samples that showed good insulating properties were selected for further investigation of their insulating properties. For subsequent

measurements, a gold contact was sputtered onto the dielectric layer using vacuum gold deposition. The gold electrodes had a surface area which was represented by the source and drain contacts in the OFET architecture.

The gold electrodes not only make a much closer contact to the interface, but also extend over a larger surface area compared to the alligator clamps. The measurement was now achieved by measuring the leak current through the dielectric layer at an increasing voltage between the gate copper contact and the gold deposited contact.

This initially achieved an accuracy of 10^{-5} A and 10^{-4} V. The maximum generated voltage was 60 V. Samples should insulate over the entire range. Final tests were conducted at increased sensitivity up to the level of pA. Voltage was increased from 0 to 10 V in steps of 1 V.

3) Leak current on semi-conductive layer and range up to pA

As for the TIPS-pentacene layer, leak current measurement was conducted on a current measuring system available at the Department of Electronics & Information Systems (ELIS). Leak current in the range of μ A to pA were observed. The setup is shown in Figure 70. The measurement was conducted by applying a voltage at the gate layer (V_G) and measuring the current at the top-contact (I_{GS}). The measurement at different voltage levels was automated and was applied in the range of -5 V to +5 V. Furthermore, the measuring time was extended to gain results for (I_{DS}) which were stabilized over time. Only the last 20 seconds of each current measurement were used to calculate the mean which then was brought in relation to the voltage applied for generating an I/V curve. A scheme of the measuring setup depicted as a scheme is shown in Figure 68.

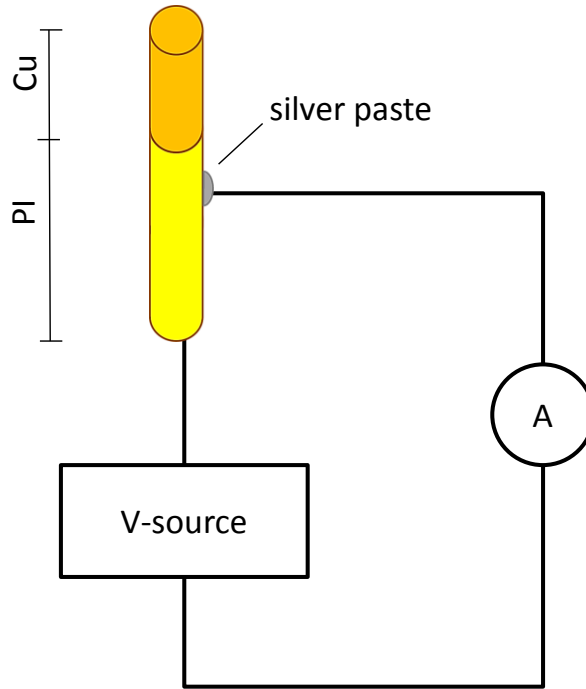


Figure 68 Measuring leak current scheme with contacts on fibre

iii) Measurement of transistor function

Finally, to test the entire construction of the transistor, the current measuring setup was modified by adding an additional power source generating voltage at the gate (V_{GS}) electrodes, where the current flowing from source to drain was measured (I_{DS}). A scheme of the setup is shown in Figure 69. The modified setup, as well as the contacts applied on the sample itself, is shown in Figure 70 and Figure 71. V_{GS} was swept from -60 V to +60 V in steps of 1 V, whereas V_{DS} was set to a range of -10 V to 10 V in steps of 1 V. The current (I_{DS}) was measured over a time of 50 seconds per voltage step.

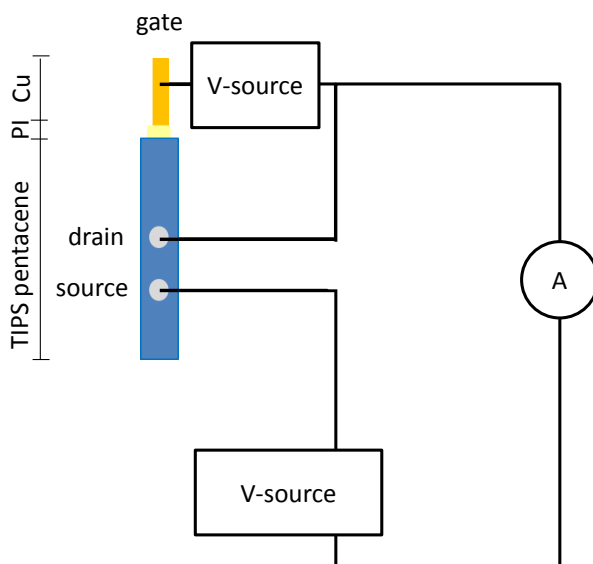


Figure 69 Measuring transistor function scheme with contacts on fibre

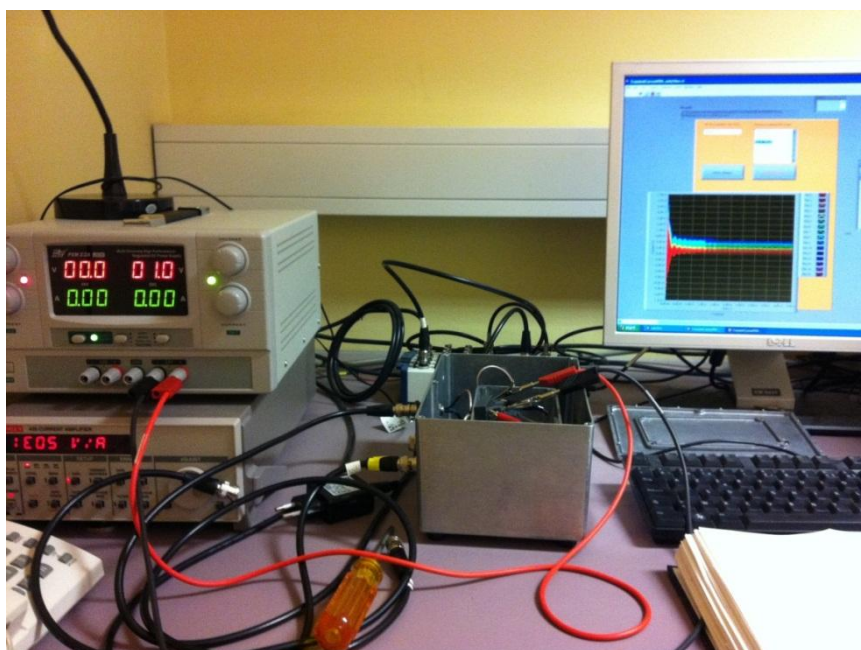


Figure 70 Transistor measuring set up including external power source for applying a voltage at the gate electrode

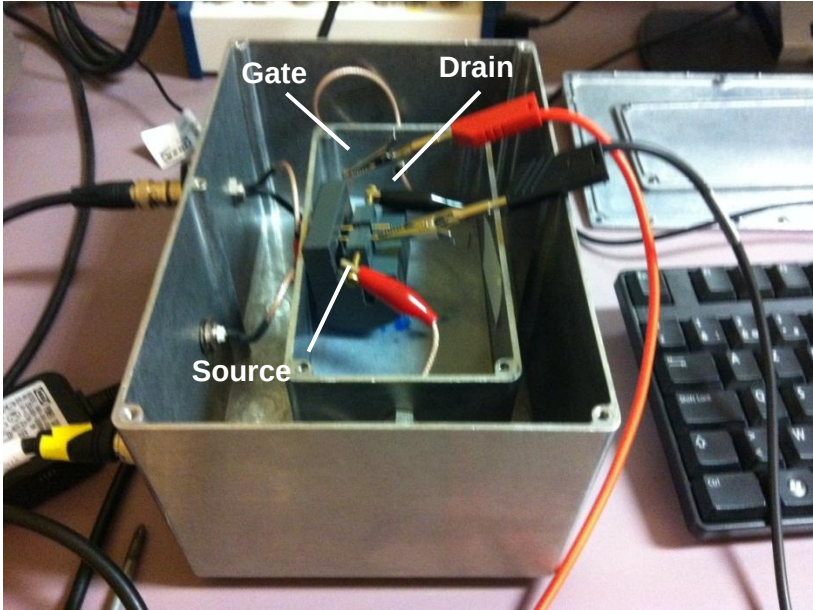


Figure 71 Contacts on sample positioned in probe station during transistor measurement

7

Gate electrode

Chapter 7 outlines the details regarding the deposition process, although the gate layer is not the main target of experimental work. The information will be helpful in illustrating the entire production process of a fibrous organic field effect transistor. The gate layer plays a crucial part in the process. This chapter describes a number of difficulties which were encountered during application which also affect the entire production process.

7.1. Storage

The 800 μm polyester filament substrate was stored on a very large reel. Unwinding the filament, left it with a deformation, comparable to bending. Since the reel was relatively big the bending of the filament was still acceptable when only short pieces of about 6 cm length were used (see Figure 72).



Figure 72 Polyester filament on reel (left) and after removal of the same (right)

When working with shorter pieces of approximately 6 cm, the bending of the filament is relatively unproblematic. However, when longer pieces were used during application of the gate layer the experimental set-up had to be changed accordingly. During polypyrrole coating and subsequent copper coating, it is of crucial importance that the substrates in the recipient do not cover each other to ensure an even coating on the substrate. The process was completed at lab scale in a variety of beakers and test tubes in which different types of baths are used. To avoid extensive waste of chemicals, very tall and thin recipients are required. For industrial application, the substrate needs to be stored on even larger reels, in a completely different manner or straightened before use, see also paragraph 8.3.

7.2. Time

The time for producing the gate layer is rather excessive and should be reduced in future experimental work (See: Annex C for detailed

description). To give the reader some idea regarding time scales, a short summary is given in Table 5.

Table 5 Steps and time scales of the application process of the gate layer

Step	Time
Cleaning and preparation of the substrate	60 min
Pyrrole coating bath I	60 min
Pyrrole coating bath II	180 min
Cleaning and drying of substrate	60 min
Drying in oven at 45°C	24 h
Palladium bath I	30 min
Copper coating sequences of bathes II	30 min
After-treatment	30 min
Drying 60°C	24 h
TOTAL	54.5 h = 2 days 6.5 h

As can be seen from the table above, the process itself is not time consuming, but the drying times between stages were. This is also an issue in drying of the dielectric layer as shown in chapter 9. It takes about two days in total to produce the gate layer on a polyester filament. It should be pointed out here, that due to the sensitivity of the intermediate pyrrole layer, the substrate cannot be stored. The copper layer must be applied immediately after the pyrrole layer has been dried.

7.3. Degradation of chemicals

The choice of chemicals determines how successful the quality of the coating can be repeatedly achieved. Pyrrole is highly sensitive to temperature, light and humidity. It is therefore prone to immediate degrading. As the producer suggests, it needs to be kept in the fridge at an approximate temperature of 5°C. However, the datasheet omits pyrrole's sensitivity to light and/or humidity. It is imperative to ensure that electricity shortages do not occur interrupting the cooling process in the fridge. Due to construction works in the building, it was not always guaranteed, that no electrical shortage occurred during the time the experiments were conducted. In addition, when the recipient in which the chemical was stored has been opened, care must be

taken to avoid exposure. The flask must be closed immediately after the chemical has been removed. Once the chemical starts degrading the respective layer will be defective. During the application of the coating the deterioration did not immediately manifest itself, but became evident following the application of the copper layer. If the polypyrrole layer becomes defective, the material cannot be used. Experience showed that pyrrole, once opened, must only be used for a maximum of six months. The longer the chemical was stored and the more frequent the container was opened, the more the pyrrole degraded. This caused an increased number of defects in the pyrrole layer which then also affected the final copper layer. This meant delaminating of the copper coating and therefore increasing layer roughness leading to distortion in the crystallisation process in the TIPS-pentacene layer, as well as, an increase in risk for short circuits in electrical characterization.

7.4. Polyester tape

Following the first cleaning stage, which was conducted in a diluted sodiumhydroxide (NaOH) bath at 90°, the flat polyester tape showed a decrease in strength. The tape was wrapped around a metal frame (Figure 75) for the cleaning step and subsequent baths to avoid being flattened out at the bottom of beaker,. Unfortunately, the polyester tape tore apart once and left the cleaning bath. The tearing might have been caused by its thickness of only 40 µm. In addition, the finished coating on this flat tape was incomplete and showed defects. Due to the deficiencies of the tape and its sensitivity, it was decided to eliminate this particular substrate from further experiments.

7.5. Polypyrrole bath excess material

When extracting the substrate from the second polypyrrole bath, a film had formed on the surface of the liquid (Figure 73) as well as a sediment on the bottom of the beaker. To ensure a defect-free coating, this excess material must not stick to the substrate. It is impossible to extract the substrates from this dark green-black solution because the samples have to be handled with care and are invisible when submerged in the solution. Hence, the solution had to be removed beforehand. Doing so, the excess material was prone to

stick to the surface of the substrate, which as pointed out above, should be avoided, as the material dried fast. Removal of dried material was difficult and caused damages to the polypyrrole layer. Therefore, distilled water must be added into the same beaker still containing the substrates, immediately following the removal of the solution from the beaker, this way the excess material cannot dry. Diluting left-over excess material made it possible to actually see and extract the substrates. Following the polypyrrole coating, the substrates must be cleaned with distilled water before being dried with a hairdryer.

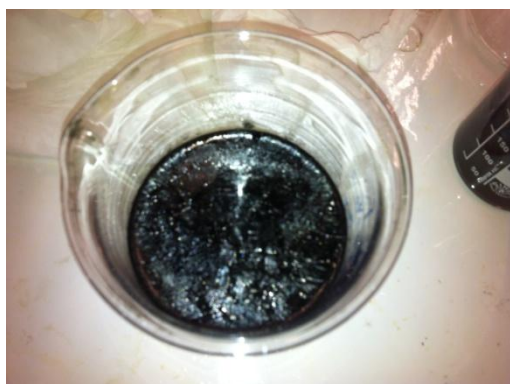


Figure 73 Film on pyrrole coating second bath

7.6. Substrate holder for coating procedure

Substrates that touch or even lay on top each other during coating can cause unevenness in the coating itself and consequently in subsequently applied layers. A technique or setup for up-scaling the copper coating process is not been developed as yet. It therefore seemed to be worthwhile to develop other methods to treat more samples simultaneously, and produce even coatings as well several options for separating the substrates during the coating procedure by using a variety of sample holders were assessed.

i) Original setup for polypyrrole/copper coating

Initially the setup was a 200 - 500 ml beaker for the polypyrrole coating and a combination of beakers and test tubes for the copper coating. Figure 74 shows the position of the filament in the beaker.

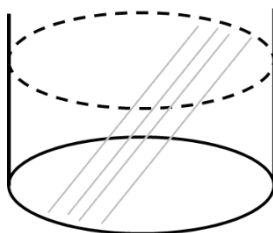


Figure 74 Scheme of position of polyester filaments in a beaker during coating process

About ten single samples with a length of 6 cm each were coated at the same time. Unfortunately, the depicted orderly separated arrangement of filaments inside the beaker could not be achieved, considering the low sample size of filaments. Furthermore, when another solution was added to the first bath, it created turbulence and the orderly arrangement was destroyed. The following sample holders have been made and tested.

ii) Metal frame construction for polypyrrole/copper coating

A metal frame following the idea of a weaving frame was made (Figure 75). As mentioned above, the flat band polyester when placed on it broke right after the cleaning stage at 80°C. The tension which exerted on the substrate during the process of winding it onto the substrate added too much stress onto the sample when it was cleaned at 80°C. It proved to be impossible to wind the thicker filaments, on the frame without somewhat stretching the filaments. The idea of using the metal frame was, therefore, discarded.



Figure 75 Metal frame holding the polyester tape during coating

- iii) Plastic holder made from a pipette tip for polypyrrole/copper coating

Even though this material should be inert to the chemicals used, the presence of the holder influenced the coatings negatively. A schematic drawing of the holder is shown in Figure 76, whereas its realization is shown in Figure 77 (right).

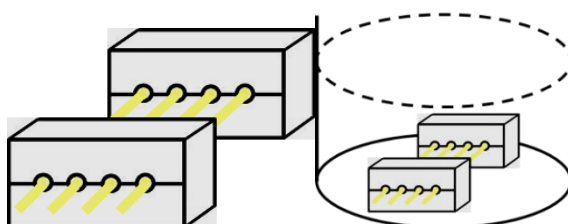


Figure 76 Concept for making plastic sample holder

- iv) PVC sample holder for polypyrrole/copper coating

This holder seemed to show great promise as it ensured stability of the filaments within the beaker despite the generation of turbulence. Extraction of the holder was awkward and the process could have been improved.

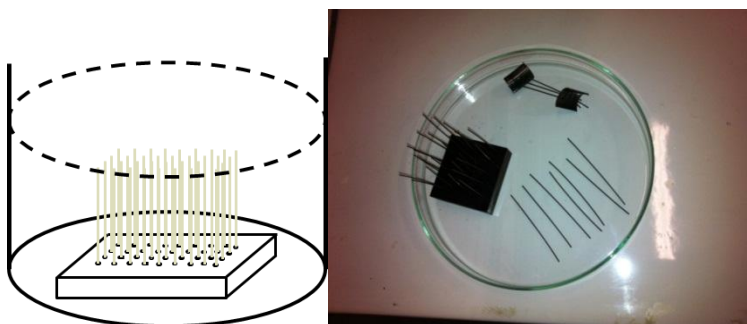


Figure 77 Schematic drawing of PVC sample holder in beaker (left) and variety in sample holder after polypyrrole coating (right)

Even if improvements were made to handling of the substrate and a large number of substrates could have been produced simultaneously, the PVC holder, unfortunately, influenced the coating procedure. Using the copper coating bath generated a great deal of bubbles. The copper coating was highly damaged and could not be used for further experiments.

By the way, the sample holders as shown in Figure 77, were not changed in between the polypyrrole coating and the copper coating. They therefore got partly coated as well as the holder got entirely coated, it might therefore, have affected the quality of the coating on the substrates themselves.

To sum up, none of the holders used the above s resulted in superior coating. As we have seen, some holders had a negative effect on the coating. As pointed out in iv), in order to produce an increased number of coated filaments with a length of 6 cm on a lab scale, the only feasible option is to use the holder concept or test inert materials like Teflon. Section 7.7 of this chapter discusses the use of Teflon during storage of the samples. Up-scaling of the copper coating has been investigated by [66] but did not lead to any solution in the process.

7.7. Storage of copper coated samples

When the copper coated samples are stored in an oven, other chemicals must be kept out of the oven. The coating is prone to

oxidation when not kept in a closed recipient. Although this oxidation can be removed with citric acid as described in section regarding the coating procedure (see Annex C.2.), also it is not the only problem, other chemicals can also have an effect on the layer.

A new sample holder for storing the copper samples before applying the polyimide layer has been made and tested. The copper-coated samples turned blue in colour after using the new holder. The discolouration of the samples was caused by the type of material the sample holder was made of. Normally Teflon is said to be inert and is used in many other experimental setups. In this instance though, the holder was made from of two kinds of Teflon (purchased at different points in time), one of them apparently was of inferior quality material. To verify the hypothesis, both materials were heated to about 90°C together with a copper plate, a glass beaker was place above to detect fogging and change in colour of the copper plate. In the production of Teflon, fluorine is used (poly(tetrafluoroethylene), $(C_2F_4)_n$). This fluorine can evaporate when still inside the Teflon. Because Fluorine is highly reactive it can only be stored or used in containers made from certain alloys of copper and nickel. It still reacts with these alloys, and forms a layer of a fluoride on the surface which protects the metal from further reaction [106]. Fluorine reacts with the copper to oxidation status +2 (reduction of electrons) it shows a colour change of copper from copper-orange to blue. This reaction is irreversible and the samples could not be recovered for further experiments.

8

Source and drain electrodes

Chapter 8 describes various techniques for applying source and gate electrodes. This layer is applied last to the filament in the Top-Contact-Bottom-Gate field effect transistor architecture. This layer is also of vital importance for the characterization of the layers previously deposited.

In the top-contact-bottom-gate configuration, source and drain electrodes are deposited as a final layer. The organic semi-conductor, where the top-contacts have to be deposited, is very sensitive to all kinds of influences for instance light or humidity. Therefore, only non-contact processes are considered for depositing the conductive electrode material. In addition, all layers which were deposited previously are thin films and hence very vulnerable to mechanical impact. Mechanical impact and accompanied damage of the layers can be caused when deposition techniques are used which are in direct contact to the substrate's surface e.g. roll-to-roll or screen printing. In this chapter, drop-casting, evaporation and ink-jet printing are investigated to determine whether or not they suitable methods of application.

8.1. Evaluation criteria source and drain layer

The application of the material required a high work function to generate a good charge injection when being used in combination with a p-type semi-conductor. The lower the work function of the material, the higher the resistance towards charge injection at a minimal contact resistance at the interface between electrode material and semi-conductor. Studies investigating the performance of microelectronic devices in relation to different materials applied for the top-contacts have been conducted [107].

When using ink-jet printing as a deposition technique, the ink must have a homogeneous distribution of its particles to achieve compatibility with the print head and it also must be highly conductive. Good candidates for this are gold (Au) nano-particles. Alternatively, silver (Ag) is a good option at lower costs as compared to gold. Silver has a work function of 4.3 eV, in comparison with Au which has a work function of 5.1 eV [107]. Ag as material is more conductive but has a lower work function leading to higher contact resistance on the interface semi-conductor/electrode [108]. Silver as well as copper is used in the gate layer, however, both tend to oxidize. In the case of copper might cause an additional increase in resistance. Even though oxidation of silver does not increase its resistance, the effect on the semi-conductor layer if a silver oxide is formed shall be investigated.

Regarding the dimensions of the contacts, the distance in between the two contacts, source and drain, as well as high accuracy in the pattern was most important. The channel width had to be a maximum distance of 100 μm from source to drain. This was not achievable with some of the techniques. However, as described below still some of those techniques have a great deal of potential for further research. The channel width of 100 μm is relatively large when compared to common micro-electronic components. Thickness of the electrodes was envisaged at 100 nm minimum but thicker contacts were preferred to increase robustness of the layer. A thickness of 100 μm would have been optimal.

Baring above deliberations in mind, the following evaluation criteria were applied:

- non-contact technique
- high work function of material deposited
- pattern accuracy and channel width of max. 100 μm between source and drain

Several options for application of the top-electrodes have been tested.

8.2. Deposition of contacts by drop-casting of silver conductive screen printing ink

This technique has been tested using copper plates with the dimensions 50 mm x 25 mm, The plates have been coated in polyimide before application of the top-contacts. Initially, a silver screen printing ink from Acheson (Electrodag PF-410) was used. The silver screen printing ink was cast and dried at 100°C on a hot plate for 15 minutes. A drawing of the drop-casted top-contacts and their location on the filament is shown in Figure 78.

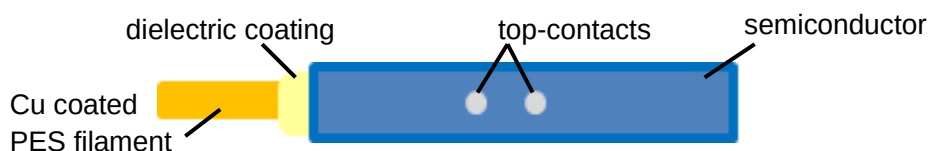


Figure 78

Scheme of drop-casted ink on filament

During characterization of the polyimide layer, an increased number of closed circuits was observed. The screen printing ink contained a solvent. It was tested in order to ascertain whether it might cause damage to the polyimide layer. It was found to cause the increased number of closed circuits.

A substitute screen printing ink was identified and used, The datasheet of the screen printing ink from DuPont (5025, silver conductor) stated that the screen printing ink was suitable to be applied on polyimide and other polymeric materials like polyester. Once the contacts were casted, the drying was completed as described above. The supplier recommended a drying time of 5-6 minutes at 120°C.

The number of closed circuits was reduced once the substituted screen printing ink was applied. Drop-casting was used for applying the top-contacts using silver conductive screen printing ink. In this study, drop-casting was the chosen method for working with flexible-cylindrical substrates (polyester filament) and planar-rigid substrates (copper plate) using nano silver jettable ink (see also chapter 8.5, p. 188).

8.3. Circumferential evaporation

Circumferential evaporation enables depositing the electrode on the entire circumference. During the evaporation process the substrate is rotated at constant speed. This is not achievable with normal evaporation chamber setups. To achieve circumferential evaporation, the evaporation chamber must be equipped with a sample holder that rotates the sample in the vacuum chamber at a predefined constant speed.

- i. State-of-the-art research conducted at TU Darmstadt, DE

The following section summarises salient points in subsequent research regarding circumferential evaporation on the fibrous substrate.

Professor von Seggern and Dr Könyves-Toth at the department for Electronic Material Division at Technical University Darmstadt (TU DA), produced organic light emitting diodes (OLED) on polymeric fibres by thermal evaporation. The configuration of this OLED and the working prototype are shown in Figure 79. The fibrous substrates had a diameter of 1000 μm and 500 μm . Best results have been achieved, apart from those using glass fibres are those using polymer hard-clad silica (HCS) coated with Ethylene tetrafluoroethylene (ETFE) [109]. Figure 79 shows a scheme of OLED fibre.

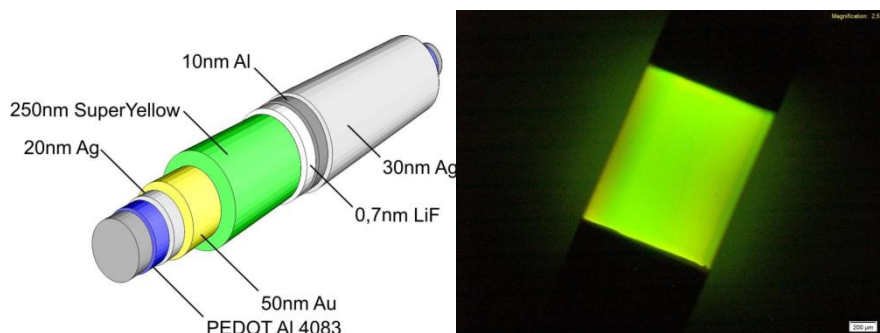


Figure 79 Scheme of OLED fibre as produced by TU Darmstadt within the LUMOLED project (left) and working prototype (right)

The system at TU DA allows a rotation speed of up to 5 rpm. Structuring is accomplished by shadow masks that can be closely installed underneath the substrate. The rotation of the substrate is synchronized with the rotation of the fibre, using this technique helical structures can be deposited, too. The system is capable of mounting 5 substrates at once. To fit the dimensions of the sample holder, the samples should have a maximum diameter of 1500 μm and maximum 60 - 70 mm in length after sample preparation. In addition the system is equipped with a load lock to transfer air sensitive samples to a glove box in nitrogen atmosphere if required. The accuracy is set to app. 100 μm since the system normally is used for OLED applications in which this is a suitable accuracy. If the shadow mask is moved closer (from 5 mm to 1 mm distance to substrate) an accuracy of 50 μm can be reached.

ii. Circumferential evaporation on polyimide and copper coated polyester filament

Dr Könyves-Toth kindly offered to conduct some preliminary test regarding the polyester filament substrate with a diameter of 800 μm . To test the applicability of this technique regarding the polyester filament, a copper-coated filament with a length of 15 cm was dip-coated in polyimide. The length of the substrate was important with respect to sample preparation and sample holder dimensions. Photographs of the samples during preparation and in the sample holder before circumferential evaporation are shown in Figure 80.



Figure 80 Substrates during preparation (left) and in sample holder before circumferential evaporation

The filaments were coated with a layer of 40 nm gold which equals a thickness of 126 nm without rotation. Six single contacts have been deposited on each filament. Evaporation was completed at a vacuum smaller than $4\text{E-}6$, and a rate of less than 2 $\text{\AA}/\text{sec}$. Rotation speed was set to 4 rpm.



Figure 81 Top-contacts circumferentially evaporated on filament with a length of app. 10 cm

Figure 81 shows, the contacts which were evaporated on the substrate had a high degree of accuracy and therefore would have been perfect for application as top-contacts in the OFET. The dark colour of the substrates surface might have derived from residues during the evaporation experiments on HCS ETFE fibre. ETFE is a fluorine based plastic (See: chapter 7.7. for description regarding the effect of fluorine on the copper layer).

During testing the electric contacts on the polyimide-coated substrate, a closed circuit between the top (source or drain) and bottom electrode (gate) was observed. The gold contacts which should be electrically insulated from each other by the polyimide layer showed a resistance of less than 300 Ω . This was only a short test for conductivity in which the establishment of contact was not optimal, consequently the resistance might have been caused by contact resistance.

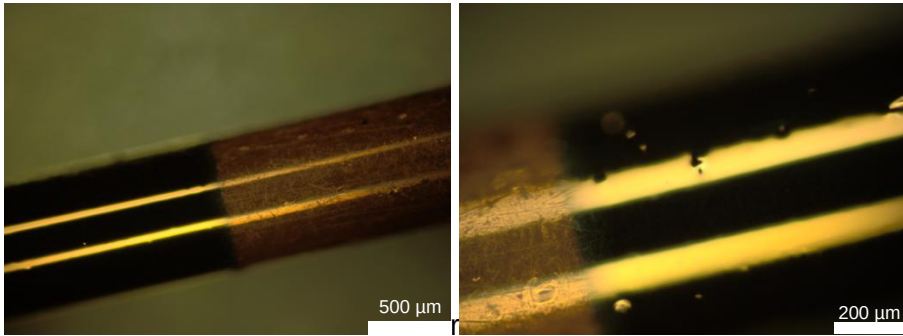


Figure 82 Circumferentially evaporated contacts on polyimide and copper coated polyester filament at a magnification of 5x (left) and at 10x (right)

The causal relationship could not be established with any degree of certainty, however as roughness of the layer is a crucial point in generating a reliable dielectric layer, it was thought that some crater-like defects in the copper layer might be increasing the roughness at certain points (Figure 82).

iii. Roughness of polyester filament surface

Even if overall roughness remained low, the polyimide coating was not capable of compensating for the difference in thickness at these points. The scheme in Figure 83 illustrates the effect.

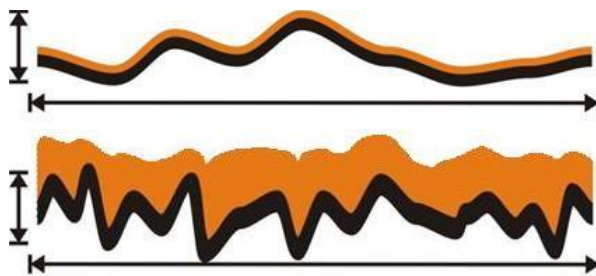


Figure 83 Scheme comparing coatings at the same overall roughness but with tremendous difference in peak height, based on results of the LUMOLED project [110]

When comparing the values for roughness (see: Figure 84), it becomes apparent that the height difference in the underlying copper layer might have severely affected the insulating properties of the

dielectric layer. Initially this fact was not considered since attention was focused on the degree of smoothness of the polyimide layer which affects the crystallisation in the subsequently applied semi-conductor layer. This layer decreased the roughness of the polyester and copper layer and therefore was an optimal choice. According to this new insight, it is evident that dip-coating in polyimide did decrease overall roughness but did not always provide sufficient layer insulation.

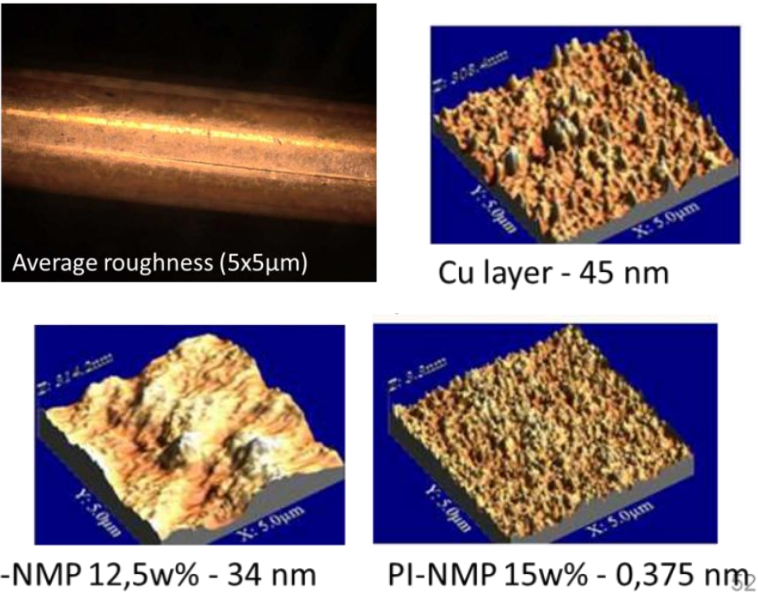


Figure 84 Microscopic image of copper layer on polyester filament (top left) and its AFM topological image (top right), and copper coated filament dip-coated in polyimide at 50 mm/min at a concentration of PI/NMP12.5w% (bottom left) and 15w% (bottom right)

A further reason why closed circuits had been detected could be that the evaporated material had diffused into the pores of the dielectric membrane as illustrated in Figure 85.

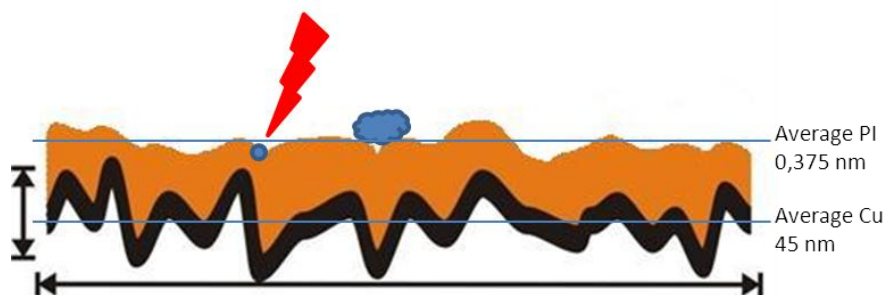


Figure 85 Scheme of diffusion of evaporated silver into the pores of the dielectric layer

To recapitulate, the semi-conductor must be insulated from the gate layer for generating the field effect. It is also a prerequisite that the polyimide layer to be as smooth as possible, even porosity or scratches of just a few nanometres thickness or dust particles may cause problems such as short circuiting.

iv. Improving the roughness of polyester filament surface

For future experiments, it was recommended to smoothen the surface of the polyester filament before coating as this showed higher levels of roughness in comparison with HCS ETFE fibre. At TU Darmstadt the HCS ETFE fibre was smoothed by applying 250°C for about 5 minutes with a hot air gun. The change in roughness is shown in Figure 86.



Figure 86 Smoothing effect in treating the ETFE coated HCS glass fibre for smoothing the surface [110]

The same technique was applied to the polyester filament. Using a hot gun, the surface of the filament was heated under tension. It was difficult to assess the proper time span required for smoothing to

avoid destroying the surface when applying the hot air gun. A trained eye might recognize the effect this procedure might have on the ETFE substrates. Microscopic images showed that the surface structure of the polyester filament was negatively affected by using this procedure. Delamination on the surface of the filament could be observed as shown in Figure 87.

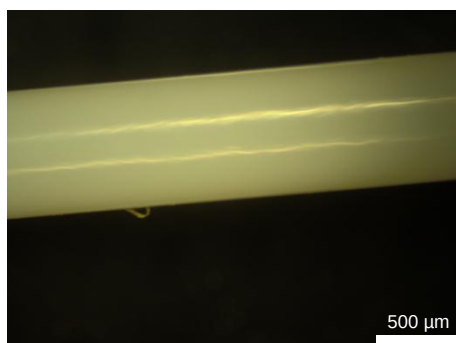


Figure 87 Delamination on polyester filament after treatment with hot air gun for surface smoothening

- v. Dip-coating of copper coated polyester filament with a length of 15 cm in polyimide for sample preparation in circumferential evaporation

Samples with an increased length of 15 cm were required for circumferential evaporation. Up to this point, only dip-coating of shorter pieces (6 cm) was studied. The setup for discontinuously dip-coating process had to be adjusted to fit the increased length of samples. The dip-coating distance, limited by the dip-coater's arm and the table top, had to be increased. This was accomplished by changing the direction of the dip-coater so that it was possible to dip-coat over the edge of the table. Access during the process of discontinuously dip-coating a filament with the length of 10 cm, needed to be least 20 cm. The rendered dip-coating setup is shown in Figure 88.



Figure 88 Dip-coating setup for dip-coating samples with increased length (15 cm)

During dip-coating, the filament's shape itself influences the dip-coating procedure. It became evident that during dip-coating compared to previous application techniques like electroless copper deposition, the dimensions and shape do play an even important role in this process. For the dip-coating process, the filament must be as straight as possible in order to fit into the vessel of the dip-coating solution (Figure 89). But also during drying, the shape of the filament was influencing the process, requiring the further adjustments to be made.

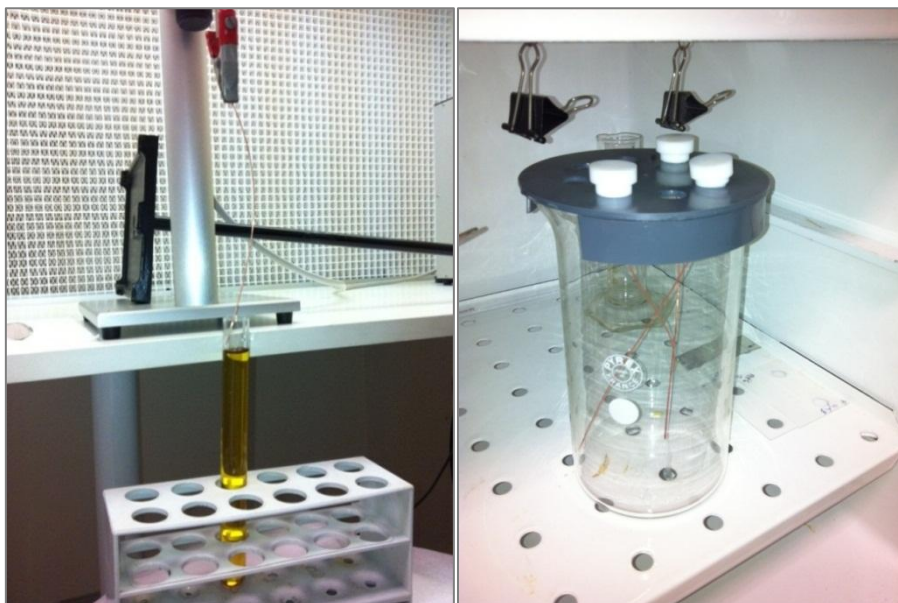


Figure 89 polyimide dip-coating (left) and drying of polyimide dip-coated filaments with increase length (right)

- vi. Straightening of the copper-coated polyester filament for dip-coating in polyimide

It can be argued that a bigger vessel should have been used. However, increasing volume of the vessel was not an option as the production and use of small amounts of dip-coating solution and the angle in which the substrate is supposed to be dip-coated and dried was more important. Therefore, the use of larger recipients was rejected. However, the filament still had to be straightened. To achieve the straightening, small weights as generally in use for fishing were attached to the end of the filament while being dip-coated. Unfortunately, due to the available weight size and the stiffness of the filament straightening of the filament during dip-coating was not achieved. Attaching the weight to the filament proved problematic. Furthermore, the material used for fishing weights did not fulfil the prerequisite such as being inert when exposed to chemical environment during dip-coating. Thus, a mechanical solution to the problem how to improve straightening of the polyester filament, such as adding weights, was unsuccessful.

To improve straightening of the polyester filament, once it was removed from the reel (see also Figure 72) it was wound onto a small hand weaving frame on which the stress on the filament could be adjusted and a straightening effect could be achieved (Figure 90)

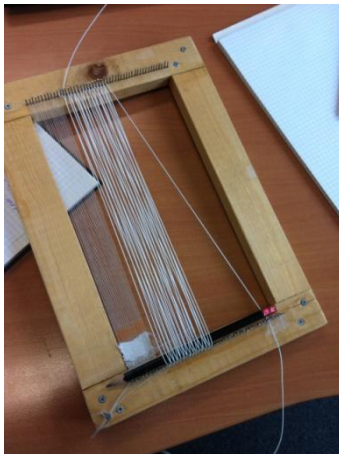


Figure 90 Storage solution to straighten filament once removed from reel

It improved the straightness of the filament prior to any application of coatings, however it did not solve the problem entirely.

Transporting the filament once dip-coated and dried was completed in test tubes with a custom made lid. This lid meant to ensure that the filament itself did not touch the inner side of the tubes by keeping it positioned in the middle of the tube. Due to bending the filament the latter was not achieved as shown in Figure 91. It is clearly shows that the filament's surface is in contact with the storage medium. The contact with the storage vessel might lead to deposition of dirt on the surface or might damage the filament.

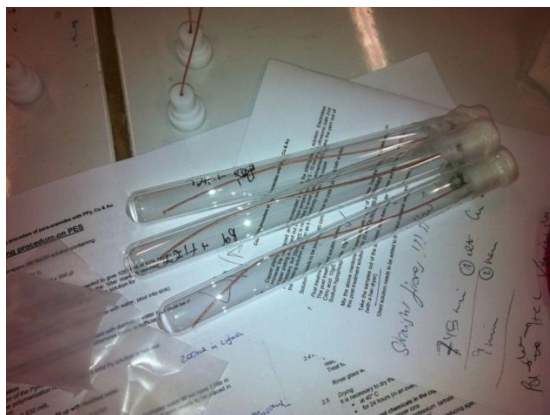


Figure 91 Storage and transport solution for filament with increased length

- vii. Conclusion for circumferential evaporation of top-contacts in concept of fibrous transistor

Unfortunately, Dr. Könyves-Toth left TU Darmstadt and the collaboration ceased. Evaporation of the contacts from a process technological point of view seemed to be very promising, particular with regard to the variation in patterning which can be achieved as shown in Figure 92.

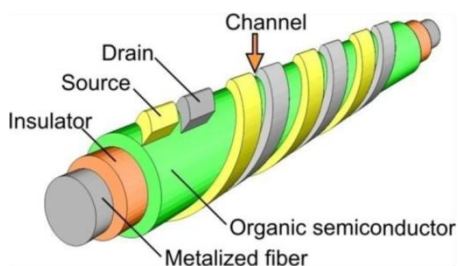


Figure 92 Scheme of pattern for helical contacts applied by circumferential evaporation [110]

From an industrial point of view, discontinuous processes like evaporation are less desirable not only with regard to batch production but also in terms of processing the final transistor filament.

Another problem might be the sensitivity of the organic semiconductor degrades in humidity, light and oxygen. At TU Darmstadt,

the samples once coated in vacuum were transported without being brought into contact with environmental influences and transferred into a glove box, where the OLEDs were tested.

8.4. Sputter coating gold plasma

The process of gold sputtering was investigated in an attempt to identify methods which would speed up the application of top-contacts in comparison to using thermal evaporation,

i) Process conditions during sputter coating

The process is relatively fast and easy to work with. In first trials, a SCD030 Balzers vacuum deposition system was used. The vacuum was generated until a pressure of 0.07 mbar was reached. Then the chamber was filled with argon gas to further increase the pressure to 0.12 mbar. Gold target disks were used as the source of conductive materials. At high voltage and a current of 30 mA the sputtering was accomplished after 90 seconds. A gold layer of app. 30 nm was formed on the flat surface of the copper plate.

The technique is relatively expensive depending on the source (gold). As pointed out above (chapter 8.1, p. 172), gold (4.75 – 5.1 eV) has a working function close to the semi-conductor TIPS-pentacene (5.3 eV) (see also chapter 10, p. 251) and therefore would be a better choice compared to silver or copper. Another option would be Platinum with working function of 6.35 eV. An example for a sputter deposition setup is shown in Figure 93.



Figure 93 Example for sputter deposition setup

In this trial experiment, masking for patterning the sputtered layer, was completed by using aluminium foil. The foil was fixed with double sided sticky tape to the platform and tightly fitted around the substrate which was a polyimide coated copper plate. Compared to the previously applied metal plate mask, aluminium foil shows more flexibility and might have an even fit around the polyester filament. Figure 94, shows the scheme of this arrangement whereas the translation into practice is shown in Figure 95.

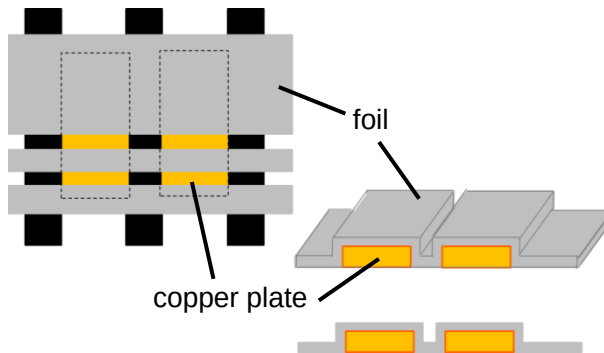


Figure 94 Scheme for masking the substrate to achieve the envisaged pattern

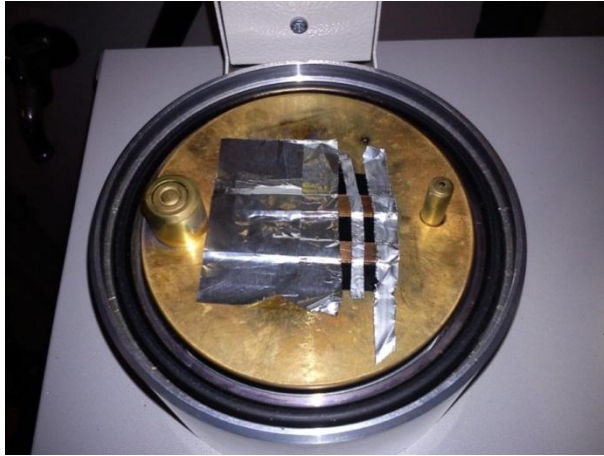


Figure 95 Platform with masking aluminium foil on copper plate substrate

- ii) Conclusion for sputter coating of top-contacts in concept of fibrous transistor

The result was not convincing since the patterning was worse in accuracy than compared to contacts applied by evaporation. The shadow generated by sputtering was visible with the naked eye. The process technology was excluded from further research. The contacts achieved with these techniques are shown in Figure 96.

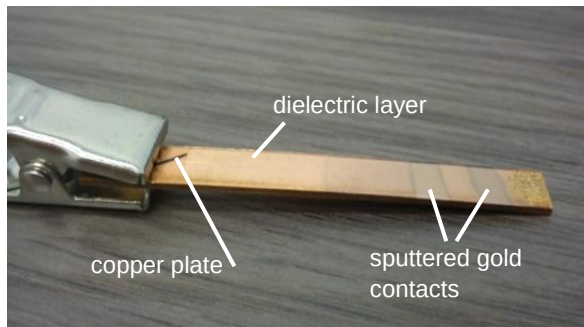


Figure 96 Gold contacts applied by sputtering

8.5. Ink-Jet printing with nano silver conductive ink

The concept of Ink-Jet printing was invented in the 20th century, since then this process technology has been well established in different

industries like publishing, and graphics, but also in packaging of products. Recently, inkjet-printing has also been used in application of functional materials in thin film technology such as the deposition of conductive jettable ink for electronics.

i. Advantages of ink-jet printing

Continuous inkjet-printing which would be optimal for continuous production in textile processing, belongs to the category of drop-on-demand (DOD) technology. There are different versions of print heads, enabling DOD technology:

- Thermal ink-jet (thermal expansion of ink)
- Squeeze mode print head, (piezoelectric material, tube)
- Bend mode print head (piezoelectric material, disk)
- Push mode print head (piezoelectric material, rod)
- Shear mode print head (piezoelectric material, channel)

Main effects used to generate DOD are thermal and piezo-electric effects. The piezo-electric printing does have the advantage over thermal expansion, because degradation of thermally sensitive materials can be avoided.

Other advantages of ink-jet printing are low cost due to low material waste, high flexibility in application of materials and dimensions. Initially, this technology was supposed to substitute other deposition techniques like screen printing or spin coating.

Currently, ink-jet printing is applied in a variety of areas. It is found in Printed circuits boards (PCB), radio frequency identification (RFID), photovoltaic cells (PV) or batteries and displays. Although promising, this technology cannot be compared as yet to silicon micro-fabrication technology. In the latter feature sizes of 28 nm is achievable which as a printing resolution not reached in ink-jet printing as yet. Meier et al. (2009) achieved the narrowest feature line width of 14-25 μm under research conditions. This represents the status of 1970 in semiconductor industry [111].

Photolithographic processes used in silicon electronic industry can use up to 34 different steps in the production of a component. In comparison, printing the different layers could reduce the number of steps to 4.

ii. Conductive jettable ink for ink-jet printing

Different types of conductive ink can be used in ink-jet printing, for instance, nanoparticle ink, organometallic inks, and conductive polymers [112]. On the whole, the ink will always contain so dispersants as well, such as adhesion promoters, surfactants, thickeners, stabilizing agents and other additives [113, 114]. The content which is mostly undisclosed by the supplier might influence the underlying layers and therefore must be tested.

Nanoparticle jettable ink is a suspension of nanoparticles in water or organic solvents such as toluene, ethylene glycol or cyclohexane. The solvent is meant to evaporate after deposition but should still be liquid at the nozzle. These days, nano-particles can be produced in high quantities which are dispersed in high concentration resulting in relative good electro-conductivity compared to the original materials i.e. nano silver conductive jettable ink to silver solids. The particles in the ink might cause agglomeration which might lead to increased viscosity and eventual clogging of the printing nozzle. Using organometallic inks allows sintering at lower temperatures (150°C) and eliminates risks for clogging.

The jettability of the ink is determined by the following fluid properties:

- *viscosity* (low enough to enable refill of ink reservoir in 100 ms and the expulsion of a droplet out of the nozzle by the transient pressure),
- *surface tension* (needs to sufficiently be high to prevent unwanted dripping from the nozzle but sufficiently low that the ejected droplet is able to detach from the nozzle)
- *density*

Not only the jettability is influenced by the listed properties but also the size and shape of droplet deposited. The inks used in the

experimental section met the demands of the printers for viscosity of 1-15 mPa.s and surface tension of 25-50 mNm⁻¹.

Printed materials must be sintered for generating continuous conductivity. Especially in particles, the connection to a neighbouring particle is a prerequisite to forming a consistent film. There are a variety of sintering techniques available

- thermal sintering
- electrical sintering
- photonic sintering (Heating)
- microwaves
- plasma
- light source (laser and flash lights)

Thermal sintering requires heating of the entire substrate, which can lead to gas emission or substrate shrinkage. It would be interesting to test other options, especially sintering with microwaves, because polymers are transparent to microwaves.

Inkjet printing is a common process technique used in printing of microelectronics like flexible circuit boards or alike. It is a direct writing process therefore no excess material is wasted. From a commercial perspective, this is a low-cost production process.

iii. Ink-Jet printing with nano silver conductive ink

The practical application of ink-jet printing with nano silver conductive jettable ink is explained in the following sections.

a) Positioning of the substrate for ink-jet printing

A glass plate was custom made to facilitate easy positioning and alignment on the printing platform in order to stabilise the substrates, forthwith referred to as the substrate holder. The filaments were fixed with tape on the substrate holder and placed onto the printing platform. Initially the filaments were affixed to the holder by microscopy to facilitate further analysis and detached for the electrical

measurements. At a later stage it was observed that the copper layer was heavily damaged when removing the tape and therefore, this option was rejected. The holder served for rough positioning of the substrate (Figure 97). Better results could have been obtained if the print head comprised a camera to detect the exact position of the print on the fibre. Positioning the head above the filament with a diameter of 1000 μm was not always successful.

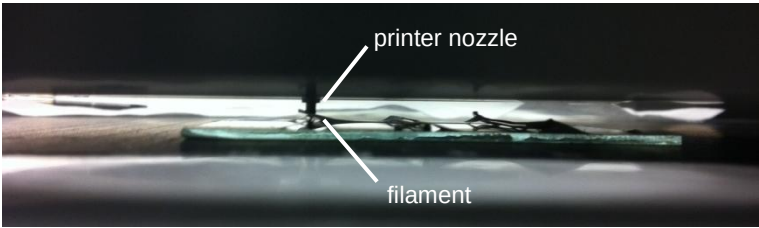


Figure 97 Ink-jet printer side view showing the printing nozzle above the polyester filament attached to the sample holder with tape for fixation

Both printing perpendicular and longitudinal to the filament's axis was tested. Exact positioning of the filament underneath the print head was impossible, the choice of perpendicular printing yielded superior results.

It should also be pointed out that the filament on the holder must be elevated to avoid that excess ink-jet printing ink runs down the curvature and builds a huge longitudinal contact at the back of the filament, connecting all electrodes as one and therefore rendering the contacts unusable, as the scheme shows in Figure 98.

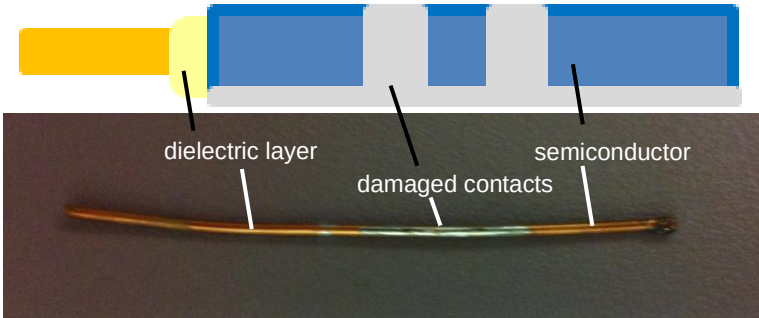


Figure 98 Schematic drawing (top) and picture (bottom) of ink run into one single contact on backside of filament during ink jet printing

This being the case, drying in upright position was not feasible, because the jettable ink was able to spread by running down the filament's axis. This problem was observed with all processes using jettable ink, but was less evident when using the screen printing ink which had a higher viscosity.

b) Ink-jet printing experiments

This section provides further information regarding the type of ink-jet printers used for experiments and results are discussed.

A. Microfab ink-jet printer, single nozzle

A small amount of nano silver jettable ink was supplied by SunChemical (Solsys Jettable Silver EMD5714, silver content 40%). The jettable ink was initially printed with a microfab ink-jet printer equipped with a single nozzle of 60 μm (MJ-ABP-60 μm). The prints were dried on a hot plate at app 90°C for 10 minutes taking into account the sensitivity of the organic semi-conductor. Magdassi *et al.* (2010) developed a sintering technique at room temperature [115]. Cleaning of the nozzle was conducted with isopropanol (IPA) or ethanol ($\text{C}_2\text{H}_6\text{O}$). Figure 62 shows a schematic drawing and a photograph of the printer.

The microfab ink-jet printer is very versatile and can work with a large range of materials. Conducting the printing itself is much more manual and is less automated then with other ink-jet printers.

The first tests resulted in contact electrodes with a good accuracy i.e. channel width and dimensions, when applied on top of the polyimide layer (Figure 99).

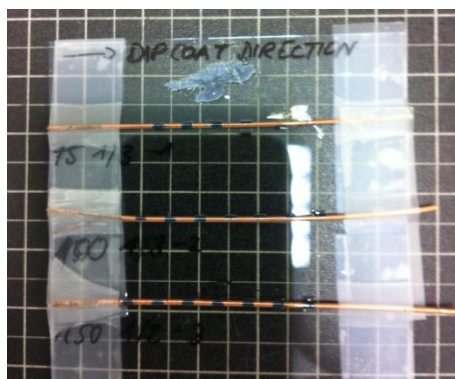


Figure 99 Ink-jet printed top-contacts show good accuracy

This changed when tested on the semi-conductor layer. Apparently the surface properties of the semi-conductive layer did not comply with jettable ink (Figure 100). The variation in printing pattern at the channel i.e. between source and drain electrode is shown in Figure 100. The printed contacts on the polyimide layer show defined borders, leading to more exact dimensions of the channel in between. In addition, the ink formed an even and well-distributed layer with almost no visible holes. In comparison on the TIPS-pentacene layer, the printed contacts do not form an evenly bordered pattern. The channel in between the contacts varies since the pattern is not well defined. Furthermore, the layer itself did not close completely and holes are visible. The ink is not uniformly distributed.

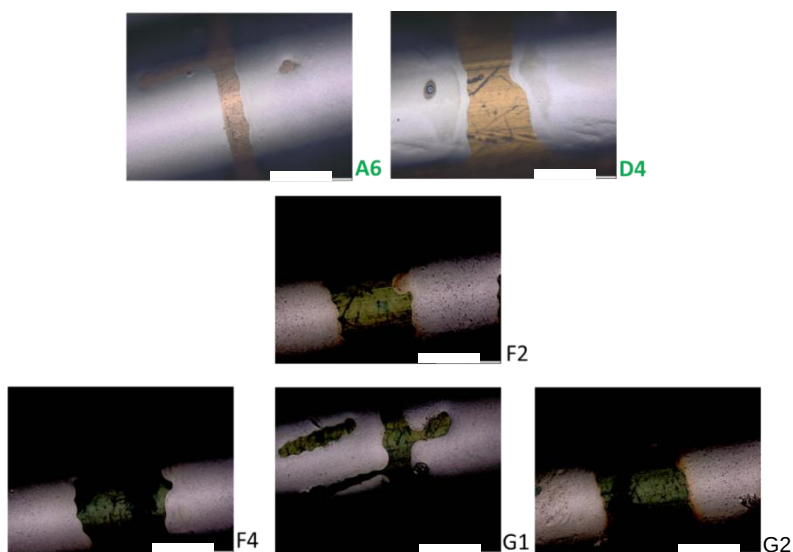


Figure 100 Overview on ink-jet printed contacts on polyimide layer (A6 and D4) and on TIPS-pentacene layer (F2, F4, G1 and G2), the scale bar indicates 200 μm

B. Dimatix ink-jet printer, multinozzle

After achieving the first results with the microfab printer, the attempt was made to print with a Dimatix ink-jet printer with a multinozzle system. Figure 63 shows a schematic drawing and a photograph of the printer.

Unfortunately, the jettable ink was not compatible with the printing system. The jettable ink dried right at the nozzle and even after repeated cleaning of the nozzle this problem could not be solved. It worthwhile noting that using the dimatix printer is a more expensive as the system works with cartridges, therefore, each ink requires having another cartridge and the ink which has gone into the cartridge cannot be removed for reuse.

c) Conclusion for ink-jet printing with nano silver conductive ink in concept of fibrous transistor

The potential of ink-jet printing for applying the top-contacts source and drain onto the coated filament was evaluated. Using the Microfab

ink-jet printer applying the contacts indicated huge potential for this technique in terms of further investigation. Unfortunately, the Dimatix printer, was excluded because the available ink did not fulfill the requirements for being used in this printing setup.

The process in ink-jet printing of the contacts could not be automated and therefore preparation, printing and drying was very time consuming, a faster solution had to be found. If applied on polyimide, the duration might not be an issue but when printing on the semi-conductive layer, time plays an important role due to the risk of layer degradation. TIPS-pentacene coatings were produced in the mornings, and should be characterized electrically on the same day.

Although in a laboratory scale ink-jet printing is highly time consuming, ink-jet printing is very promising, considering the up-scaling options, positioning could be automated and continuous production might be a possibility (Figure 101).

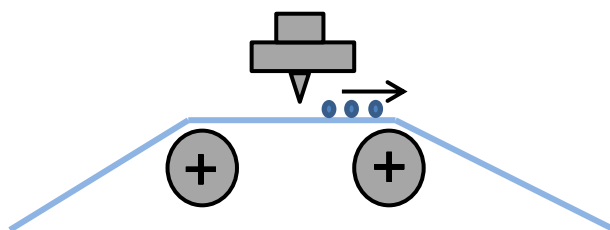


Figure 101 Scheme for u-scaling ink-jet printing on filament, the arrow indicated the transport direction of the filament

8.6. Deposition of nano silver conductive jettable ink by drop-casting

To establish a quicker method the nano silver conductive jettable ink was applied by drop-casting. This technique initially was used in combination with silver conductive screen printing ink on the polyimide coated copper plates. Now, drop-casting was completed on the semi-conductive layer deposited onto a polyimide and copper coated polyester filament in parallel to assessment by optical microscopy. Following this approach, the contacts were placed in regions where crystals were detected on in the layer. Consequently, positioning of the contact could be improved as well as time saved.

Deposited contacts by drop-casting of the nano silver conductive jettable ink was completed during microscopy (Figure 102). The samples were dried in a sample holder (chapter 7.7, 168 pp.) in upright position, which sometimes caused problems when excess ink was spreading, as described above (see section 8.2). Apart from elevating the sample during drop-casting, no further measures were taken (Figure 102).

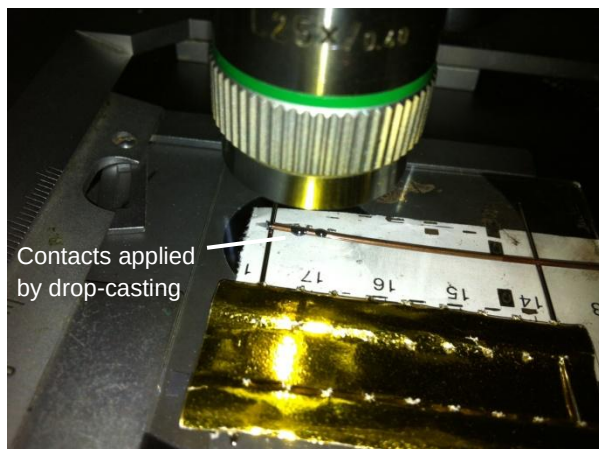


Figure 102 Drop-casted nano silver conductive jettable ink on filament during microscopy

8.7. Conclusions for deposition of source and drain electrodes

Drop-casting with nano silver conductive jettable ink was shown to be the most suitable deposition technique application to the filament. Acceptable to good results in matters of contact dimensions and accuracy as well as with regard to time-saving and ease of application were achieved. Gold also shows the advantage of having a work function closer to the one of the p-type semi-conductor used in this study (see chapter 10). Unfortunately, gold has to be sintered at even higher temperatures (300°C) which might make it impossible to use if the organic semi-conductor is applied beforehand. As an Option, a bottom-gate-bottom contact (BGBC) transistor architecture in which the semi-conductor is applied after the deposition of the contacts might make the application of nano gold conductive ink more feasible.

9

Dielectric layer

Chapter 9 describes and analyses experiments regarding the dielectric layer within the fibrous field effect transistor. It defines the criteria for evaluating the dielectric layer and presents options for materials and processing techniques. The experiments concentrate on optimizing the dip-coating process with special regard to solution concentration, choice of solvent, dip-coating speed and drying procedure.

9.1. Evaluation criteria for the dielectric layer

Developing a homogeneous insulating layer with constant minimum thickness and low roughness is a prerequisite for optimal transistor properties [116-118].

1) Minimum layer thickness at maximum insulating properties

This section of the dissertation examines the transistor architecture, the thickness of the dielectric layer which determines the required level of turn-on voltage which must be applied as well as considering the performance (field efficiency) of the transistor at least in part. The thicker the layer, the higher required voltage must be to start the transistor to facilitate the current to flow from source to drain contact. Operation at low voltage is preferable, not only in terms of normal practice in electronics, but also in view of the potential end application such as fibrous transistors in wearable electronics., Therefore, the aim of this experiment is to develop a very thin layer with just the right insulation properties (see: chapter 6, p. 133).

2) Minimum layer roughness

The roughness of the dielectric layer affects the molecular ordering of the subsequently applied semi-conductor during solidification [119]. When the semi-conductor self-assembles after being deposited on the dielectric layer, a higher roughness can lead to the formation of voids and defects in the semi-conductor layer. Therefore, the layer's roughness and heterogeneity resemble traps for charge carriers, which decrease the performance of the transistor, as well as the mobility of the electrons (carrier mobility), and the switching speed (on/off ratio) of the transistor (see chapter 6, p. 133). Roughness, in addition to the overall morphology, is therefore a reliable performance indicator and therefore crucial to the performance of the final component [120, 121].

3) Appropriate mechanical properties

The dielectric material, once deposited as a film on the substrate, should mimic the mechanical properties of the substrate i.e. having a similar flexibility or strength. In addition, the layer should serve as a

protective layer, shielding the underlying copper layer from e.g. humidity to avoid oxidation or degradation [45].

9.2. Choice of material and process techniques

On the whole, in microelectronic thin film device manufacturing, a dielectric layer has to meet some fundamental conditions for application in organic field effect transistors. In this instance it means the layer should be as thin as possible but still electrically insulating. To meet these conditions, many inorganic but also organic materials, have been assessed for their suitability as dielectric layer, for instance polystyrene, polyvinylalcohol (PVA) or polyimide [96, 122-125]. Polymeric materials used as dielectric are the perfect match for textile substrates. With their flexibility, these organic materials are very compatible with textile substrates.

As the presentation of the study concentrates on low temperature processes, polyvinylalcohol (PVA) nor polyvinylpyrrolidone (PVP) were considered for application. Once deposited in form of a solution, the polymers have to be cross-linked. This involves the addition of other chemicals e.g. cross-linking agents [62, 63, 91] and a curing step at elevated temperatures at a minimum of 200°C [62, 91, 126-128]. Both have the potential of presenting risk factors in terms becoming a negative influence on substrate or underlying layers.

Polyimide films were used as dielectric layer in electronics as early as the late 1970s [129]. Even before high quality insulating layers made a come-back as a research topic meeting the ever-increasing demand in the field of thin film microelectronics. Youngs *et al.* (2006) [130] showed, that the absolute volume of global publications regarding dielectrics increased at steady pace over the years. Frequent researched topics are high permittivity (high dielectric constant (k)) dielectrics for electronics applications, and the role of the interfaces between the different layers i.e. thin films [119]. Materials with a high dielectric constant are less prone to leak current and therefore enhance transistor performance. Top three application areas for research, regarding dielectric materials in 2004, were

related to capacitors, insulators and transistors [130], the functionality of the latter is the research topic of this dissertation.

Polyimide was chosen as the dielectric material as it has good flexibility [96], low conductivity, high breakdown voltage and high dielectric constant. The dielectric constant of polyimide varies with temperature. At 150°C, its dielectric constant is approximately 3.5, whereas it decreases to 3.02 at 350°C [96]. The dielectric constant is an indicator for the insulating properties of the material.

The insulating properties were demonstrated by Maccioni *et al.* (2006) who used a cylindrical metal fibre with a uniform polyimide layer of 1 μm (purchased from Elektrisola) indicating a leak current of below 10^{-10} A [65]. A theoretical value of 550 nm for the insulating layer thickness with a leak current of 10^{-9} A was defined by ProeTex (2007) [64].

Furthermore, polyimide's biocompatibility is a plus when considering applications close to the skin. Polyimide films substrates are commercially available for example as Kapton Film (DuPont) [131] and are frequently used in the electronics industry.

Imides normally exist as monomers. These monomers can be transformed into polyimide by imidization, as reaction between for example a dianhydride and a diamine. The polymer used in this study, comes as a powder and has the advantages of being fully imidized, being soluble in a variety of solvents and processable at low temperatures. According to the producers, coating with polyimide results in a durable and tough layer. Polyimide has an excellent chemical stability and shows good adhesion to various surfaces [94]. Polyimide is stable towards most of standard solvents, unlike other polymers e.g. polyethylene or polyester [132, 133]. This is an important prerequisite for subsequent deposition of the organic semiconductor.

The insulating layer should have similar mechanical properties as the substrate in order to allow bending and stretching during the final textile integration, e.g. by weaving [45]. In addition, the dielectric layer

should also prevent degradation of the underlying layer, by being water proof and inhibiting oxidation of the layers beneath [97].

Many solutions have been found for depositing a perfect dielectric layer on rigid flat substrates. This includes application via different coating processes like evaporation, lithographic or etching processes, spin-coating, ink-jet printing, spray coating, drop casting and screen printing can be used [120]. Often those processes are discontinuous and therefore are not an attractive option for application in continuous production of transistor filaments.

Polyimide is compatible with solution processing [122, 134]. This is an advantage because solution processes are frequently used in processes in the textile industry e.g. pre-treatment, printing, and finishing [135]. One of the techniques in solution processing is dip-coating which in the textile industry is also called padding. Padding is the continuous application of dip-coating (see chapter 6.2, p. 143)

Cardoen *et al* (2007), successfully deposited a dielectric layer on copper-coated polyester ribbons by dip-coating [97]. This process can easily be up-scaled from lab conditions to mass production [30]. However, the resulting layers suffered from heterogeneities and a rough cellular surface. Even though prior results were not satisfactory dip-coating is perceived as the process which is the most suitable to coat fibrous substrates, the process parameters are optimized to find the best process conditions.

9.3. Effect of variation in dip-coating speed and solution of polyimide in dimethylformaldehyde (DMF)

Until now, dip-coating of the dielectric layer with polyimide was only tested on metal copper wires [96] and polyester ribbons [97] but not on copper-coated polyester filaments. One of the reasons for this might be that realization of reliable conductive filaments, coated by electroless copper plating has not been achieved in the past [97]. These days, we are able to successfully reproduce conductive copper-coated polyester filaments with a diameter of 800 and 888 μm [66] which merits further investigation. Using a copper-coated PES filament in comparison to a copper wire has the advantage, apart

from its flexibility, that it is reluctant to break. Therefore it is the better choice when targeting an application in e.g. intelligent clothing [136].

Cardoen *et al.* [97] have shown that PES ribbons dip-coated in solutions from polyimide and dimethylformaldehyde (DMF) at concentrations lower than 10w% resulted in homogeneous coatings.

However, those coatings did not provide sufficient electrical insulation. Only a concentration of 10w% and higher, as well as, coating speeds equal to or higher than 75 mm/min achieved fully insulating layers on the PES ribbons [97].

The solution which adheres to the substrate when withdrawn from the dip-coating bath, forms the film as the solvent evaporates [101]. From the Landau-Levich equation, and underlined in the work of Arfsten *et al.* [103], it can be inferred that the thickness of the layer can be tailored by varying the solution concentration and the dip-coating withdrawal speed. Increasing either of these parameters not only creates a thicker dielectric layer, but also increases the risk of dielectric layer delamination. Previous research confirmed that minimal speed at which an insulating coating is obtained decreases with increasing solution concentration [66].

i) Thickness and resistance when dip-coating in PI/DMF

During dip-coating, the withdrawal speed was varied from 1 to 150 mm/min. The solution concentration was set in steps of 2.5w% in the range from 7.5w% to 17.5w%.

Subsequent to dip-coating, the filament is dried at ambient conditions at 22°C or alternatively, at elevated temperatures (60°C) for 24 h in vertical position, imitating continuous dip-coating conditions. Relative humidity during the dip-coating process itself depended on atmospheric conditions.

Resistivity measurements were conducted as described in chapter 6.3, p. 149. The insulating properties of the dielectric layer are shown

in Table 6. The layer thickness is shown regarding different withdrawal speeds and solute concentration of polyimide in DMF.

Table 6 Thickness [μm] of dielectric layer at different withdrawal speeds v (in mm/min) versus PI concentration in DMF (in w%). Shaded fields indicate conductivity (threshold $< 10^{10}\Omega\text{cm}$ [67]).

[mm/min] [w%]	[μm]							
	7.5	10.0	12.5	15.0	17.5			
1	Cond.	Cond.	0.21	0.25	1.53			
5	Cond.	Cond.	0.26	0.32	1.60			
7.5	Cond.	Cond.	0.57	0.56	1.96			
10	Cond.	Cond.	0.53	0.88	2.76			
12.5	Cond.	Cond.	0.56	1.09	8.70			
25	Cond.	Cond.	0.61	1.36	9.01			
50	Cond.	Cond.	0.86	2.83	9.20			
75	Cond.	Cond.	2.07	3.64	9.95			
100	Cond.	Cond.	2.19	7.65	12.83			
150	Cond.	Cond.	4.28	7.45	15.47			

The results show that the layer thickness increases with an increasing solute concentration (in w%) and increasing withdrawal speed (in

mm/min). When coated at a lower concentration of 7.5w% as well as 10w% polyimide, all samples remain conductive over the entire range of withdrawal speed (threshold $< 10^{10} \Omega\text{cm}$) [67]. Insulating layers were only obtained at a concentration of 12.5w%, when the dip-coating speed was relatively low, i.e. 50 mm/min. A cross section of the filament illustrating the previously deposited gate layer is shown in Figure 103.

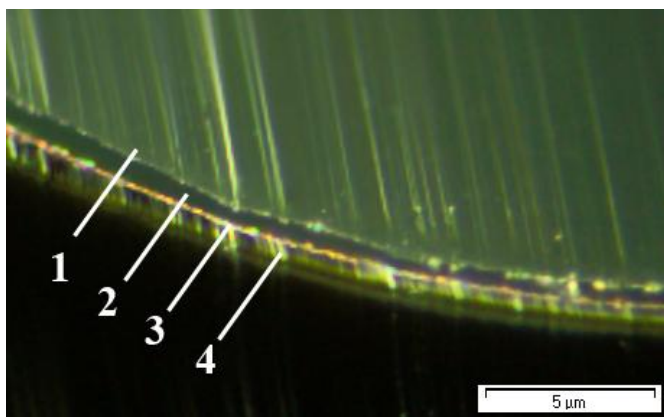


Figure 103 Microscopic image of fibrous transistor cross section. The image shows the polyester filament (1), the gate layer (2+3), and the dielectric layer coated from 15w% PI/DMF solution at 75 mm/min (4) [66]

It was observed that the lower the solute concentration, the higher the dip-coating speed must be to achieve an insulating layer. At a concentration of 15w%, an insulating layer was achievable at a withdrawal speed of 10 mm/min, as shown in Table 6.

As for the concentration of 17.5w%, all tested withdrawal speeds resulted in an insulating layer. To visualize the trend, the results are presented in Figure 104. A clear increasing trend in thickness was observed upon increasing the withdrawal speed.

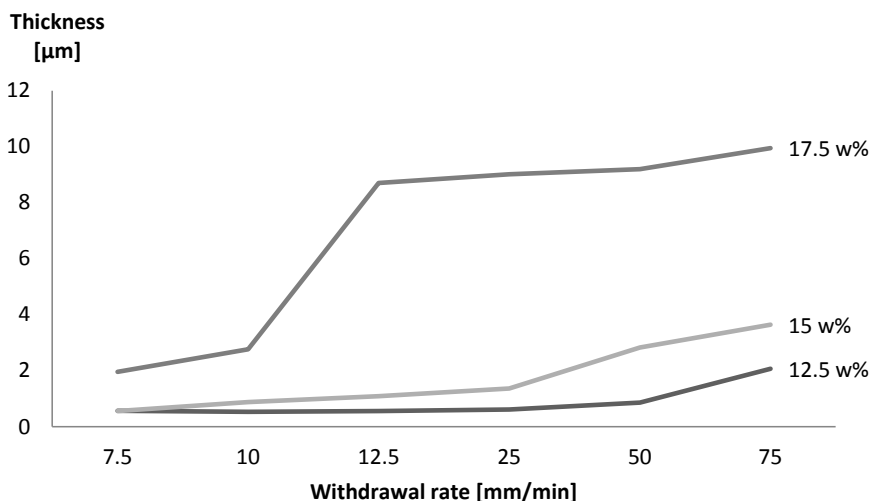


Figure 104 Thickness of dielectric layer in function of the withdrawal rate at concentrations 12.5w%, 15w% and 17.5w% PI in DMF

9.4. Effect of variation in dip-coating speed and solution of polyimide in 1-methyl-2-pyrrolidone (NMP)

Following the analysis of the layer dip-coated in the solution of polyimide in dimethylformaldehyde (DMF), polyimide in 1-methyl-2-pyrrolidone (NMP) was investigated as a potential solvent as well. As reported in literature, the use solvents which have a higher boiling point affects the morphology and therefore the properties of the deposited layer [101, 137-139]. During the solvent evaporation, molecules take more time to self-assemble, therefore NMP, which has a boiling point of 202°C [140], was chosen as an alternative solvent to DMF. The boiling point of DMF is only 153°C [141] under standard atmospheric conditions. Therefore, the solution with NMP was likely to show better results.

i) Thickness and resistance when dip-coating in PI/NMP

Again in this testing series, the withdrawal speed was varied from 1 to 150 mm/min. For comparison, an overview of the measured thicknesses for samples coated from 12.5w% DMF and NMP is shown in Table 7. For NMP solutions, it follows that with increased concentration the thickness increases and therefore the insulating properties of the layer increase. It could be observed that in the case

of NMP, the thickness was lower as compared to DMF at the same withdrawal speed and concentration. This effect became more pronounced at higher withdrawal speeds. Coatings at a concentration of 12.5w% and a speed of 25 mm/min and higher were insulating. When comparing the test results in the DMF series to those of the NMP series (see Table 7), we are in a position to conclude that a threshold thickness near 600 nm is required for the PI layer to become insulating.

Table 7 Thickness [μm] of dielectric layer at different withdrawal speeds (in mm/min) versus DMF or NMP as a solvent at a constant concentration of 12.5w% PI.
Shaded fields indicate conductivity (threshold $< 10^{10} \Omega\text{cm}$) [67].

	[μm]									
	DMF					NMP				
solvent [mm/min]	1	5	7.5	10	12.5	25	50	75	100	150
	0.21	0.26	0.57	0.53	0.56	0.61	0.86	2.07	2.19	4.28
	0.18	0.23	0.26	0.27	0.57	0.58	0.78	0.88	1.24	1.28

- ii) Leak current measurement related to dip-coating in PI/NMP and variation in dip-coating speed

In addition to the resistivity measurements, the leak current between the gate layer and one contact electrode applied on the surface of the

dielectric layer was investigated. Only those samples which have been tested over the entire range of the DC generator (up to 60 V) are tested with the same setup but with more exact tools than the multimeter, which only has an accuracy of 10^{-5} A. The HP LF Impedance Analyzer 4192A can measure up to 10^{-14} A accuracy, i.e. up to pA. Previously, the contacts on the layer were applied in silver jettable ink, the next series of contacts consisted of evaporated gold. The contact resistance with the gold evaporated electrodes is decreased as on the one hand gold is used which has a higher conductivity, on the other, evaporated particles result in improved contact between the layers.

As shown in Table 7, measurements showed that samples coated with a 12.5w% solution of polyimide in NMP at a speed higher than 25 mm/min were insulating. In Figure 105 gives an overview of the measured leak current of samples coated in 12.5w% PI/NMP at differing dip-coating speeds of 50, 75, 100 and 150 mm/min. All samples exhibit a leak current in the order of mA, a value which is unacceptably high for the chosen application. Therefore, it can be assumed that the layer is too thin to provide good insulating properties considering an evenly thick layer.

Furthermore, it was observed that the leak current decreased upon an increasing dip-coating speed. Once a certain threshold value was met, the leak current started to increase again at an increasing speed. The reason for this phenomenon could be the instability in the layer at an increased dip-coating speed. The layer becomes thinner at certain points across the fibre length as described in literature [142, 143]. Additionally, dip-coating at higher speed increases the risk of cracks. The gold electrodes make very close contact to the substrate, any cracks propagating in the PI layer might result in a strongly increased leak current. This possibility was not considered when using silver paste because this paste did not penetrate into the layer's voids because of the paste's higher viscosity and silver particle size. Therefore, the silver contacts remained on the surface and therefore, cracks in the PI layer did not influence the outcome of the measurements.

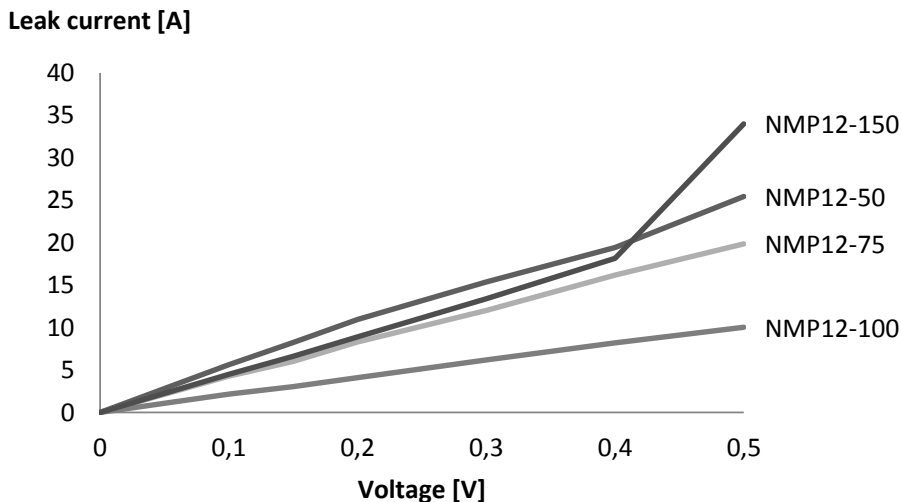


Figure 105 Leak current for samples coated from PI/NMP 12.5w% solution at dip-coating speeds 50, 75, 100 and 150 mm/min

iii) Increase in solvent concentration PI/NMP

Previously conducted experiments have shown that in order to increase the layer thickness, the concentration of dissolved polymer in the solution must be increased. This yielded more polyimide per solution volume, consequently a higher viscosity and thickness of the deposited layer. As a result, the concentration of the PI/NMP solution was increased to 15w%. The new measurement results show that the leak current is strongly reduced compared to the samples coated from a 12.5w% PI/NMP solution (see Figure 106). In this test series, again it was observed, that to a certain point, the leak current decreases at increasing dip-coating speed. After that point, the leak current increases again. Only at a dip-coating speed of 50 mm/min, the leak current stayed below the measurable range of mA detectable with the multimeter.

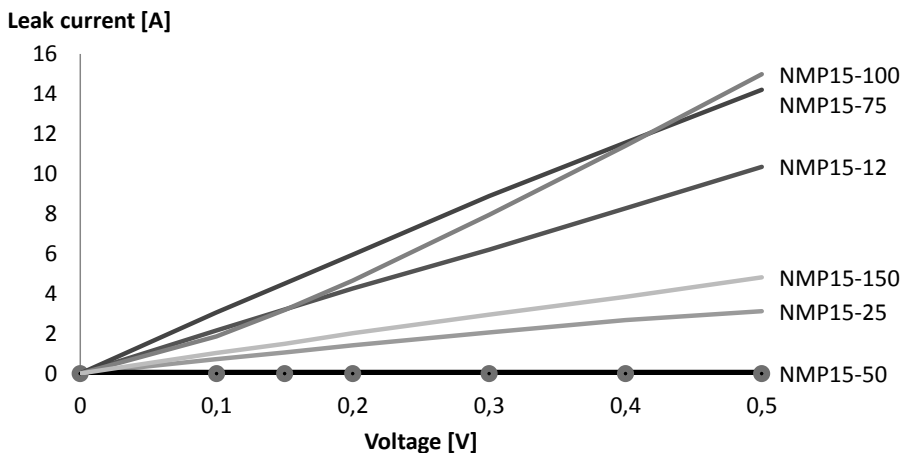


Figure 106 Leak current for samples coated from 15w% PI/NMP solution at dip-coating speed 12.5, 25, 50, 75, 100 and 150 mm/min

- iv) Leak current evaluation related to increase of solvent concentration PI/NMP

In comparison to the samples coated with PI/NMP solution, the combination with DMF as solvent was tested at a concentration of 15w%. The results are shown in Figure 107.

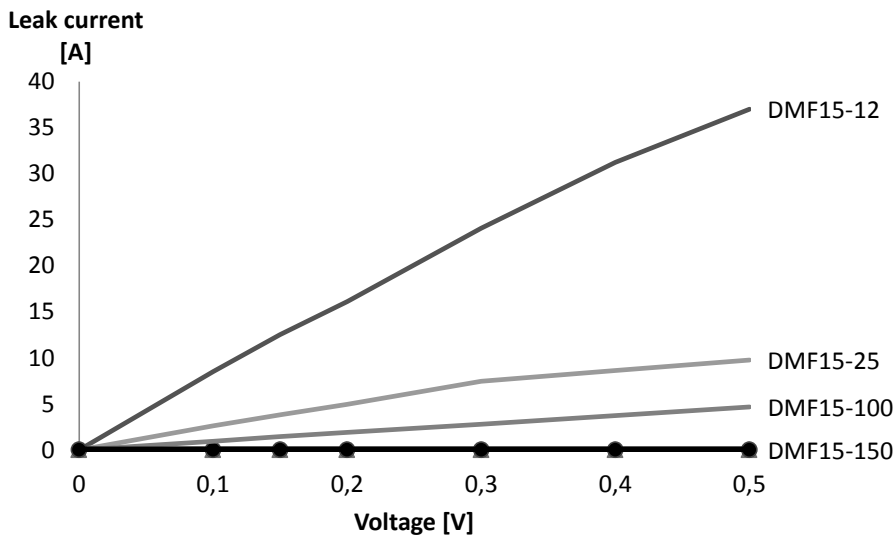


Figure 107 Leak current for samples coated from 15w% PI/DMF solution at dip-coating speed 12.5, 25, 50, 75, 100 and 150 mm/min

In this test series, a similar effect was observed. At a low dip-coating speed of 12.5 mm/min, the layer thickness was probably too thin and a high leak current was measured. At a dip-coating speed of 50 mm/min, the first layer with no measurable leak current was obtained. At 100 mm/min, again a slight conduction was observed, probably again due to small cracks in the layer.

Further experiments showed that samples from PI/DMF 17w% were slightly conductive when the dip-coating speed was 12.5 mm/min. Samples coated at higher velocities were insulating over the entire measuring range. The sample coated at 150 mm/min exhibited a small, yet measurable leak current of 0.01 mA when testing at 60 V indicating again occurrence of film instability or cracks in the dielectric layer.

For comparison, a commercially available copper wire coated with a 10 μm PI layer was tested. The result is shown in Figure 108. The leak current of the copper wire was very high. Therefore, this wire was unsuitable for the development of a cylindrical shaped transistor. Furthermore, comparing our sample coated with PI/NMP 12.5w% at 50 mm/min, the layer thickness does not seem to be sufficient. Best results were achieved by using a solution concentration of PI/NMP 15w% at 50 mm/min.

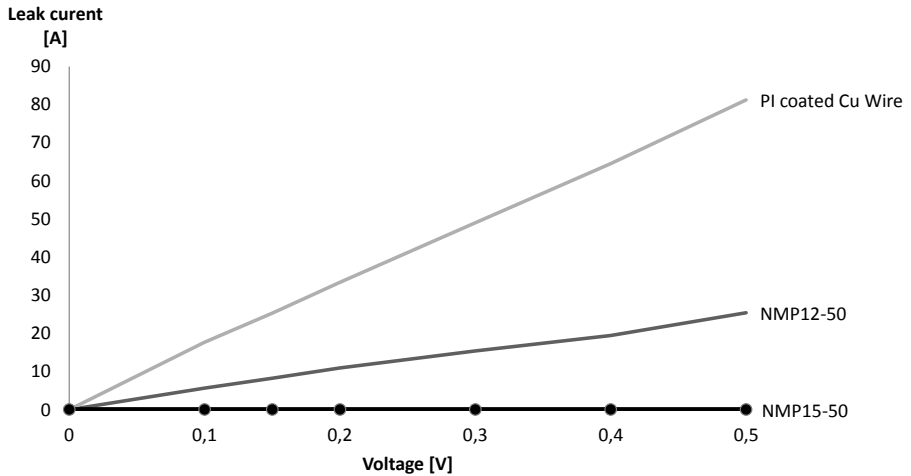


Figure 108 Leak current for samples coated from 12.5w% PI/NMP and 15w% PI/NMP at 50mm/min versus commercially available PI-coated copper wire.

v) Comparison of leak current measurements PI/NMP and PI/DMF

In Table 8, an overview is given of the insulating behaviour of the dielectric layer in different combinations of withdrawal rate and polymer concentration (DMF or NMP). The non-shaded fields indicate layers which had a leak current below the measurable range of 0.01 mA at 60 V. The shaded fields indicate a significant measured leak current. Corresponding thickness measurements are provided in μm .

Table 8 Overview leak current with gold contacts [μm]

	[μm]					
	NMP 15 w%					
		0.41	0.55	0.60	0.62	0.93
		Leakage	Leakage	0.64	0.71	0.75
		0.24	0.36	0.55	0.77	0.87
		0.51	0.80	1.09	1.20	1.15
						Leakage
mm/min	12.5					
solvent w%	25					
	50					
	75					
	100					
	150					

vi) Conclusions for Effect of variation in dip-coating speed and choice of solvent (DMF or NMP)

Based on the results shown above, it can be concluded that for a dielectric layer coated from an NMP solution, only the combination of

15w% and a 50 mm/min withdrawal rate resulted in a sufficiently insulating fibre with a thickness of 600 nm. When DMF was used as a solvent at 15w%, insulating dielectric layers were obtained for 50 and 75mm/min. Also here the ideal thickness was in the order of 600 nm. At PI/DMF 17.5w%, the fibres coated at 25 and 100 mm/min became sufficiently insulating.

Those samples were further examined with HP LF Impedance Analyzer 4192A, which can measure up to 10^{-14} A accuracy. A typical graph for a dielectric leak current was obtained for the samples coated at 50mm/min (PI/NMP 15w%) (see Figure 109). When plotting $\log (A)$ in function of $\sqrt{V}$ a linear correlation was observed, this is confirmed in Figure 110. Leak current was in the order of 10^{-9} A. Consequently, this dielectric layer could be used for further development of a transistor on a filament.

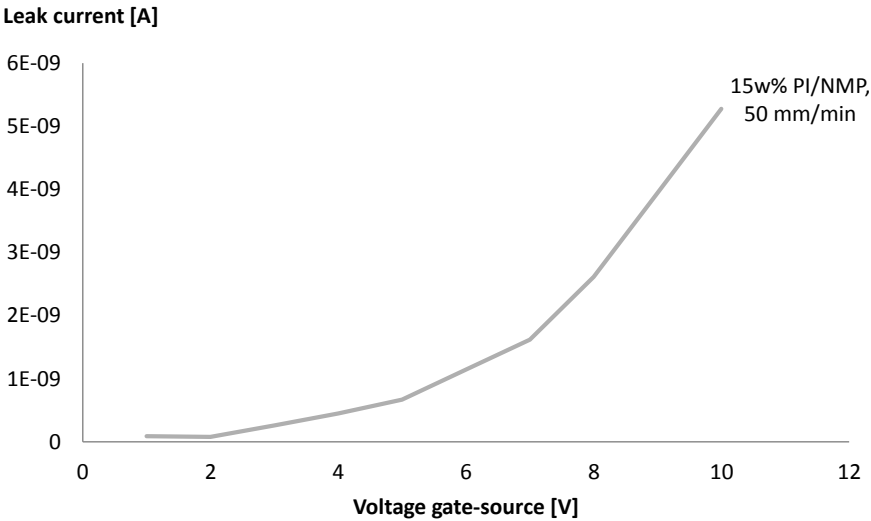


Figure 109 Leak current for samples coated from 15w% PI/NMP solution at withdrawal rate of 50 mm/min

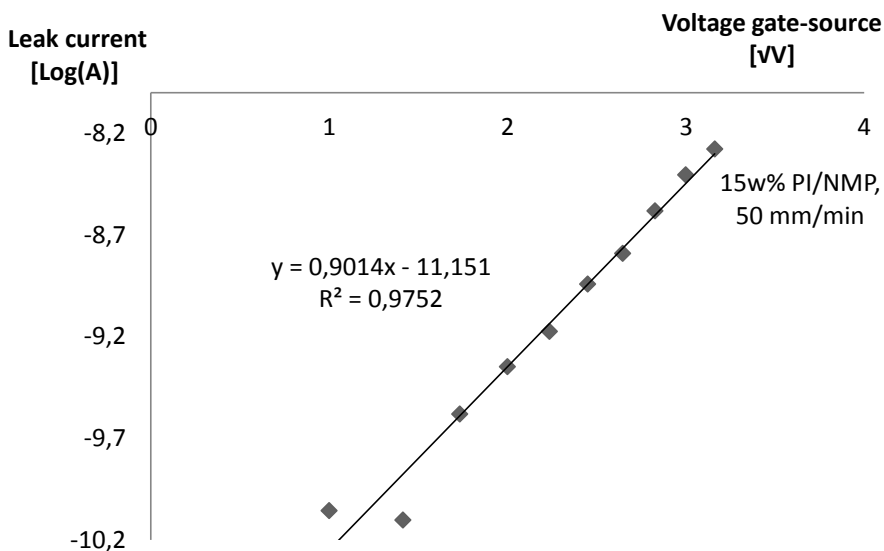


Figure 110 Leak current for samples coated from 15w% PI/NMP solution at withdrawal rate of 50 mm/min with log (A) in function of $\sqrt{V}$ showing a linear resistor typical behaviour

Indicated in Figure 111, for the insulating fibres with 15w% PI/DMF, a leak current in the order of 10^{-10} A was measured, which is a very good result. Only for 100 mm/min a sudden increase in leak current was measured, still well below 10^{-9} A. The leak current is much lower than previously detected with the multimeter. Potential causes could be that a new sample was produced and in all likelihood this time round no cracks had been formed. A higher dip-coating speed created increased layer thickness. In any case, it might be advisable to coat fibres at a lower speed as the aim is to achieve minimal thickness. Thus, the risk of cracks in the sample should be avoidable.

9.5. Verification of results by Poole Frenkel conduction

From the electric measurements obtained so far, it is clear that two kinds of PI layers were made. Comparing the results shown in Figure 105, Figure 106, Figure 107, and Figure 108, all layers show a relatively high leak current. Such PI layers should be considered as electric conductors rather than electric insulating layers. In addition, a leak current of 10 mA for an applied voltage of 0.1 V corresponds to a resistor of 10Ω , which is a rather small value.

Totally different results are shown in Figure 110. Firstly, the I/V curve characteristic is no longer linear. Secondly, the leak current is several orders of magnitude smaller (nA instead of mA range). It can be said, that the 15w% PI/NMP solution at a withdrawal rate of 50 mm/min is a good technique to achieve good insulation properties. A leak current of 5 nA for an applied voltage of 10 V corresponds to a resistor of 2 GΩ.

To interpret the results of Figure 109, the same data were plotted again in Figure 110, however, this time a semilog plot versus $\sqrt{V}$ was used. Although the leak current varied over almost two orders of magnitude (from 10^{-10} to 10^{-8}), a linear fit was achieved. According to the trend line, the experimental IV curve characteristic can be represented by:

$$I = 10^{0.9014} \bar{V}^{-11.151} = 7.0631 \cdot 10^{-12} \cdot 10^{0.9014} \bar{V} = 7.0631 \cdot 10^{-12} e^{2.0755\sqrt{V}} \quad (1)$$

One mechanism that explains a relation like (1) is known as the Poole-Frenkel conduction mechanism [144, 145]. The theoretical formula reads:

$$I = I_0 \exp \frac{q}{kT} \frac{\sqrt{qV}}{\pi \epsilon_0 \epsilon d} = I_0 e^{[\beta_{PF} \sqrt{V}]} \quad (2)$$

d : the thickness of the insulating layer

V : the applied voltage

$\epsilon_0 = 8.85 \cdot 10^{-12} \text{ F/m}$: dielectric constant in vacuum

$\epsilon = 3.5$: relative dielectric constant of PI

$k = 1.38 \cdot 10^{-23} \text{ J/K}$: Boltzmann constant

$q = 1.6 \cdot 10^{-19} \text{ C}$: elementary charge

T : absolute temperature

I_0 : reference current

Table 3 (NMP 15w%; 50 mm/min), shows that the thickness of the PI layer is given by $d = 0.6 \text{ } \mu\text{m}$ so that one gets the following numerical value for the Poole Frenkel coefficient:

$$\beta_{PF} = \frac{q}{kT} \frac{\overline{qV}}{\pi \epsilon_0 \epsilon d} = 2.0948 \quad (3)$$

This value is remarkably close to the experimental value 2.0755 in (1). The fact that the relation (2) was found to be valid for almost two decades of current values, one may conclude that the observed conduction phenomenon in the polyimide layers must be a Poole Frenkel conduction mechanism verifying the experimental results.

Another related theory is the Schottky conduction mechanism [146]. The theoretical relationship is now given by:

$$I = I_0 \exp \frac{q}{kT} \frac{\overline{qV}}{4\pi \epsilon_0 \epsilon d} = I_0 \epsilon \beta_s \bar{V} \quad (4)$$

Remark that $\beta_s = \beta_{PF}/2 = 1.0474$, a value which not does not sit well with our experiments. The main difference between Poole Frenkel and the Schottky conduction is that Poole Frenkel is a bulk phenomenon whereas the Schottky conduction appears at the electrode contacts. Some authors caution that one should be too eager to conclude that one is dealing with a Poole-Frenkel mechanism as soon as one is able fit the $\log(I)$ versus $\sqrt{V}$ plot onto a straight line. The fit must be valid for at least one order of magnitude of the current values, which was certainly the case in the experiment.

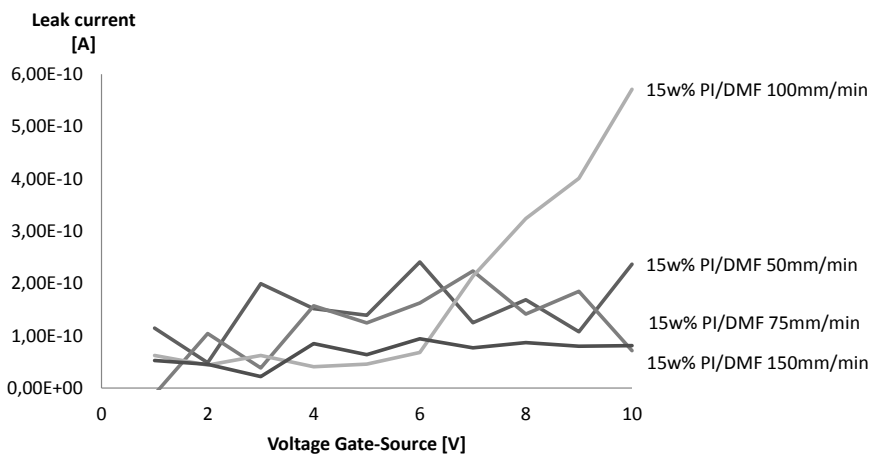


Figure 111 Leak current for samples coated from 15w% PI/DMF solution

For the samples coated with 17.5w% PI/DMF solution, a similar effect was observed as shown in Figure 111 and Figure 112. Because the layer becomes even thicker, a very low leak current was observed. The maximum leak current was measured when the dip-coating speed measured 25 mm/min. All other dip-coating speeds resulted in a leak current well below 0.1 nA.

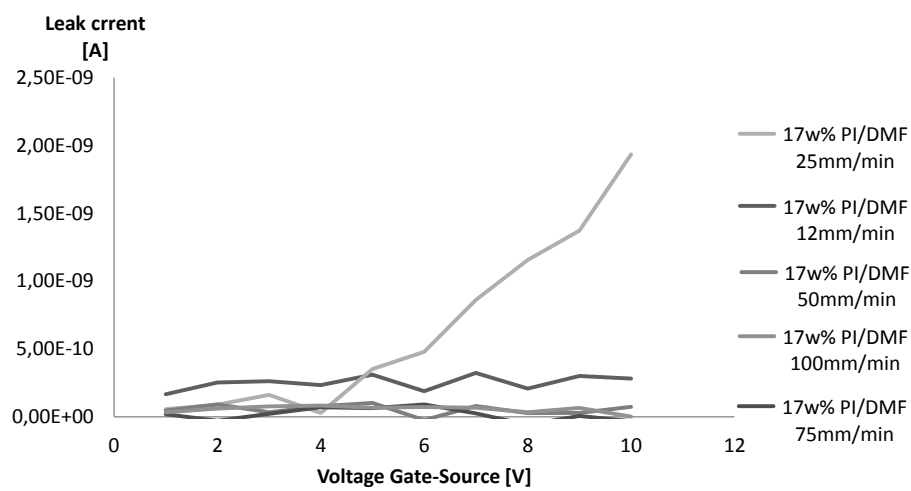


Figure 112 Leak current for samples coated from 17.5w% PI/DMF solution

Someya et al. (2004) obtained a leak current in the order of 10-10 A with a 500 nm thick spin-coated polyimide layer on a flat poly(ethylene naphthalate) (PEN) substrate. This result is comparable to the leak current obtained in this work on a cylindrical substrate [86].

In general, both higher PI content in solution and higher dip-coating speed, created thicker layers. Coating at higher speed compared to slower dip-coating speeds therefore resulted in achieving thicker layers. The choice of solvent also adds to the quality of the layer thickness [137]. DMF evaporates faster so entrapment of voids, air or humidity can occur leading to thicker layers. The influence of humidity on the dielectric layer will be discussed in the remainder of this chapter.

9.6. Effect of environmental humidity on layer morphology

As described in paragraphs 9.3 and 9.4, to find the optimal process conditions, the dip-coating solution PI/DMF as well as PI/NMP was prepared in a variety of concentrations. In addition, the withdrawal speed was varied during the dip-coating process. With both solutions, a whitening of the deposited polyimide layer was observed within the first 60 seconds after withdrawal of the filament from the solution in ambient conditions (see Figure 113 and Figure 114).



Figure 113 Whitening of polyimide layer on Copper-coated Polyester filament (PI/NMP 12.5w%, 50 mm/min)



Figure 114 Copper coated PES filament dip-coated with PI/DMF at 50 mm/min with a PI concentration of 10w%, 15w% and 17.5w% (from left to right)

This effect was less obvious with regard to withdrawal from solutions with lower concentration. The layer stayed almost transparent and only a slight change in colour was observed. At constant solution concentration, the higher the withdrawal speed was the more opaque

the layer became. As stated in chapter 9.3 (p. 203), increasing withdrawal speed or solution concentration increased the layer thickness. Therefore, it was inferred that the layer thickness has an influence on the whitening of the layer.

Polyimide is usually transparent in the spectrum of visible light, it does not comprise light-absorbent additive molecules such as pigments or dyes. Diffuse reflection can occur caused by light rays which are reflected in many random directions on rough and irregular surfaces. The cavities that were detected through SEM microscopy are therefore the cause for a decrease in optical transmission. This means, that the cavities (voids or cracks) reflect the light randomly, leading to diffuse reflection and therefore, the opaqueness of the layer.

Cavities could act as charge traps in subsequent application as dielectric layer in the transistor architecture. Hence, the cavities trap mobile charges flowing at the interface to the semi-conductive layer. This reduces field effect mobility and therefore, severely affects performance of the transistor. Consequently, reducing the layer's roughness/porosity is an important consideration in terms of further research.

To assess the surface morphology, a scanning electron microscope (SEM) at a magnification of 5000x was used. SEM analysis showed that small cellular holes in the order of magnitude of micrometers were formed at the layer surface. Increasing either the withdrawal speed (from 5 to 100 mm/min) or concentration (7.5 to 17.5w%), created larger cavities (Figure 115 and Figure 116)).

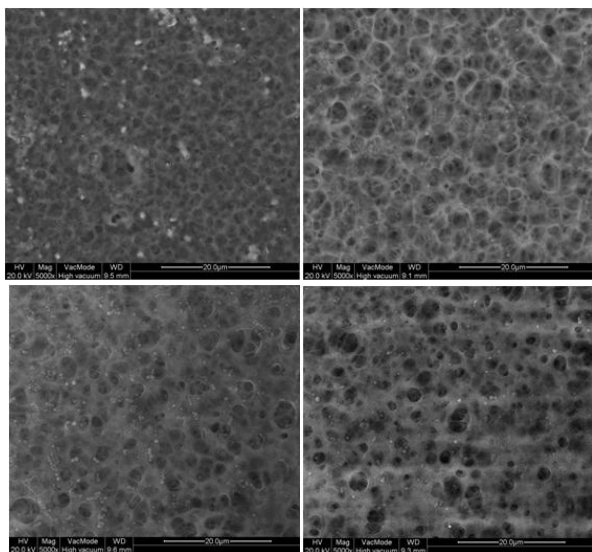


Figure 115 SEM images of PI dielectric layer dip-coated from 12.5w% PI/DMF solution with respective withdrawal speed of 5 mm/min (top-left), 25 mm/min (top-right), 50 mm/min (bottom-left) and 100 mm/min (bottom-right), the scale bar indicates 20 μm

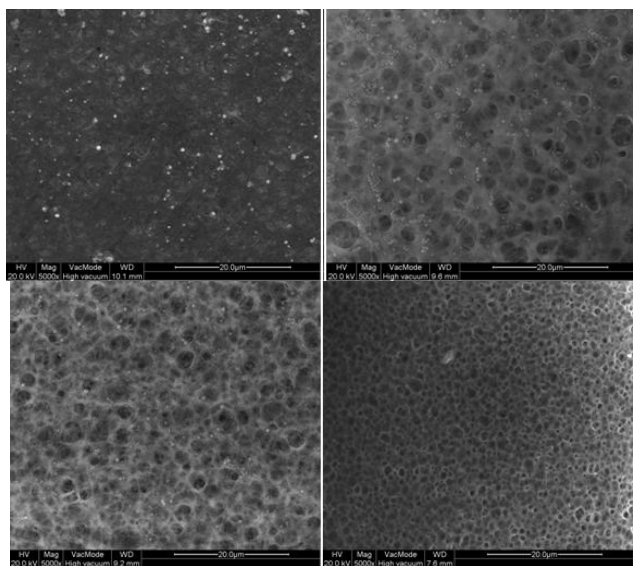


Figure 116 SEM images of PI dielectric layer dip-coated at a withdrawal rate of 50 mm/min and PI/DMF solution concentration of 7.5w% (top-left), 12.5w% (top-right), 15w% (bottom-left) and 17.5w% (bottom-right), the scale bar indicates 20 μm

Several parameters were investigated to improve the dip-coated polyimide layer morphology. The ambient conditions in the clean-room where the dip-coating took place were assessed and found to be unstable. A mobile weather station indicated a temperature of 22.0°C and a relative humidity of 25%. Humidity was a potential threat to the quality of the layer morphology. The probability that relative humidity was responsible for the discolouration also explained why the samples that were transparent still had white ends at the lower end of the sample. The samples were drying in upright position. Once the filament got withdrawn from the solution, gravity causes the solution to flow downwards on the sample resulting in a thicker droplet at the lowest point of the fibre. Because this part of the layer is thicker than the rest, it required a longer time to dry and it took longer for the layer to absorb water.

The environmental humidity was reduced from 25-30 % to app. 5 % when drying the freshly coated samples in an oven at 60°C. Drying the samples in the oven at low humidity led to complete transparency of the polyimide layer after drying. Samples were analysed at 5000x magnification with a SEM and compared to samples dried at ambient conditions. The result was impressive. Figure 117 shows SEM images of a PI/NMP coated fibre drying in a relative humidity (RH) of 30%, 18% and 5%. The increased transparency of the layer is an indicator that the diffuse reflection was reduced, therefore, an improvement of the surface morphology of the layer. Low humidity drying led to a decrease in number and sizes of voids in the layer.

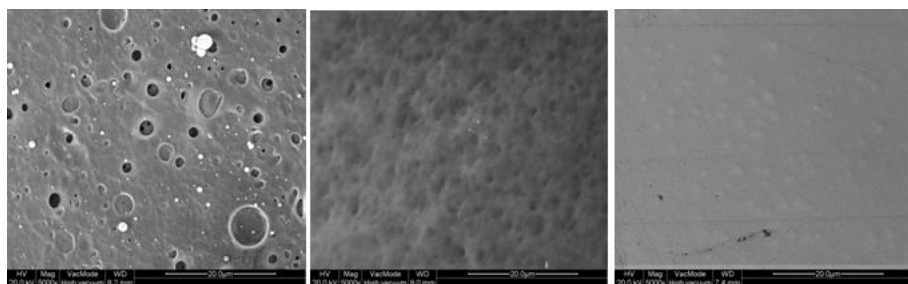


Figure 117 SEM images of samples coated with 12.5w% PI/NMP solution at 50 mm/min at relative humidity of (a) 30%, (b) 18% and (c) 5%. Picture (c) shows the highest transparency, the scale bar indicates 20 µm

In the literature, this phenomenon is described as vapour induced phase separation [95, 147, 148]. NMP is a very good solvent for water, which acts at the same time as a non-solvent for the polyimide molecules. In general, phase separation can be triggered by the so-called wet immersion processes. Here, the polymer solution is applied onto a substrate and immersed into a coagulation bath. The mass exchange is very rapid upon extraction of the solvent and penetration of non-solvent solidification. When solvent extraction is too fast, this process often leads to the formation of large holes.

Bouyer (2010) discussed the behaviour of polyimide-solvent-water systems. In situ measurements of concentrations of PEI/NMP/Water system were conducted at a relative humidity of 75% during the drying process [147]. A reduction in relative humidity from 75% to 43% at 40°C has increased the de-mixing time by a factor of six creating a more uniform cell distribution along the membrane thickness. If the value of the relative humidity is even more reduced, a dense film would be formed rather than a porous membrane. The minimum value of relative humidity to induce demixing has been reported at 27%, below this concentration dense polymer films were obtained from solutions with NMP [147, 148].

In PI, a similar mechanism as in PEI has been observed and the same solvent was used, consequently, the effect is thought to be similar. The obtained morphology was characterized by large cells near the air/solution interface and also a whitening of the layer was observed. According to J.H. Kim *et al.*, a similar morphology is obtained when quenching a DMSO/PI system in a water coagulation bath at 8°C [95].

For comparative purposes, a cross section was made of a sample coated from 12.5w% PI/NMP solution at speed of 50 mm/min and analysis with a Focused Ion Beam (FIB) microscope. The sample dried at ambient relative humidity of 30%, and the result is shown in Figure 118. A large macroscopic-void structure could be observed.

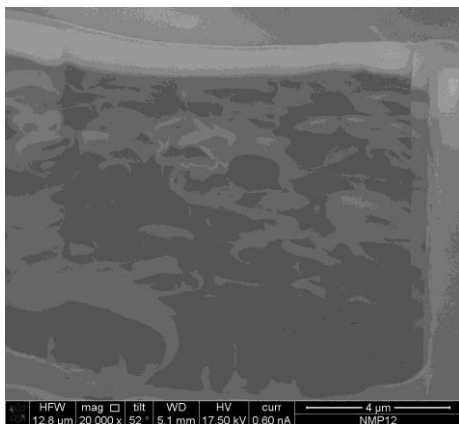


Figure 118 FIB cross section of sample coated with dielectric layer from 12.5w% PI/NMP solution at 50 mm/min in ambient conditions with RH 30%, the scale bar indicates 4 μm

When drying the coating at low relative humidity, small cavities seemed to have disappeared. Water begins to evaporate if the chemical potential of water in the liquid phase reaches its chemical potential in the gas phase. Depending on the respective evaporation rate, the composition path could stay in the homogeneous region [148]. For the PI/NMP system, this effect was stronger. This might be explained by the increased differential of the boiling point of NMP (207 °C) and water as compared to the differential between DMF (153°C) and water. Using high boiling point solvents results in a better morphology in film deposition [137-139].

As for the samples dip-coated with DMF based solution, it was observed that whitening of the polyimide film occurred within 60 seconds after coating. The process was reversed by putting the samples immediately into the oven (60°C), which created dense, transparent films. At lower dip-coating speed and therefore, longer coating procedure, the whitening became irreversible even after drying in the oven. SEM analysis led to the conclusion that the PI/DMF solution is even more sensitive to humidity than the PI/NMP mixture. To start phase separation, in the case of PI/DMF, less water must be absorbed. All samples dip-coated from PI/NMP 12w% and dried at 60°C were transparent (see Figure 119).

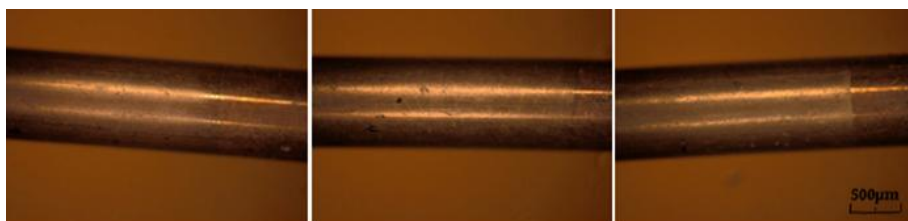


Figure 119 Copper-coated PES filaments dip-coated in PI/NMP solution at 12w% concentration and at withdrawal speed of 5, 25 and 75 mm/min respectively (from left to right). The layer remains transparent.

The absorption of humidity from the environment also could be observed during dip-coating. The polyimide solution started phase separation when the humidity in the clean-room was high (See: a picture below illustrating the polyimide dip-coating solution at a humidity of 45%).



Figure 120 Polyimide dip-coating solution at a humidity of 45%

It was suggested that using an ultrasonic bath might remove air bubbles that could be entrapped by stirring the solution during production polyimide dip-coating solution. Its use has been tested but since ultra-sonic baths inherently contain water, a direct effect on the solution i.e. change in colour of the top layer was observed. The

solution started phase separation which was not the indented result. Therefore the use of an ultrasonic bath has been assessed as not applicable.

Figure 121 shows thickness measurements results for 12.5w% polyimide/NMP solutions. The values for solutions from polyimide/DMF at concentrations of 15w% and 17.5w% are shown in Figure 122. See: section 9.4 (p. 207) regarding exact thickness values.

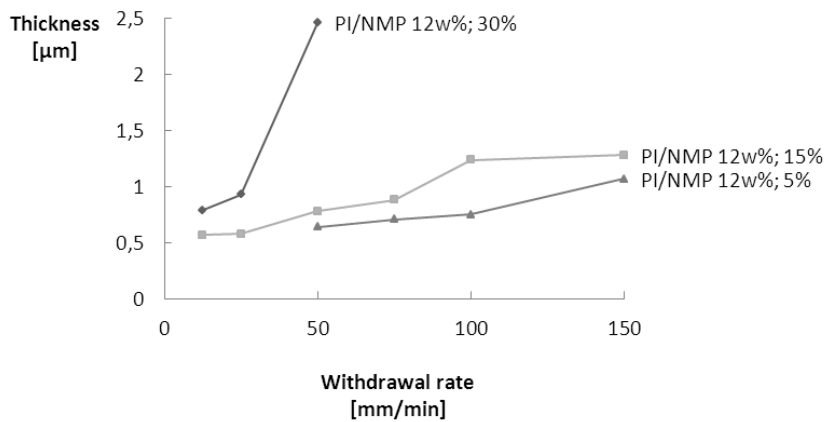


Figure 121 Thickness of PI layer coated from 12.5w% PI/NMP solution in function of the withdrawal rate at different levels of relative humidity

Figure 121 shows the layer thickness resulting from drying at a respective relative humidity in the oven at 60°C, at a relative humidity of 15% (transparent layers) and at a relative humidity of 30% (whitening of the film) was measured. It was observed that thickness increased with increasing relative humidity. This effect became stronger as the withdrawal rate increased.

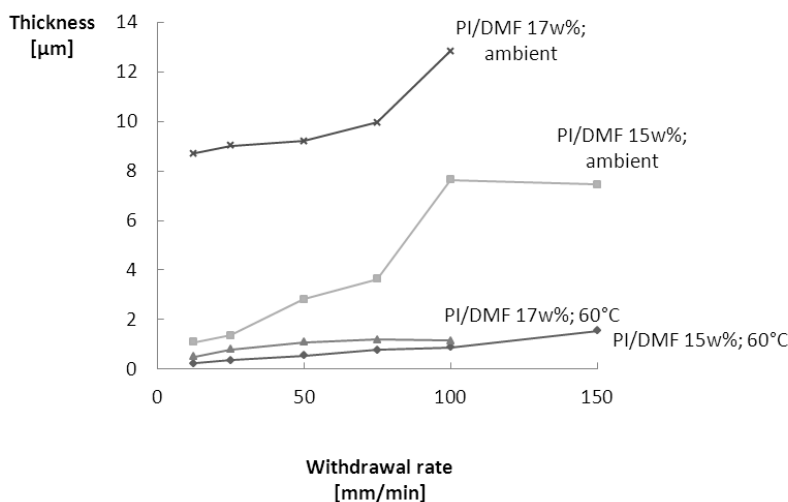


Figure 122 Thickness of PI layer coated from 15w% and 17.5w% PI/DMF solutions in function of the withdrawal rate at different levels of relative humidity

This experiment compared, only two conditions, dry conditions at 60°C and 5% RH and in ambient temperature and >15% RH. The increase of thickness was greater compared to the samples coated from NMP solution showing the effect of the increased sensitivity of DMF solutions towards humidity. Phase separation which occurs at high relative humidity levels result in a cellular morphology, consequently, the cavities which formed in the layer do fill a much larger volume with the same amount of material deposited.

The overall layer thickness in dry conditions showed that for compatible speed and solvent concentration, the layer thickness was lower when NMP was used as solvent. This effect became stronger as withdrawal rate increased. At a withdrawal speed of 25 mm/min and higher, all deposited layers were insulating. This corresponds with an approximate thickness of 600 nm.

The application of a silver paste as contact medium during measuring insulating properties, created a sufficient insulating layer ($R > 200 \text{ M}\Omega$) when the dip-coating speed was 50 mm/min at a concentration of 12.5w%. At a lower concentration, all samples remained conductive over the entire range of withdrawal speed. At higher

concentrations, an insulating layer was achieved at lower speed. At 15w% a withdrawal speed of 10 mm/min created an effective insulating layer. Thickness measurements lead to the conclusion that a threshold layer thickness of about 600 nm must be achieved to be sufficiently insulating.

To assess the improvement in morphology detected by SEM analysis (see Figure 115 to Figure 117), AFM scanning was chosen to quantify results. A sample coated with 15w% PI/DMF at 12.5 mm/min was compared to one coated with 12.5w% PI/NMP at 50 mm/min dried in ambient conditions. As a reference point for comparison, the roughness of the underlying copper layer was measured. Provided that the copper layer had a roughness of 45 ± 1 nm, the coating in polyimide solution with DMF or NMP as a solvent showed a roughness of 107 ± 2 nm and 34 ± 5 nm respectively. Voids which were detected by SEM beforehand also were clearly visible through AFM imaging. Coatings with DMF led to dramatically increased roughness compared to the roughness of the underlying copper coating.

Comparing the roughness of the initial copper layer, the surface roughness was improved when using NMP as a solvent for polyimide dip-coating. It was concluded that dip-coating with NMP as solvent resulted in a better morphology than with DMF, even at higher withdrawal speeds. A roughness of 34 nm at the interface of dielectric and semi-conductor is still considered very rough. Someya *et al.* (2004) reported a roughness of 0.2 nm of a spin-coated PI layer on a poly(ethylene naphthalate) flat substrate [86]. Therefore, further research was necessary to improve the morphological properties of the layer with NMP as a solvent.

As a final comparison, samples coated from 15w% PI/NMP as well as PI/DMF solution were produced at 50 mm/min dip-coating speed and dried at 60°C. Their roughness was assessed using AFM analysis (Figure 123). Both samples' surfaces looked perfectly smooth and the calculated roughness for both samples was almost equal with an average value of $0.375 \pm 0,007$ nm. This is an improvement with a factor of 285 compared to the first PI/DMF coated samples which were dried in high relative humidity. Therefore, the result was a dramatic increase of the material's potential to be used as dielectric at

the interface with the semi-conductor without excessive charge entrapment.

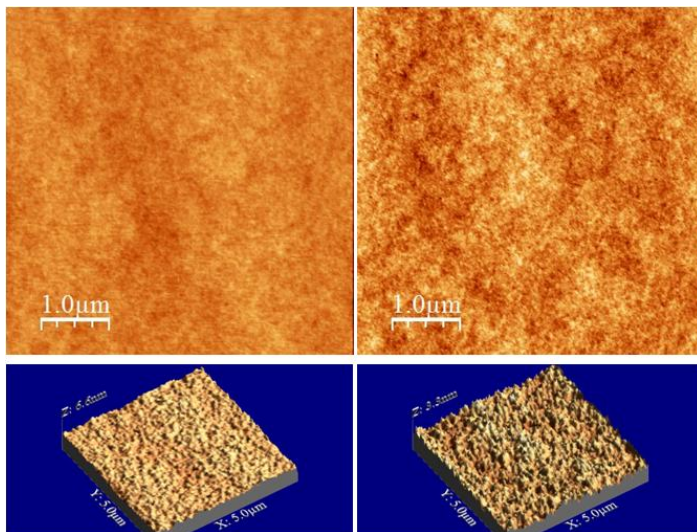


Figure 123 AFM images of samples coated with 15w% solutions PI/DMF and PI/NMP, at withdrawal rate of 50 mm/min from DMF (left) or NMP (right). Their 3D representation of the surface is given (below). The surface looks perfectly smooth.

To avoid humidity, even the solvents were dried by adding molecular sieves into the containers at later stage. Previously, activation of the sieves was completed by keeping them at 500°C for 20 h.

9.7. Electrical characterization of the polyimide layer in view of subsequent application of semi-conductor layer

Several methods for electrically characterizing have been investigated determined by experiments on the polyimide layer, which were also applicable in terms of the semi-conductive layer (see chapter 10). In the experiment described below, only the measurements on the polyimide layer deposited on a planar copper plate were considered.

While measuring resistance of the dielectric layer on a copper plate, it was observed that slight shifts in position of the crocodile clamps as

used initially damaged the layer. The resistance measurements with a simple ampere meter confirmed the insulating properties of the polyimide layer with 0.1 μA (lowest detectable, probably 0 μA). Current was detected in the mA range when a voltage of 0 to even 60 V was applied at the gate (copper plate). This measurement, the gold sputtered (section 8.4) top-contacts were tested as well. Both contacts showed high conductivity. The short circuit was thought to be caused by the edge effect after dip-coating. At the edges of the flat copper plate, the polyimide layer is thinner than in the middle of the plate. Therefore, if the contacts connect this area, it is very likely that the insulation is insufficient at these points).

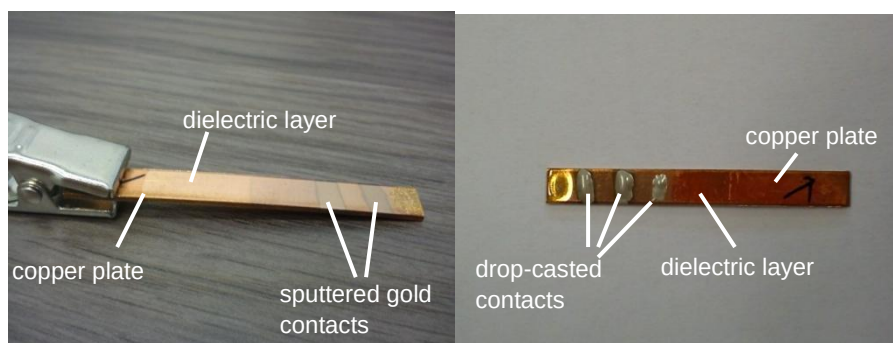


Figure 124 Gold sputtered electrodes (left) and contacts applied by drop-casting of silver conductive screen printing ink covering the edges of the sample (right)

In further experiments, silver conductive screen printing ink was used to place drop-casted top-contacts. Again, the assumption was confirmed that the edge effect influenced short circuiting, if the drop-casted contacts covered the edges of the sample. Consequently, drop-casted ink was carefully placed into the middle section of the plate avoiding the area around the edges of the sample.

Repeatedly in the subsequent experiment, short circuits were also occurred when silver conductive screen printing ink was applied by drop-casting in the middle section of the plate. It was thought that the crocodile clamps might have damaged the polyimide layer. For the subsequent measurement, small copper wires were pressed into the ink before drying. This meant that the copper wires could be

connected using crocodile clamps without potential damage to the polyimide layer.

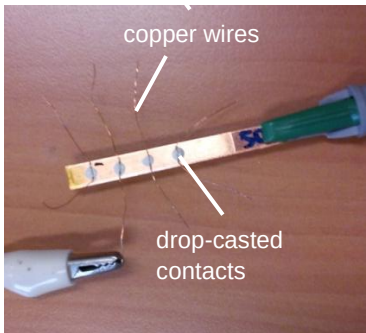


Figure 125 Sample with silver conductive screen printing ink and copper wires connected to crocodile clamps

The copper wires pressed into the ink were not very stable as they often broke, frequently interrupting the contact. The described approach was, given the circumstances, the best solution for establishing contact with the sample. Leak current measurements, as described in chapter 9.4 (p.207), were conducted with this setup (see chapter 6.3, p. 149) until it was decided that the measurements it was best to continue with the targeted substrate, the semi-conductor, polyimide and copper coated polyester filament.

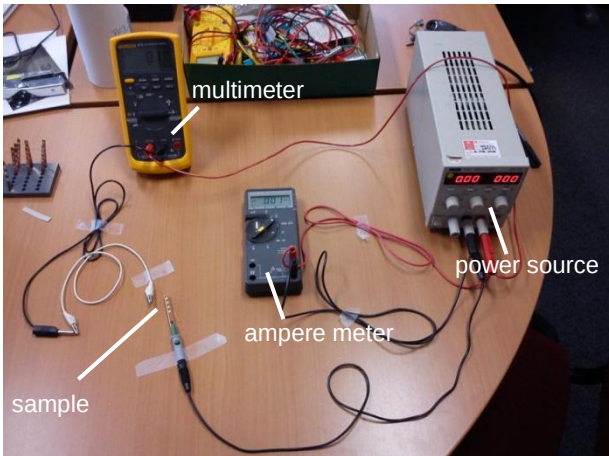


Figure 126 Resistance measurement setup including a power source, an ampere meter to control voltage at the source and a multimeter to detect current

As the filament with a diameter of 800 μm had a smaller surface and a curvature, other methods for contacting the filament had to be developed.

After conducting the first resistance measurements with the setup as described above (see previous paragraph 9.6, p. 220), a current measuring setup with higher sensitivity (up to pA) was used to conduct subsequent measurements. This new setup has the advantage of measuring at a lower speed and therefore produced more accurate data. Polyimide-coated copper plates were connected to the setup with crocodile clamps. Between the voltage steps, a voltage of 0 V was applied as well as at the start and beginning of each measurement. In addition voltage was applied with increasing value but alternating sign from 0 to +5 respectively -5. The current was measured over time. Each of the 21 voltage steps was set to 1000 seconds.

All contacts were tested for short circuits with a multimeter before being placed into the measuring setup. In addition, a quick test to choose the measuring range e.g. pA or nA was conducted before the actual measurement was started.

To confirm electrical properties leak current measurements at the Electronics and Information Systems department (ELIS) have been conducted with a sensitive current measuring setup. Initially the insulating properties of the dielectric layer were assessed when applied on a copper plate with a size of 5 mm x 50 mm. Conductive silver screen printing ink was used to apply the contacts by drop casting. The coating was done at a variety of speeds 50, 75 and 100 mm/min. Measurements were taken at pA level ($= 10^{-12}$ A). The insulating properties of the dielectric layer over time (1000 seconds/step) was investigated and different voltage levels applied at the gate layer which was the raw copper plate. The voltage steps applied were alternating with 0 V in steps of 1 V. also alternating negative and positive voltages were applied (0 / 0 / +1 / 0 / -1 / 0 / +2 / 0 / -2 / 0 / ... / 0 / +5 / 0 / -5 / 0). One measurement lasted about 6 h. The data points of the final 20 seconds in each measurement were

collected and an average was calculated ready for analysis. The averages were then used to establish the current-voltage (I/V) curve per sample. 11 samples have been analysed at three different dip-coating speeds (50 mm/min, 75 mm/min, 100 mm/min) representing three different layer thickness', as shown in Figure 127.

Based on the trend-lines, as shown in Figure 127 it is once again confirmed that the dielectric layer behaves like a resistor. The linearity of the IV curves, showed the electrical behaviour of an insulator i.e. being a linear resistor. At increased voltage and increase current was detected in the range of max $-1\text{E-}10$ to $+1\text{E-}10$. It was confirmed that the layer applied at all coating speeds was insulating. The higher the coating speed the higher was the insulation as the layer was supposed to become thicker. The deposited dielectric layer therefore is sufficiently insulating for the application as insulating layer within the transistor architecture.

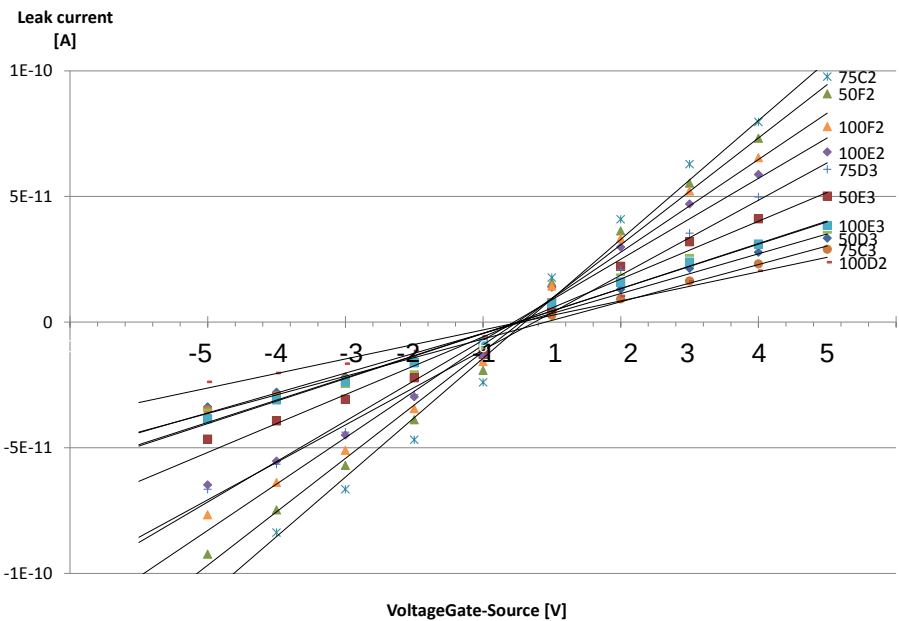


Figure 127 I/V curve for samples dip-coated in polyimide at 50, 75 and 100 mm/min

i) Conclusions for characterization of the polyimide layer in view of subsequent application of semi-conductor layer

In conclusion, it can be said that all layers are insulating when applied on the copper plate, although the values for resistance were spread over wide range. Therefore reliability was questioned (see: Figure 128). Variations might be caused by varying contact electrode dimensions, distribution of ink particles in the ink applied as electrode and/or the uneven distribution in the layer's thickness or the quality of the polyimide layer.

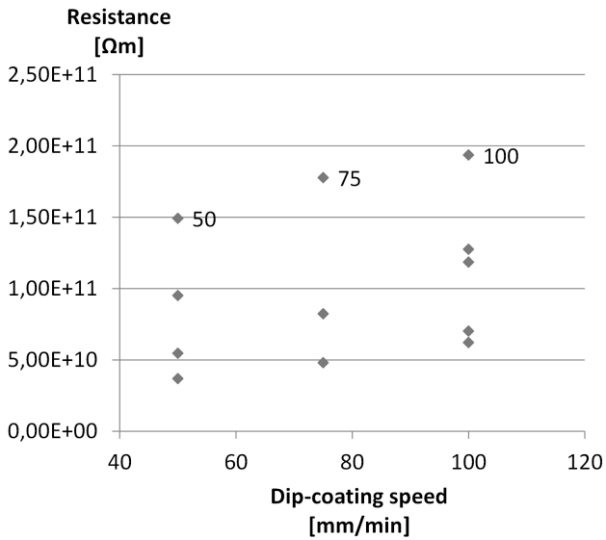


Figure 128 Average resistance

ii) Practical remarks for the electrical characterization of the polyimide layer in view of subsequent application of semi-conductor layer

When investigating the right approach in depositing the contact electrodes (chapter 8) a suitable method for electrical characterization had to be developed as well. The following experiment describes the challenges of contacting the deposited top electrodes.

Starting with the polyimide-coated copper plate onto which aluminium top contacts deposited by thermal evaporation, the first measurement showed high conductivity. The contact probes (tungsten needles)

pierced through the dielectric layer. This created a closed circuit by contacting the copper plate instead of the surface of the dielectric layer. The tip of the tungsten needle had a diameter of 5 - 15 μm . To overcome this issue, small drops of a two component conductive glue (conductive epoxy, CW2400, chemtronics) were added onto the contacts to increase the thickness of the top-contacts. In addition, the tungsten needle filed down with sand paper making the tip somewhat blunter. With this configuration, it still proved to be impossible to establish contact despite the application of liquid glue. Only after hardening the glue on a hot plate for 10 min at 100°C, and for additional 5 minutes at 150°C could the measurement proceed. The final figuration is shown in Figure 129.

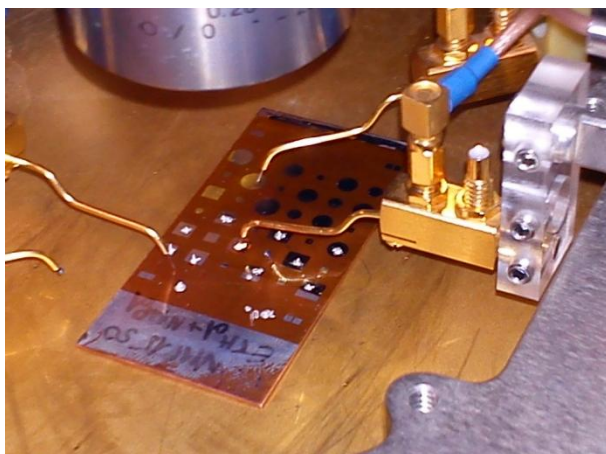


Figure 129 Probe station with polyimide-coated copper plate equipped with top-contacts by evaporation and conductive glue to increase thickness of the electrode

9.8. Effect of variation in pre-treatment of the substrate

In general, dip-coating requires good wetting properties of the substrate's surface. Tests have been conducted on flat copper foil [97]. To test the effect of a variety of pre-treatments, the surface was treated with different substances: distilled water, oxidation with hydrogen peroxide, chloroform, and methanol. Both visual inspection and analysis under optical microscope showed that best results without damaging the copper layer could be achieved when using

methanol. This pre-treatment resulted in a decrease of the contact angle from 45° to 20° on copper foil with solution from PI/DMF 7w% [97]. During subsequent experiments, if the copper (coated) substrates were stored for a longer time before the polyimide dip-coating, they were treated with a solution of citric acid. In addition, the copper coated PES filaments were pre-treated with methanol for two minutes before dip-coating, to remove dirt particles and improve the contact angle. To avoid any water contamination, the samples were also dipped into DMF and dried. There was a strong probability that the surface energy of the substrate might be influenced by absorption of liquids, too [142]. However, SEM analysis did not show any significant differences in morphology of the polyimide layer itself (see Figure 130).

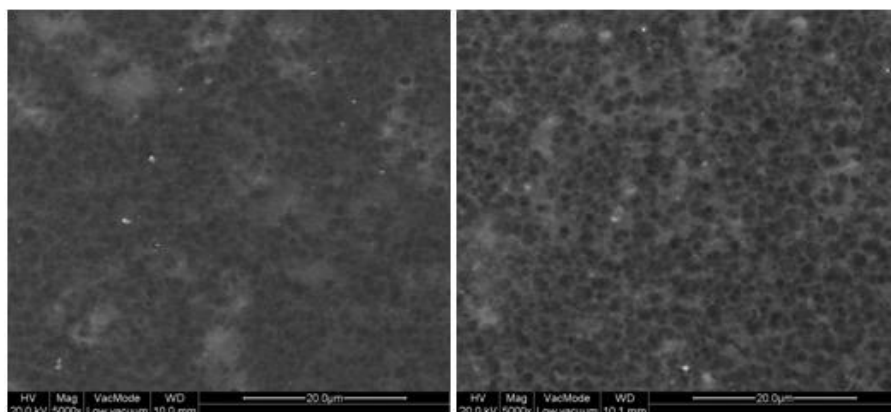


Figure 130 SEM images: DMF 15w% 25 mm/min without (left) and with methanol pre-treatment (right), the scale bar indicates 20 μm

As methanol is a hazardous chemical, it was substituted by ethanol in the pre-treatment. It has been investigated whether this cleaning solvent would affect the layer. Visual inspection of the sample did not reveal any influence regarding the substitution of the cleaning solvent. This was confirmed by measuring the contact angle of the polyimide solution on pre-treated copper plates. The measurement has been conducted on a DSA-30 Krüss setup for measuring contact angle and surface tension, as mentioned in chapter 6, p. 133. After pre-treating the substrate with methanol for two minutes and subsequently dipping into the dip-coating solvent NMP, the angle was reduced from 39.5°

to 32.7° by substituting methanol with ethanol. The setup is shown in Figure 131.

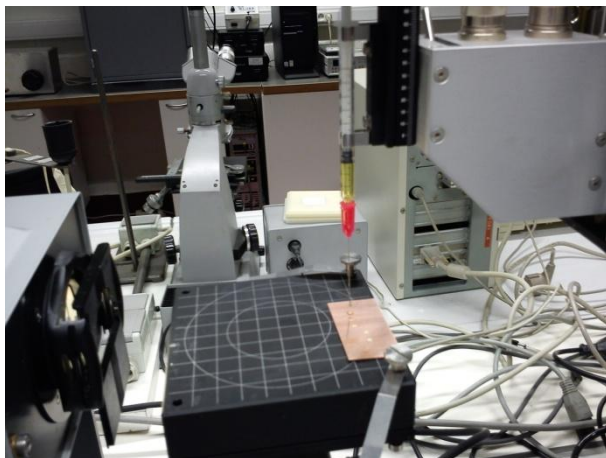


Figure 131 Drop-casting of polyimide solution for measuring contact angle and surface tension

The total surface tension of the ink can be extracted from a pendant drop measurement. The calculated surface tension was increased from 58 mN m⁻¹ with methanol to 94.3 mN m⁻¹ when ethanol was used.

Another observation was made with regard to the handling of the substrate after being pre-treated. Initially, the substrate was directly coated after the pre-treatment. Since the second solvent in the pre-treatment was NMP, the substrate was not dried before dip-coating in polyimide. A disruption of the layer on the top of the coating was observed resulting in an uneven coating in this area (Figure 132).



Figure 132 Disrupted polyimide layer morphology on copper plate

At the top of the sample, the layer was thinnest when compared to other part of the same sample, because the still liquid solution on the sample after withdrawal from dip-coating flowed to the lowest point of the sample. This caused the formation of a thicker part at the lowest point of the sample but also a thinner part on the very top of the sample. If the sample was still wet from being dipped in to NMP from pre-treatment, the solution at the point might have been diluted and consequently might have caused the disruption. This negative result was avoided by drying the substrates after pre-treatment overnight in at 60°C the layer was evenly coated even at the top of the sample.

It should be emphasised, that measuring contact angles on a filament is far more challenging than on flat plates because of the surface curvature. Once the droplet has been deposited onto the surface of the sample, gravity causes it to move from top to the bottom, depending on the position of the filament (see paragraph 8.5). In addition, the measured angle on the surface with curvature will yield valid comparison to flat substrates.

Measuring the surface tension on a cylindrical substrate with the Wilhelmy plate setup (Figure 133) might be a solution. The setup enables measuring the forces on the substrate which derive from the solution sticking to the substrate at withdrawal.

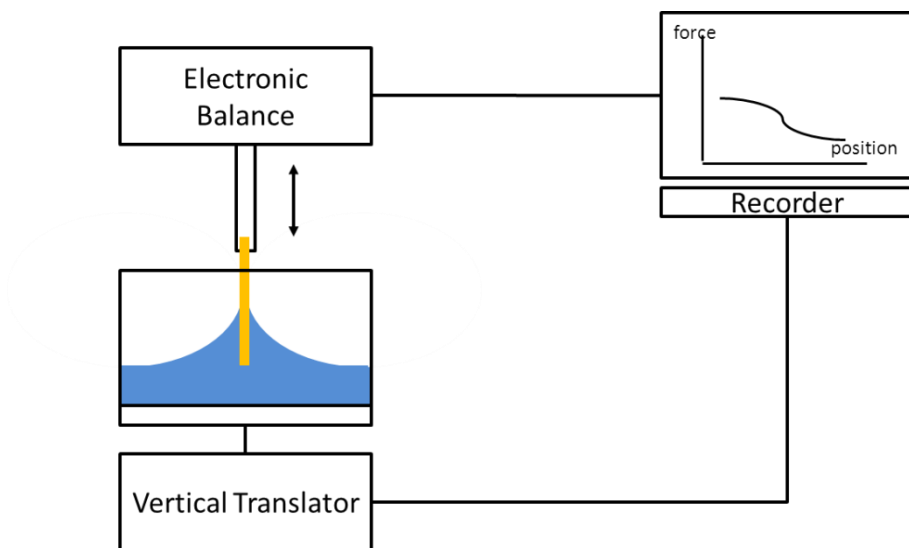


Figure 133 Scheme of Wilhelmy plate setup

9.9. Effect of drying of the dip-coated layer in solvent rich environment

Since humidity was detected as one of the influencing factors for the quality of the dielectric layer, an attempt was made to exclude humidity completely during drying. Experiments were conducted on a polyimide coated copper plate.

- i) Drying in dry conditions at ambient temperature in solvent rich environment

To further decrease the appearance of cavities the coated samples were dried in dry and solvent rich atmosphere. The experiments were completed at room temperature in a desiccator in which a dehydrating agent, phosphorus pentoxide (P_2O_5), and a solvent (ethanol) were placed. After 17 h the polyimide layer on the substrate was still wet, but had a transparent and even appearance. Humidity apparently was not affecting the layer in this setup. After 43 h still the layer was not completely dry and the experiment was continued. Following, after 65 h the layer did still not dry but now the layer looked dull and strangely uneven. After approximately one week of drying, the experiment was discontinued. By this time, the layer was dry apart from the bottom

end where the layer was thicker. After taking the sample out of the solvent rich environment, the wet part at the bottom of the sample immediately started phase separation when reacting with the humidity in the air. In addition, a sort of sweating in the lower part of the substrate was observed (Figure 134).



Figure 134 Test on polyimide layer when drying in solvent rich environment

It was concluded that drying the polyimide dip-coated layer in dry dehydrating and solvent rich atmosphere was inefficient. Furthermore, the bottom part of the deposited layer did not dry after one week, overall increased drying time of the layer was perceived as deemed to excessive, therefore unsuitable for application in the final production process.

ii) Drying in dry conditions at 60°C in vacuum

Another attempt to eliminate humidity during drying was made by placing the coated substrates into a vacuum oven at 60°C for 24 h.

After drying, the layer showed defects in some parts of the sample and it seemed that the polyimide did not adhere to the substrate in some parts. This effect was visible on the front and on the back of the copper plate, therefore the defect could not have been confined to

only in one spot, but was a defect, which was distributed over multiple areas of the same sample (see: Figure 135).



Figure 135 Polyimide layer after drying in vacuum at 60°C for 24 h

iii) Drying in dry conditions at 60°C at <5% humidity

It was decided to return to the initially applied drying procedure, that was, completion of drying in the oven at 60°C for a duration of 24 h. Until now, it was always assumed that 24 h would be sufficient to dry the layer, but the assumption had not been previously tested. This study has succeeded in establishing the exact drying time for the dip-coated polyimide layer.

Therefore, the sample was weighted every hour for the first 12 h of the drying time after dip-coating, then it was weighted again after 24 h and it had been taken out of the oven. The difference in weight of the freshly coated sample and the sample with a dried layer was 0.3541 mg. The final weight of the sample had been already achieved after a drying period of 7 h at 60°C. This weight included the entire sample, which is including drying of the lower part of the sample where the layer thickness increased. If the lower and upper parts in the sample were to be excluded from weighing, because they did not represent the actual layer thickness, the drying time would have been much shorter. Because of practical considerations the samples were now dried “overnight” (12 h instead of drying 24 h). It meant that the required drying time was reached and the application of the semiconductor layer was able to start early the following day.

It was concluded that drying procedure for the polyimide dip-coated layer is optimal when completed in low humidity (<5%) in the oven at 6°C within a minimum of 7 h.

9.10. Storage during drying of polyimide coated substrates

Immediately after dip-coating and for drying, the coated samples should be kept in an upright position and stay in the same direction as during dip-coating. Arfsten *et al.* point out that the angle of withdrawal and therefore during drying effects the coating in its evenness and thickness [103]. Several storage solutions have been evaluated.

- i) First generation sample holder used in drying process of just dip-coated layer

Initially the work was carried out using clamps. At this point the substrate was a 1 mm thick copper plate which could be held by a metal office clamp. When using filaments the pressure of this clip was too low and filaments easily slipped out of the clamps. Metal curtain clips sourced from IKEA exerted greater pressure. The clips were then hung from a glass rod and the rod placed across a beaker. This set-up allowed the samples to hang freely inside the beaker (Figure 136). The beaker served as protection from any air turbulence in the environment. However, the rod kept rolling of the beaker and the clips were liable to slide off the glass rod.



Figure 136 First generation sample holder

It was not possible to use the storage system used for the copper coated samples (Figure 137). In this holder the samples could dry in upright but only in opposite direction.

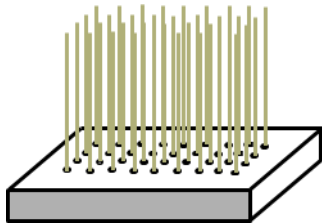


Figure 137 PVC holder used for storage of copper coated filaments

Storing the still liquid layer in holders shown above (Figure 137) would have let it solidify inside the holder towards the bottom end of the sample. In addition, the layer itself would have been affected when rotating the filament. It would have been highly unlikely to remove the sample without damaging it. Therefore, only once the layer was completely dry could the samples be stored in this holder.

- ii) Second generation sample holder used in drying process of just dip-coated layer

A new storage system was developed, this time the set-up still included the beaker but with the new construction included a lid, which prevented sliding of the clamps (Figure 138). Furthermore, the still liquid layers could dry without any air turbulence, which was thought to be generated when the oven was repeatedly opened and shut. In the previous configuration, all samples attached onto the glass rod had to be removed when extracting one sample.

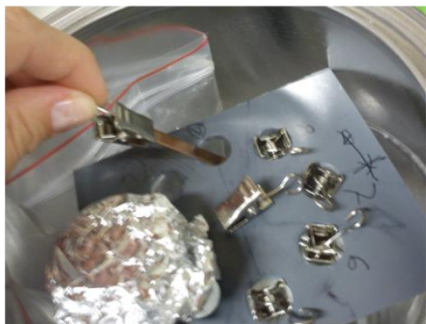


Figure 138 Second generation sample holder

Now transport of the samples was more secure but still handling was not optimal. It sometimes it was impossible to place the sample without touching the PVC lid while placing the sample into the lid, or while working in the dark with the semi-conductor. Attempting to quickly place the samples into the holder in the oven without letting humidity in, was similar to playing the game “the hot wire”.

- iii) Third generation sample holder used in drying process freshly of dip-coated layer

Figure 139 shows the final sample holder which made placing of the filaments on the clamps relatively easy. The holder was made imitating a glass holder as shown in Figure 139. The third generation sample holder was also used for drying and storage of the semi-conductor coatings.

In the case of the semi-conductor coating, it was important that the holder could be placed into an additional box so that the samples could be kept in the dark after drying in the oven.



Figure 139 Third generation sample holder (left) following the example of a glass holder (right)

After final characterization of the samples, the final storage solution was keeping the samples in small plastic tubes with a lid. This excluded humidity which might have an effect on the semi-conductive layer.

9.11. Effect of bending during dip-coating in TIPS-pentacene

It has been observed that cracks in the polyimide layer can be generated as shown in Figure 140, if a sample during dip-coating in the semi-conductor touches the ground of the vessel and is eventually bent.

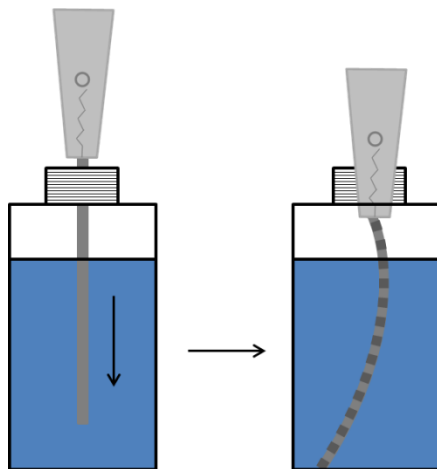


Figure 140 Sample bending during dip-coating process

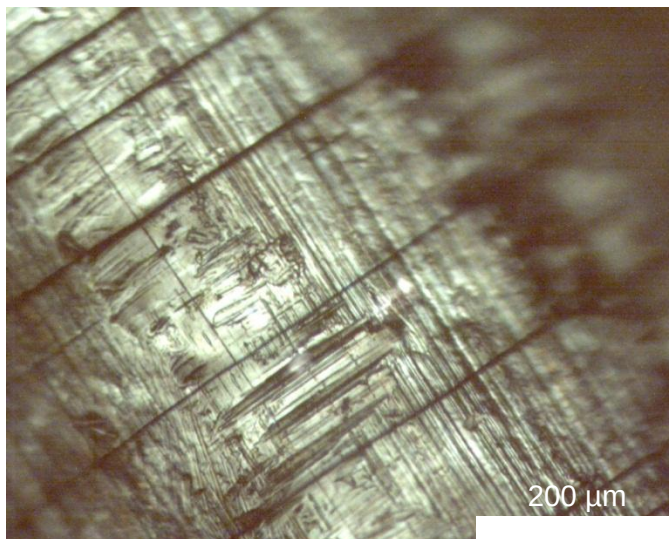


Figure 141 Sample was bent during dip-coating, cracks have been formed perpendicular to fibre direction

To avoid these cracks appearing in the polyimide layer, it was essential that great care was taken in dipping the sample avoiding contact with the ground of the container.

It was therefore imperative to measure the height of the solution inside the vessel before dip-coating. TIPS-pentacene dip-coating was completed in the dark. This impaired vision and only left the dip-coating software to indicate the actual dip-coating depth. Before dipping the substrate into the solution, it needed navigation to the surface of the solution, on the screen, this position was marked with $Y=0$, enabling the dip-coating process to proceed. The sample was extracted once the maximum dip-coating depth was reached [cm] i.e. until it was “safe” to dip without touching the ground of the vessel.

Bending of the sample was also a risk during polyimide dip-coating, whereas here the dip-coating was completed in the ambient conditions and the dip-coating solution was transparent. As cracks develop in the polyimide layer during TIPS-pentacene dip-coating when the ground of the vessel was touched, this also posed a risk during the polyimide coating this could have influenced the copper layer underneath.

With current material configuration, including polyimide as dielectric layer, the transistor could not be bent as the different layers could break. Therefore the current material configuration is likely to fail in electrical characterization i.e. short circuits could be caused.

Evaluating the experiments described above one is able to draw the conclusion that as at this point in time the transistor is not bendable, the application in intelligent clothing does not seem feasible. In any case, there still is high potential in other application areas. As long as stiff constructions are targeted which will not be bend e.g. in textiles for building and construction or composites, the current filament transistor architecture could be applied. In some composites the filament is only placed into the composite structure instead of being woven or knitted into a textile structure beforehand. This reduces bending and therefore, also this study's transistor filament can be used in real applications. Furthermore, once the function of a transistor is achieved, a very good foundation is laid for continuing research using another dielectric substitute.

9.12. Additional remarks - use of the solvent NMP

According to Mikhailenko *et al.* [140] it is very difficult to remove the solvent NMP completely from the substrate, because of its high boiling point of 202°C. The solvent stays in the polyimide membrane. If the application of this transistor is envisaging to be used in clothing or to be worn close to the body i.e. as sensor, the use of NMP in the transistor is not recommended, because of its reproductive toxicity. [149].

9.13. Evaluation of the polyimide dielectric layer

Variations in the dip-coating process were made to improve the layer morphologically. Evaluation criteria for the layer were maximum insulating properties at minimum thickness, and minimum layer roughness. To achieve the improvement, the choice of solvent and solution concentration was assessed, and the dip-coating speed adjusted. Furthermore, the pre-treatment of the substrate and drying behaviour of the layer were investigated.

1) Minimum layer thickness at maximum insulating properties

The following factors influenced the layer thickness and therefore, the electrical insulating properties of the layer:

- choice of solvent
- solvent concentration
- dip-coating withdrawal speed
- drying conditions

Best results were achieved with a polyimide NMP dip-coating solution of 15w% and a dip-coating speed of 50 mm/min, resulting in a layer thickness of 600 nm and good insulating properties (threshold $< 10^{10}$ Ω cm). Avoiding phase separation and water penetration, drying in dry conditions ($< 5\%$ humidity) for a minimum of 7 h was leading to optimal results. This way, roughness and consequently thickness of the layer was decreased.

2) Minimum layer roughness

Layer roughness was mainly influenced by absorbing humidity in the layer when in liquid conditions. The absorption water led to the

formation of cavities increasing the thickness and roughness of the layer. The absorption of water was influenced by the choice of solvent with regard to its boiling point as well as the ambient conditions during drying of the dielectric layer.

As pointed out above, with deposition of polyimide solved in NMP a roughness of 34 ± 5 nm could be achieved. As mentioned in 1) the roughness also was decreased in the right drying conditions.

3) Appropriate mechanical properties

During dip-coating, it has been observed that the dried polyimide layer is sensitive to bending. Cracks appeared in the substrate, leading to an increased number of closed circuits during electrical characterization of the polyimide layer.

Therefore, the dip-coated polyimide layer can only be used in those application where bending of the substrate is avoided. In this respect, composites would be one of the potential application areas.

10

Semi-conductive layer

The aim of Chapter 10 is to provide a brief introduction into the field of in(organic) semi-conductor materials. It explores the justification for choice of semi-conductor (see: the experimental part of this chapter below, p. 257). The experimental part, elaborates the deposition of the organic semi-conductor 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) by dip-coating. Furthermore, it highlights the challenges which have been encountered during completion of the coating processes as well as during subsequent characterization.

10.1. Introduction

The following sections discuss the rationale for choosing a specific semi-conductor from a range of inorganic and organic material options. In addition particular difficulties are identified as well as actions taken to achieve the most effective solution will be evaluated.

i) Requirements

As indicated in chapter 6 (p. 133), a semi-conductor material had to be chosen for application as active layer in the fibrous organic field effect transistor (OFET). A variety of factors had to be considered for making this choice. The best match of material properties and process conditions which also suited the application on the fibrous substrate had to be identified. A list of requirements in view of material properties and process conditions is given below.

Material property requirements:

- ☐ forms thin films
- ☐ flexible when applied as film
- ☐ low-sensitivity when processed in the textile industry environment and long-term stability of the deposited layer
- ☐ compatible with the underlying polyimide layer
- ☐ high charge mobility, good on-off in deposited layer

Processes condition requirements:

- ☐ low temperature deposition
- ☐ up-scalable production
- ☐ inexpensive (solution processing) [63]

ii) Semi-conductors

A variety of materials for application as active layer were chosen for their potential use in the fibrous organic field effect transistor.

a) Inorganic materials

The primary choice in micro-electronic processing with regards to the choice of material is (inorganic) amorphous silicon (a-Si).

The advantages when using silicon are, as follows:

- ☐ The material is commonly applied in industry, highly developed and optimized. Processes are proven and readily available.
- ☐ Amorphous silicon has a high field effect mobility and yield, typically ranging from 0.1 to 1 cm²/V.s.

The application on the fibrous substrate is the focus of this work. Based on the disadvantages, as listed below, silicon is not an appropriate match for the application:

- ☐ Silicon is not compatible with textile processing due to the application of high temperatures in production and substrate-type compatibility.
- ☐ Its rigidity after film formation does not comply with the application of flexible substrates such as filaments.

b) Organic semi-conductors

As pointed out in chapter 6 (p. 133), semi-conductors do either have a high electron affinity (n-type) or a low ionization potential (p-type). The p-type semi-conductors show better stability in air and a relative high carrier charge mobility than their n-type opposites. N-type semi-conductors show a decrease in stability during operation and in general show a lower mobility [91]. Consequently p-type organic semi-conductors are preferred for the application in the fibrous OFET.

There are two main groups within the field of organic semiconductors: small molecules and polymers. α -sexithiophene (α -6T) and pentacene do belong to the group of small molecules whereas polyacetylene, poly(3-hexylthiophene) (P3HT) and poly(thienylene vinylene) are polymers [46, 126]. The advantage of using polymers is that they are solution-processable.

The disadvantages are:

- a) they are prone to impurities,
- b) polymers have to be synthesized by polymerizing monomers.

This process is not completely controlled, because molecular weight is highly affected by the exact stoichiometry of the reacting monomers. Furthermore, in particular thiophenes do tend to oxidize. This increases their conductivity, which unavoidably also increases the off current in the layer [91]. The mobility achieved with polymers is usually lower than in small molecules due to poor molecular ordering and low crystallinity. One of the few semi-conductors with a relatively high mobility of $0.1 \text{ cm}^2/\text{V.s}$ is regioregular poly(3-hexylthiophene) (RR P3HT) [45, 48, 91].

c) Small molecule organic semi-conductors

Compared to polymers, small molecule semi-conductors such as pentacenes and anthradithiophene show better stability and controllability in processing and a higher mobility. Hence, they are preferred for application in the fibrous OFET. Even though pentacene is more stable in air than other organic semi-conductors [150], it is still prone to oxidation [151].

Pentacene is a small (organic) aromatic molecule including five benzene rings which conjugate into a π -system. Van der Waals forces cause the crystalline structure to develop. In the literature, it is reported that the crystal structure and morphology of the film strongly influences the charge carrier mobility. In this respect, influencing parameters are substrate morphology and surface roughness, temperature, pressure and material deposition rate [48, 96]. Films of Pentacene show a mobility of $1.5 \text{ cm}^2/\text{V.s}$ to $3 \text{ cm}^2/\text{V.s}$ [50, 96, 152] when deposited by thermal vacuum deposition. Experiments indicate a mobility of as high as $35 \text{ cm}^2/\text{V.s}$ in high purity single crystals of pentacene [50, 126].

Pentacene is almost not soluble at room temperature in organic solvents and is therefore mainly applied by vapour deposition conducted in vacuum [150]. This rather expensive deposition technique is not applicable for mass production in textile industry due to the nature of the substrate (continuous filament) [48, 51, 126, 150].

Even though the semi-conductor pentacene and its deposition techniques are expensive, pentacene is frequently researched because of its high performance as semi-conductive material. To

make the compound industrially available at lower costs as well as to be used with other deposition techniques, the material was further engineered to increase its solubility and performance [48, 52, 127].

d) Soluble organic small molecule semi-conductors

Increased solubility of the semi-conductor as described above is extending the range of applicable deposition techniques, such as printing, spin-coating, or dip-coating which enables processing at room temperature in non-vacuum conditions. Using the new range of deposition techniques increases the variety of substrate types available for use. This can lead to application on flexible substrate or even large area applications [50, 120, 152]. The application of large area electronics in particular will be interesting, if low cost production techniques can be used with the high performance small molecule [53]. Substitution of side groups can lead to increased solubility of the semi-conductor small molecule compound. For example, the small molecule 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) is based on the pentacene compound which is functionalized by the addition of side groups leading to increased solubility [50].

e) 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene)

Because of its high mobility this substituted small molecule shows high potential for industrial application and is therefore, intensively researched. Field effect mobility of the small molecule TIPS-pentacene was reported as high as $1.8 \text{ cm}^2/\text{V.s}$ [54, 151, 152]. Mobility or transport of charge carriers relates to the morphology of the material and the crystalline microstructure of the deposited film (highly conjugated π -systems). As cited above, the crystal orientation highly affects the overall performance of the semi-conductive layer. There are differences in the exact orientation of the molecule on the surface leading to better performance. As for organic semi-conductors like pentacene or phthalocyanines, molecules orientate with the molecule's axis as shown in Figure 142, with the shorter side perpendicular to the substrate's surface. In organic soluble semi-conductor poly(3-hexylthiophene) (P3HT), the molecule attaches

edge-on onto the surface of the underlying layer, i.e. with the long side of the molecule (Figure 142). In addition, the small molecules pentacene arranges itself in edge-to-face manner (Figure 143). Well-organized TIPS-pentacene layers can be detected in the XRD spectrum showing distinctive peaks at 5.36° at vertical intermolecular spacing of $16.8 \text{ \AA}$ [37, 54, 138]. Important in the synthesis of the compound is the material purity which is likely to have an effect on film crystallinity, material stability and film performance [53, 54].

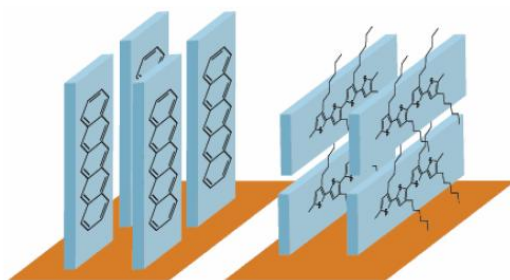


Figure 142 Molecular orientation of high-performance organic semiconductors pentacene (left) and P3HT (right) [91]

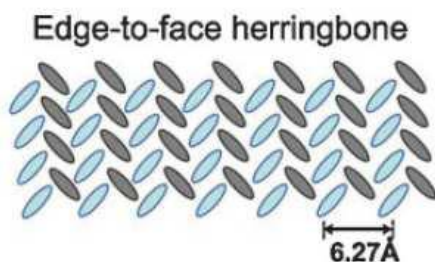


Figure 143 Pentacene crystals in edge-to face herringbone configuration [152]

f) Conclusion

Because of its high performance, solubility and accompanying deposition techniques with the advantage as low cost, low temperature and up-scalability, the p-type semi-conductor 6,13-bis(Triisopropylsilylethynyl) pentacene (TIPS-pentacene) will be applied as active layer in the fibrous OFET architecture. A further

advantage is, that the compound is commercially available for research at a reasonable price.

- iii) Difficulties to be resolved regarding the application of TIPS-pentacene as semi-conductive layer within the fibrous organic field effect transistor

As outlined in the previous sections (p. 252), the crystal orientation plays an important role in the performance of the active layer within the fibrous OFET. In order to influence this self-organization the intermolecular orientation in the crystalline film should be controlled [126, 152] by

- ☐ choice of solvent and solution concentration
- ☐ method and stability of solution
- ☐ solvent evaporation rate (drying) and post-deposition techniques
- ☐ deposition rate

to engineer the interface properties at adjacent layers i.e. interface between dielectric and semi-conductive layer.

10.2. Experimental

The following section will describe various experiments conducted while applying TIPS-pentacene as semi-conductive layer within the fibrous OFET architecture.

1) Choice of solvent

In literature, it was suggested that the solvent in the semi-conductor solution has an effect on the deposited layer and consequently, on the overall transistor performance [101, 137]. Hence, the effect of the solvent had to be investigated before layer deposition.

a) Properties for the choice of solvent

For finding the appropriate solvent for the TIPS-pentacene solution, two main properties have been considered. On the one hand, the

solvent should not affect the underlying polyimide layer. On the other hand, the solvent of choice should have a high boiling point ensuring slow solvent evaporation leaving the semi-conductor time to crystallise.

i. Solubility of polyimide in solvent for TIPS-pentacene solution

To ensure that the polyimide layer is not affected by the solvent in the semi-conductor solution, the solubility of polyimide was tested in a range of potential solvents for this TIPS-pentacene solution. A small amount of polyimide resin was placed into a vessel containing the respective solvent. Over time it was investigated if the resin dissolved.

In literature, aromatic solvents like toluene, tetralin, chlorobenzene, dichlorobenzene and xylene are commonly used in TIPS-pentacene solutions [101] (Figure 144).



Figure 144 Solubility test of polyimide in toluene, tetralin, chlorobenzene, dichlorobenzene and xylene

Polyimide quickly dissolved in chlorobenzene and dichlorobenzene. In toluene, tetralin and xylene, the resin did not dissolve, though polyimide started to swell in tetralin (Figure 145). To test the effect on copper, small pieces of a copper wire, a polyimide-coated copper wire (as purchased) and a copper-coated polyester filament were added into the solvent. Verified by optical microscopy, none of the solvents affected the copper visibly.



Figure 145 Polyimide resin shows to be insoluble in the solvents toluene, tetralin and xylene (from left to right)

- ii. Slow evaporation of solvent ensured by high-boiling point solvent

Based on the above, most promising solvents were toluene and xylene. Because xylene (138.37°C) has a higher boiling point than toluene (110°C), xylene was chosen for making the first TIPS-pentacene solution.

b) Preparation of the solution and observations

Initially, a stock solution of 40w% TIPS-pentacene in xylene was prepared. It then was diluted to 2w%. A colour change of the solution was evident within one day. TIPS-pentacene shows sensitivity to light and air even though the compound is reported as less sensitive as other organic substitutes (see chapter 10.1 c)). A new solution was prepared and stored in the dark with a lid on the vessel. This solution after few days also changed colour. Since complete exclusion of air was not an option for the application of the solution by dip-coating in ambient atmosphere, another possibility to decrease sensitivity of the solution to degradation was explored.

Firstly, literature suggests [151] that the semi-conductor is more sensitive to degradation in solution is due to possible inclusion of impurities leading to oxidation. Secondly, it was argued, that the sensitivity in xylene is higher than in toluene [151]. Coatings with the semi-conductor were generally conducted in inert atmospheres in a

glove box. Electrical characterization though was conducted in ambient conditions.



Figure 146 Solution of 2w% TIPS-pentacene in xylene degraded (left) and in toluene stored in vessel with argon gas (right)

Consequently, a solution of 2w% TIPS-pentacene in toluene was prepared and the vessel was kept in the dark at all times, also during dip-coating and transport. Argon gas was filled into the vessel to avoid trapping air and with it humidity. After applying this procedure, the solution kept its dark blue colour over time and hence, could be reused for consecutive dip-coating experiments. Figure 146 shows Solution of 2w% TIPS-pentacene in xylene degraded and in toluene stored in vessel with argon gas.

c) Investigation of degradation in TIPS-pentacene/toluene solution and deposited layer

Degradation of the solution could have a tremendous effect on the semi-conductive layer and therefore, had to be investigated. Even though the solution did not change in colour, it had to be verified that that the TIPS-pentacene/toluene solution did not degrade in between consecutive experiments.

i. Investigation of degradation by Raman Spectroscopy – TIPS-pentacene layer

Degradation of the semi-conductive layer was tested by using Raman spectroscopy (Perkin Elmer Spectrum GX NIR FT-Raman) on a

polyimide and TIPS-pentacene dip-coated copper plate. The sample was scanned in a range of 3500 to 200 cm^{-1} but results could not be collected since the sample itself (copper) was too dark. This test could have given information about the chemical composition of the TIPS-pentacene layer and its crystallinity.

ii. Investigation of degradation by Ultraviolet-visible spectrophotometry (UV/VIS) – TIPS-pentacene/toluene solution

Degradation within the semi-conductive solution (TIPS-pentacene/toluene) could be successfully detected by ultraviolet-visible spectrophotometry. An absorbance spectrum at five points in time was taken to detect degradation in the solution. In literature two distinctive peaks at around 600 and 650 nm were shown (Figure 147) [153], the peaks were confirmed during the experiment (Figure 148).

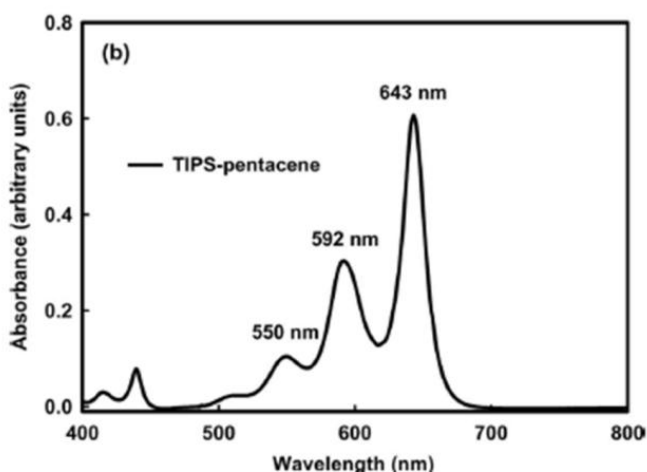


Figure 147 Absorbance spectra of TIPS-pentacene in chloroform [153]

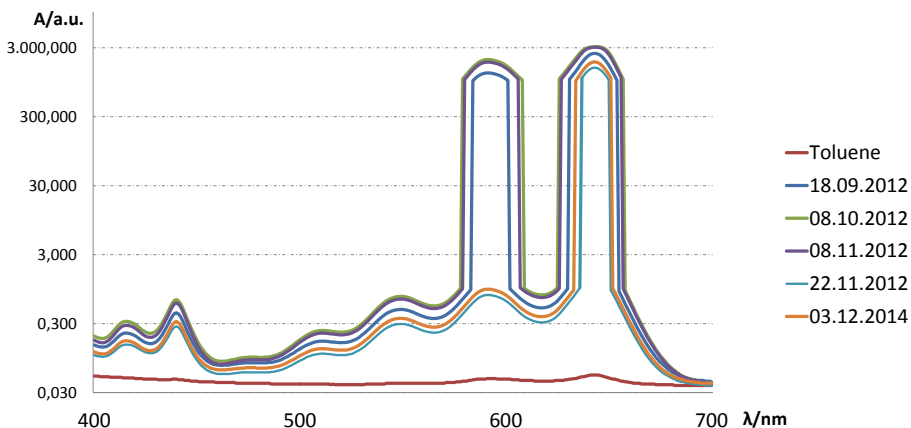


Figure 148 Absorbance spectra of TIPS-pentacene in Toluene

The peaks did not shift which would indicate degradation but only decreased in intensity. Using the new TIPS-pentacene/toluene solution, after eight days full colour change was recognized when being stored at ambient conditions in light and air [154].

d) Conclusion for choice of solvent

A range of solvents commonly used in the preparation of TIPS-pentacene solutions, was evaluated. Their effect on the polyimide layer, the solvent's boiling point and the semi-conductor's sensitivity to light and air in solution has been investigated. Additionally, degradation of the solution was enhanced by storing and handling the solution in the dark minimizing the influence of light, as well as, filling the vessel with inert gas (argon) to avoid the influence of air during storage. Choosing toluene as solvent, in combination with the method for storing and handling of the solution prevented degradation of the solution indicated by a constant dark blue colour and verified by ultraviolet-visible spectrophotometry (UV/VIS).

2) Choice of (choosing method of) analysis (technique) for detection and investigation of crystallinity in the TIPS-pentacene layer on polyimide and copper coated polyester filament

As shown in chapter 6, the performance of the transistor is, besides others, strongly defined by the crystallinity in the semi-conductive layer. Here, the amount of grains or crystals, grain size, their

distribution and amount are important and can be verified by changing the process conditions during dip-coating. The following sections, deal with the detection of the crystals. Once the best technique for the analysis is found, the process conditions are changed and their effect on the crystal growth is investigated.

a) Requirements for choice of analysis technique

Crystallinity in the deposited semi-conductive layer does affect the entire component performance, a technique had to be identified for detecting crystallinity in the TIPS-pentacene layer on the copper and polyimide coated polyester filament. Due to the sensitivity to degradation of the materials, this technique should be low in consumption of time, a non-contact and non-destructive technique. The latter leaves room to test the transistor electrically because the necessary top-electrodes for this analysis can be applied onto the unaffected semi-conductive layer.

b) Methods for detection and investigation of crystallinity

Two non-destructive, non-contact methods were already tested on the material in the previous section. In addition to these, optical microscopy with and without polarizer as well as XRD were tested for suitability for detecting the crystallinity of the semi-conductive layer after deposition by dip-coating. The following sections report on the evaluation of the methods as well as on the results detected by the respective method when rendering the deposition process.

i. Detection and investigation of crystallinity by optical microscopy

The TIPS-pentacene solution is dark blue in colour but when deposited as thin film transparent in colour and therefore invisible in common optical microscopy. Also the polyimide layer is transparent and therefore, cannot be used as reference to detect the TIPS-pentacene layer. Hence, by common optical microscopy crystals could not be detected.

Crystals are visible in polarized light, hence the microscope was equipped with a polariser making it possible to detect the crystals in the deposited layer.

On the flat substrates crystals were detected right after using the polarizer. As for the wire and filaments, substrates with surface with a curvature, no crystals were shown. This was exceptional because both, the flat and cylindrical substrates were dip-coated at the same speed and in the same solution.

It was found, that the positioning and alignment of the samples, as seen in X-ray analysis as described later-on in this chapter, had to be rendered to detect the crystals formed within the TIPS-pentacene layer. The filaments were, therefore, rotated to align them in parallel to the microscope's light beam. The filaments were rotated from being positioned perpendicular to beam direction (180° on a rotatable platform) to a parallel alignment in direction of the light beam (90° on rotatable platform). Crystals were highly visible when analysed in a 20° angle, from approximately 70° to 90° . The visibility changed with the rotation angle.

As for the substrates types only those with a diameter of 800 to 1000 μm could be analysed. Due to the small and curved surface area offered for analysis, the focus surface was too small to analyse the layer in terms of crystallisation.

At a magnification of 25x the highest quality microscopic pictures were taken regarding amount, distribution, size and shape of the crystals.

Microscopy is a fast, non-destructive and almost non-contact technique consequently, all samples were analysed using polarized light microscopy to assess their crystallinity. Not only were the existence of the crystals detected, but also their amount, shape and distribution along the filament axis. Using optical microscopy, only a qualitative assessment was possible, therefore alternative quantitative methods were investigated for their suitability.

ii. Detection and investigation of crystallinity by Raman spectroscopy

It was not feasible to use Raman spectroscopy for the analysis of the experiment undertaken on the copper plate, due to the material's dark colour. The polyester filament was copper coated. Furthermore, in this instant the dark colour prevented the analysis by Raman spectroscopy.

iii. Detection and investigation of crystallinity by UV/VIS

As the detection of degradation in the TIPS-pentacene solution was successful, the layer after solidification was investigated by UV/VIS. The reflectance spectrum of the TIPS-pentacene layer on the copper plate was compared to results found in literature (Figure 149 and Figure 150). Even if not completely confirming the results, within the received, spectrum the distinctive peak at 350-550 nm was detected confirming that the transparent semiconductor was deposited onto the polyimide coated copper plate.

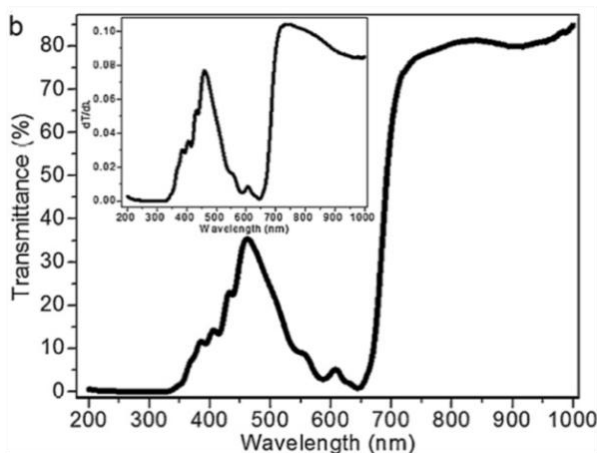


Figure 149 UV/VIS spectra reflectance [153]

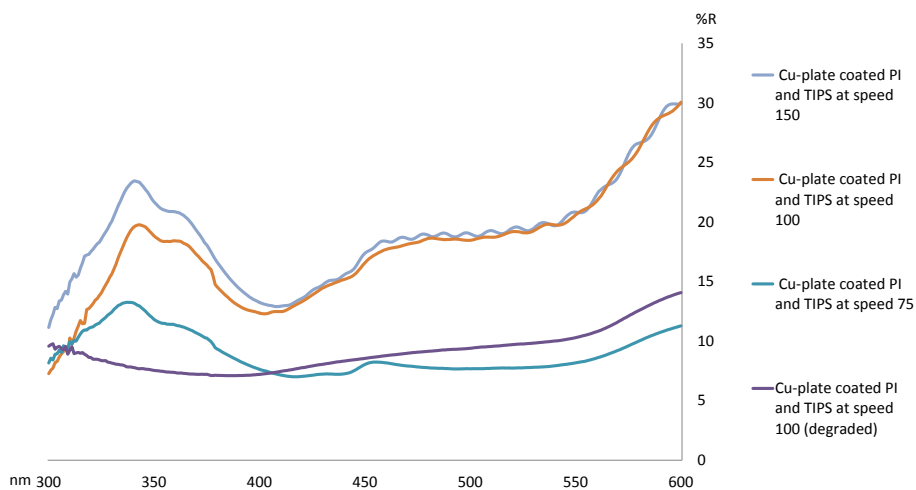


Figure 150 Reflectance spectra measured of TIPS-pentacene layer on a variety of substrates

Taking the spectrum of TIPS-pentacene coated copper-coated polyester filaments did not lead to any results. The available surface area for measuring on the filament was too small for gaining sufficiently reliable data fit for interpretation. Hence, since the techniques were not applicable to the substrate type, another method had to be identified for analysing the deposited semi-conductive layer quantitatively.

iv. Analysis by x-ray diffraction spectroscopy (XRD)

X-ray diffraction spectroscopy was applied to detect crystallinity in the TIPS-pentacene semi-conductor layer. Initial analysis comprised measurement of the plastic sample holder, the polyester filament, a copper plate and a polyimide and TIPS-pentacene coated copper plate. Due to its molecular spacing, TIPS-pentacene has a very distinctive peak at 5.4° if crystalline [155]. The graph in Figure 151 shows the XRD spectra of a TIPS-pentacene film deposited through three different process techniques, namely spin-coating, dip-coating and drop-casting.

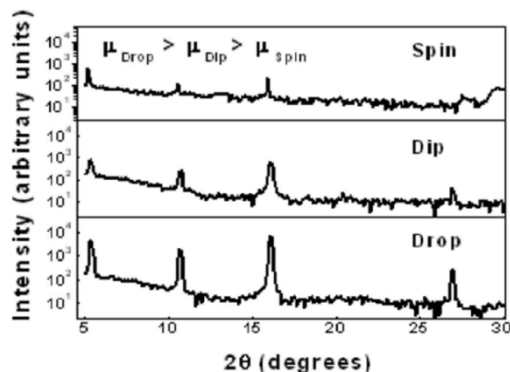


Figure 151 XRD graphs of TIPS-pentacene deposited by different process techniques: spin-coating, dip-coating and drop-casting [155]

A diffractogram of a variety of polyesters is shown in Figure 152. All polyesters in this diffractogram show a wide peak starting at around 10° [38]. First scans of the deposited layer showed that this wide peak at 12° to 28° in the scan resulting from the polyester filament confirming the results cited in the literature [155]. This bump would cover a wide angle from the scan leaving only the distinctive peak at 5.4° for detection of the crystallinity of TIPS-pentacene. Copper shows peaks at around 45° and 51°, and therefore, were also less import.

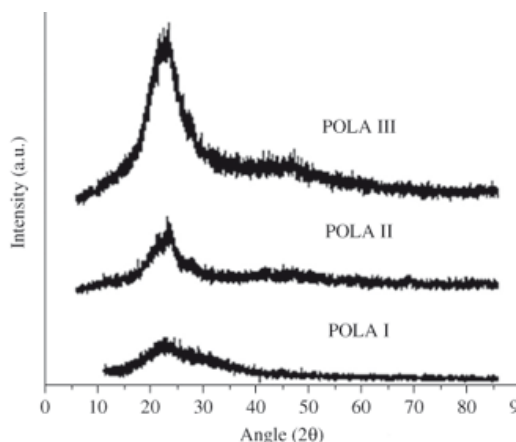


Figure 152 X-ray diffractogram of three types of polyester [38]

Polyimide as deposited before the TIPS-pentacene layer shows a similar behaviour as shown in Figure 153. A wide peak or humps is shown in the range of 10° to 35° .

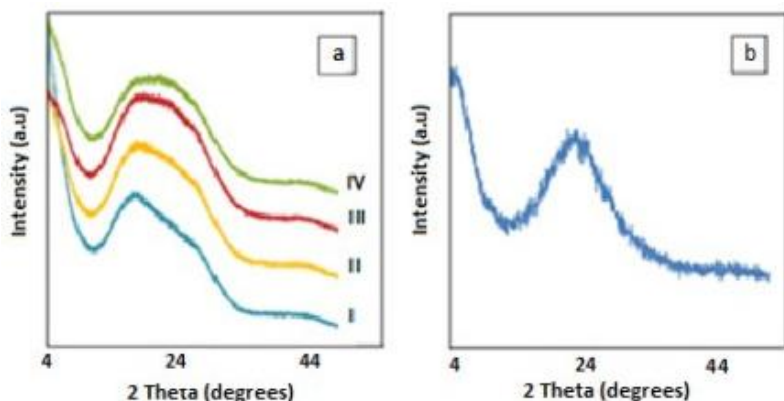


Figure 153 XRD patterns the polyimide/SiO₂ composite films at different concentrations (I–IV) of tetra-ethyl-ortho-silicate (TEOS) (left), and SiO₂ particles (right)[40]

1) Analysis of TIPS-pentacene layer deposited on polyimide-coated copper plate

Figure 154 shows the spectrum of a copper plate coated with polyimide and TIPS-pentacene and scanned in the range from 3° to 80° . The TIPS-pentacene layer was deposited at a speed of 100 mm/min. Peaks indicating crystallinity of the TIPS-pentacene layer were detected at 5.41° , 10.853° and 16.237° . The bump pertaining to the polyimide layer is visible starting from about 7° . In this case, it is likely that the peaks of TIPS-pentacene at 10.853° and 16.237° are visible since the polyimide layer is not very thick, hence is less influential. When working with the polyester filament in the following sections, the very same range will not show the peaks indicated above because polyester with a wide peak in the similar range as polyimide will obscure the TIPS-pentacene peaks. As mentioned, therefore, only the peak at 5.4° indicating TIPS-pentacene crystallinity will be of importance.

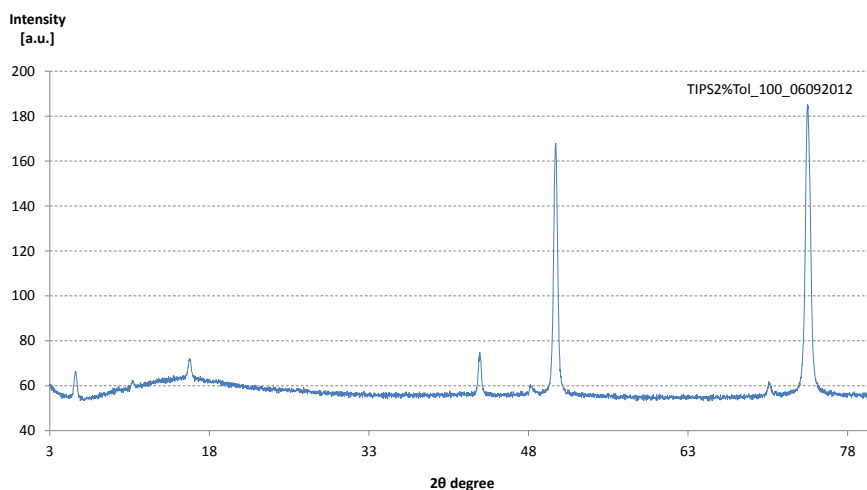


Figure 154 XRD of TIPS-pentacene layer on a copper plate without background subtraction

To detect degradation, after one and after five days, the measurement was conducted on exactly the same samples when stored in a closed box avoiding light. The peaks were still visible even in a quick scan of a reduced scan rate from 2°/min to 0.6°/min. The peak's intensity only slightly decreased which might be due to the position of measurement on the sample.

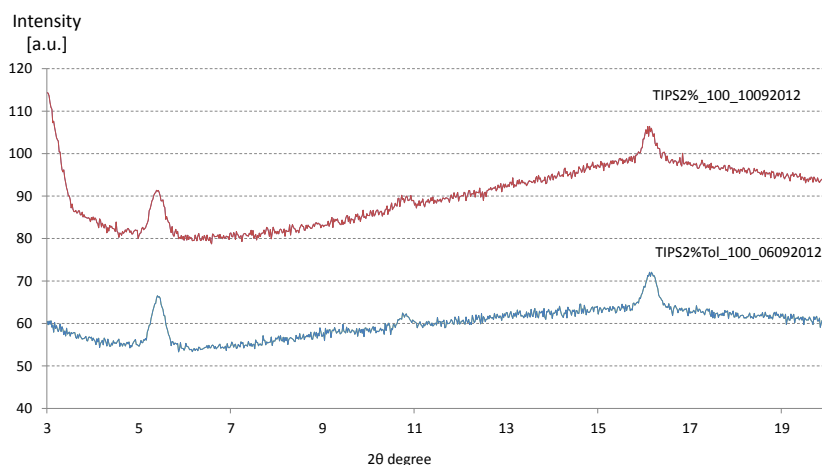


Figure 155 XRD scan of a TIPS-pentacene layer on a polyimide dip-coated copper plate one day after production and five days after production

The measurement confirmed that one is able to detect crystallinity in the deposited TIPS-pentacene layer on the polyimide coated copper plate. The following experiments, intended to test, if the detection of this crystallinity in the TIPS-pentacene layer on a polyimide coated and copper coated polyester filament was also possible.

1) Analysis of TIPS-pentacene layer deposited on polyimide- and copper coated polyester filament

When conducting the very same measurement (as described above) on the TIPS-pentacene layer which was deposited on a polyimide and copper coated polyester filament a different diffractogram as on the copper plate was obtained (Figure 156).

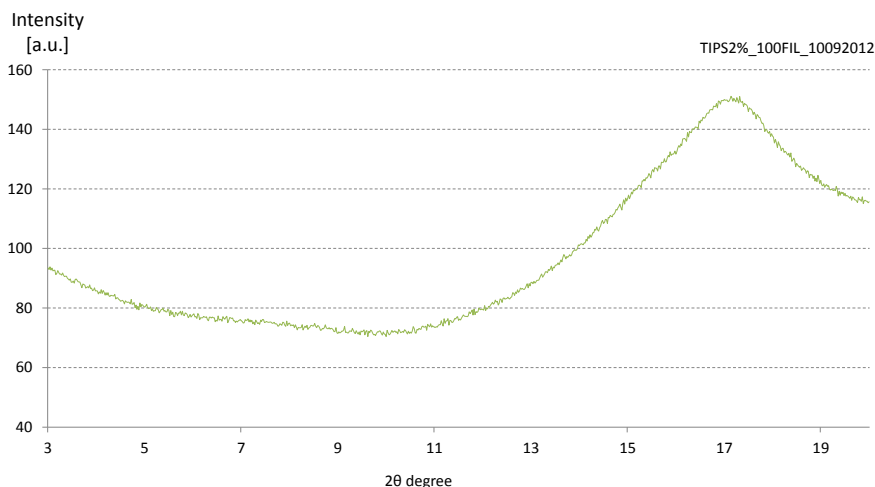


Figure 156 XRD scan of a TIPS-pentacene layer on a copper and polyimide coated polyester filament

In order to obtain a spectrum of TIPS-pentacene on a filament by XRD which yields sufficient reliable data for interpretation, measuring conditions had to be adjusted for detecting the crystallinity in the TIPS-pentacene layer.

Firstly, the amount of samples was increased from one to 6 samples per measurement to offer an increased surface area for analysis. Secondly, the direction of the samples inside the setup was changed

from perpendicular to parallel to the x-ray beam direction. Thirdly, the position in height of the samples was adjusted so that the x-ray could exactly hit the surface of the sample. For this reason, other filaments with the same thickness as the coated sample were used to position the sample holder. A scheme of the positioning of the samples in the sample holder of the setup is shown in Figure 157.

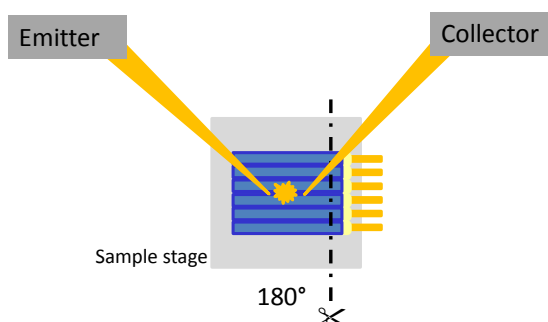


Figure 157 Six dip-coated filaments positioned on sample holder in 180° direction, parallel to X-Ray Diffraction (XRD) beam

In addition to positioning and alignment of the samples, the measuring time was increased whereas the range to be scanned was decreased leading to a smaller scanning step size and rate.

Following the technique as described above, new measurements were conducted. The first long-term measurement was conducted overnight with an approximate duration of 12 h. The scanning range was set to $2\theta \div 3^\circ - 22^\circ$. The slit size at the emitter was set to 1.5 and 2, whereas the slit size at the collector was set to 2 and 1. Power was fixed to 45/40. This long-term scan showed crystallinity of the TIPS-pentacene layer on a filament for the first time. The polyimide and copper coated filaments were dip-coated in TIPS-pentacene at the speed of 5 mm/min. A peak was detected approximately at 5.4° (Figure 158).

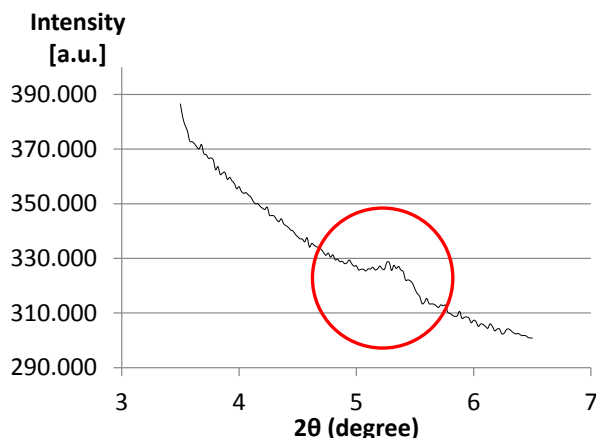


Figure 158 XRD of TIPS-pentacene layer on filament showing a peak at approximately 5.4°

In summary, after initial trial for detecting the layer's crystallinity by XRD failed, it was not clear if the measurement would be suitable for analysing the layer on the filament. Reasons for this assumption were the small amount of material deposited (thin film) and the small surface areas due to the surface curvature of the filament. By adjusting the measuring technique and resulting diffractogram, it was proven that the measurement technique was applicable on the filament.

Some more practical adjustments were made for the following measurements and are described below.

- To focus the emitted X-ray beam and to open the collector as wide as possible. The slit sizes of the emitter were change to 0.7 and 1.0 and of the collector to 2 and 1.
- To avoid any response resulting from the sample holder, the plastic holder was substituted with a silica holder and cleaned with ethanol before use.
- To increase the quality of the measurement at constant measuring time (12 h), the interval which was scanned was reduced to app. $2\theta \div 4^\circ - 6.5^\circ$.

By controlling the external conditions, samples produced at three different dip-coating speeds were analysed. As shown in chapter 9,

the dip-coating speed affects the deposited layer thickness. The faster the dip-coating speed the thicker is the layer deposited. Figure 159 shows the diffractogram of TIPS-pentacene layers deposited by dip-coating at 1, 5 and 50 mm/min on a polyimide and copper coated polyester filament.

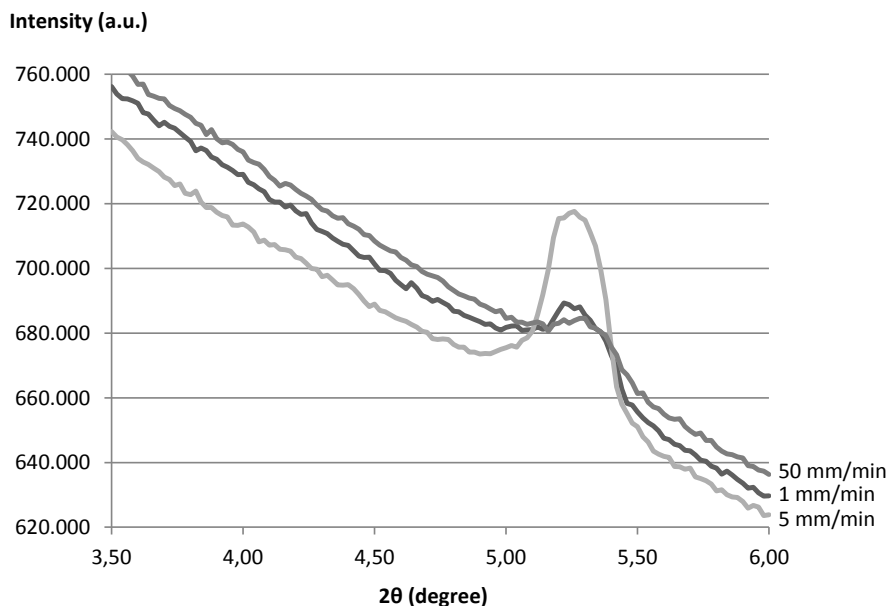


Figure 159 XRD of sample dip-coated in TIPS-pentacene at a dip-coating speed of 1 mm/min, 5mm/min and 50 mm/min

As can be seen in Figure 159 to **Error! Reference source not found.**, all three layers showed crystallinity with a different intensity. Highest intensity of the peak at 5.4° was achieved at a di-coating speed of 5 mm/min. It is questionable if the samples, indeed, exhibit different crystallinity or if observed differences are due to differences in positioning. The following experiments showed that the qualitative *best* crystallinity was achieved at a speed of 5 mm/min confirming the high intensity detected by XRD. The results of the effect of dip-coating speed on the layer morphology are shown in the following section (p. 284).

c) Conclusion for choice method of analysis

The detection of crystallinity in TIPS-pentacene thin films on a polyimide and copper coated polyester filament by XRD is feasible, if the right method is used, including correct positioning, alignment of the samples in the x-ray beam direction and a long-term measurement at reduced scanning range. This method, being inserted in the outline of the production of an entire OFET on a filament, XRD is not the optimal choice in terms of time and effort expended. The measurement required at least six samples which had to be prepared at very low dip-coating speeds e.g. 1 mm/min. Dip-coating and handling of only one sample at this speed and at dip-coating depth of 25 mm requires about 60 min. Hence, subsequently preparing six samples including a drying time of 90 min can take up about 8 hours. All-in-all, preparation of the substrate under laboratory conditions and measurement do take up to 20 h. Consequently, the sample preparation for detecting crystallinity in the layer by X-Ray diffraction cannot be completed in a time efficient manner and therefore would not be suitable as quick method before application of the top-electrodes and subsequent electrical characterization. As shown above [1]), the deposited layer is sensitive to environmental influence. The top-electrodes should be deposited right after semi-conductor deposition to achieve electrical characterization. This intervention following the long-term measurement, not only falsified the electrical measurement, but degraded the entire semi-conductor layer. In addition to time constraints, the measurement results do not add to a quantitative evaluation of the layer due to the variation in peak height which could be derived from variation in the positioning or alignment of the samples on the sample holder.

Optical microscopy, using a polarizer, is the most adequate technique to analyse the crystallinity of the deposited TIPS-pentacene layer on the filament. The crystal scan is qualitatively evaluated in view of their size, distribution and shape. The effect on the crystallinity in the semi-conductive layer when rendering the process conditions in the following sections will therefore be evaluated by optical microscopy mainly. Once up-scaling of the coating process is achieved the potential of the analysis via XRD should be reassessed.

3) Effect of drying conditions on crystallinity in TIPS-pentacene layer detected by optical microscopy on polyimide and copper coated polyester filament

Optical microscopy was most suitable for the analysis of the crystallinity of the semi-conductive layer as deposited on the polyester filament. The following sections describe the results using this qualitative assessment technique when rendering the drying conditions during solidification of the TIPS-pentacene layer on the polyimide and copper coated polyester filament but also in comparison to the layer as deposited on the polyimide coated copper plate.

a) Sample preparation

The dip-coating solution is prepared as described in chapter 6. In addition, before dip-coating in the TIPS-pentacene solution the polyimide-coated filaments were cut in length. To remove the thicker part of the polyimide layer one cm was cut-off from the bottom. The complete coating process in respect to the polyester filament's dimension is shown in Figure 160.

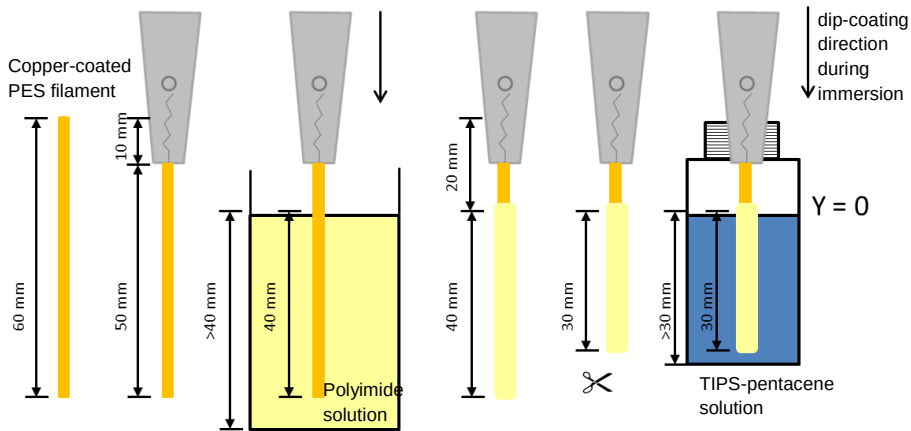


Figure 160 The scheme shows the dimensions in processing the substrate: from the copper-coated polyester filament to dip-coating in polyimide and subsequently TIPS-pentacene

b) Analysis of TIPS-pentacene layer by optical microscopy

Experiments regarding dip-coating in 2w% TIPS-pentacene/toluene solution was initially completed on a copper plate as described in chapter 6. The initial test should rule out the influence of the surface curvature of the cylindrical substrate being a wire or filament. The copper wire was used because it was assumed that the surface roughness of the wire and the plate were similar. Following a polyimide coated wire, as purchased, was used to exclude the influence of the quality of the polyimide layer. And finally, the TIPS-pentacene layer was deposited on a copper-and polyimide coated polyester filament which was the targeted textile substrate.

i. TIPS-pentacene layer on polyimide coated copper plate

In this experiment, polyimide copper plates were dip-coated in TIPS-pentacene at a speed of 50 mm/min and dried for duration of 120 minutes at 60°C. The preceding polyimide coating was conducted at 50 mm/min in a polyimide/NMP solution with a concentration of 15w%. The semi-conductive layer was deposited at a dip-coating speed of 50 mm/min on a polyimide coated copper plate is shown in Figure 161.

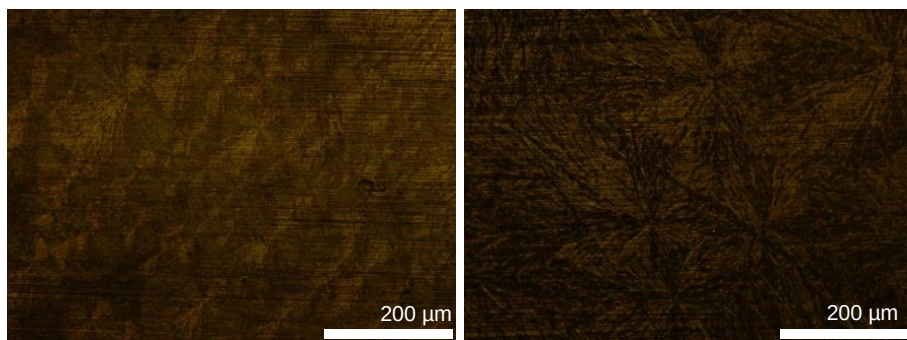


Figure 161 Two microscopy pictures of the TIPS-pentacene layer on polyimide coated copper plate. The semi-conductive layer was dip-coated at 50 mm/min in 2w% TIPS-pentacene/toluene solution and dried for 120 min. at 60°C

To obtain a preliminary indication regarding the effect of dip-coating speed on the crystallisation, the polyimide coated copper plate was also dip-coated at 75, 100 and 150 mm/min (Figure 162).

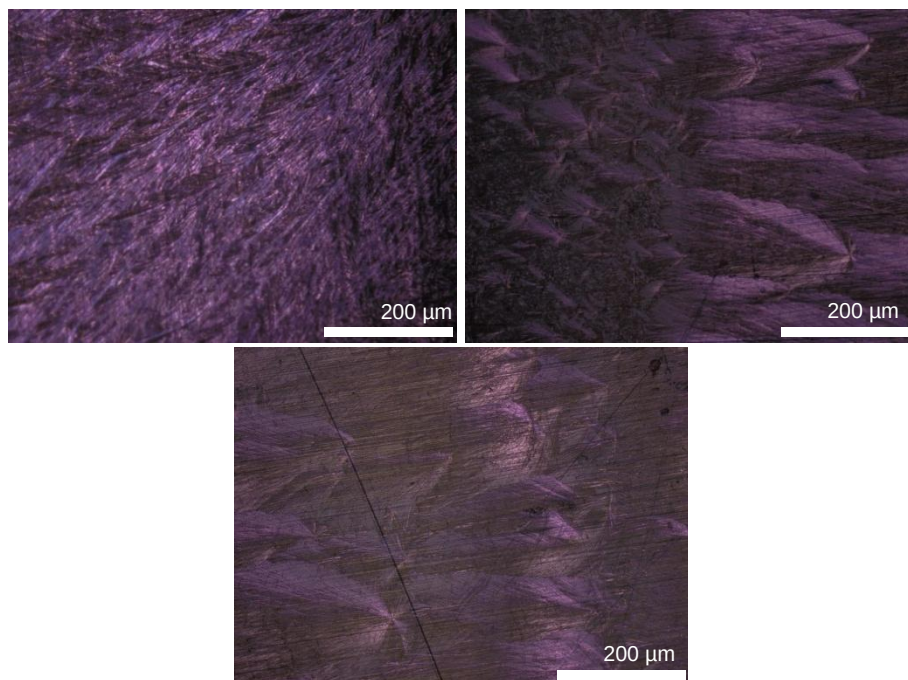


Figure 162 Polyimide coated copper plate dip-coated at 75 mm/min (top left), 100 mm/min (top right) and 150 mm/min (bottom) in 2w% TIPS-pentacene/toluene solution dried for 120 min. at 60°C

Crystals could only be detected on the flat copper plate but not on any of the cylindrical substrates. An attempt was made to improve the crystalline structure by rendering the drying conditions. This should lead to a crystalline structure on the cylindrical substrates visible in optical microscopy.

- ii. Effect of drying the TIPS-pentacene layer, as deposited on a polyimide coated copper plate, in solvent rich and ambient environment

Nam et al. (2010) discussed the effect on layer morphology when drying the film in different solvents. It was stated that crystal growth can be influenced by changing drying conditions. Drying in solvent

rich atmosphere was singled out as a method to extend the time for crystallisation since the layer cannot solidify as quick as in ambient conditions [156].

A) Drying of the semi-conductive layer in solvent rich environment (toluene)

A glass desiccator was equipped with a small vessel (approximately 50 ml) containing toluene. After dip-coating the substrate in TIPS-pentacene the sampled was placed into the desiccator for drying at room temperature. The solvent content at equilibrium in the closed environment inside the desiccator is difficult to define, because the desiccator had to be fully opened before adding the dip-coated samples, decreasing the saturation within the environment. The samples were dried in this setup for 3 h. Crystals could be detected on the polyimide coated copper plate as shown in Figure 163.

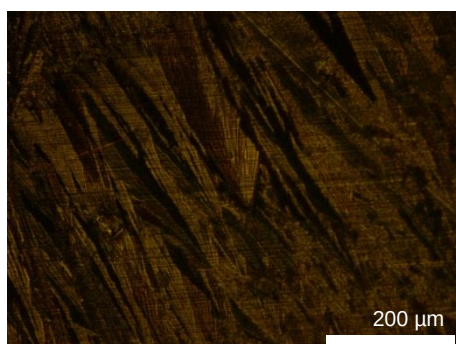


Figure 163 Polyimide coated copper plate dip-coated at 50 mm/min in 2w% TIPS-pentacene/toluene solution dried for 180 min. at room temperature in solvent rich atmosphere (toluene)

The length of the crystals was increased by extending the drying time in the solvent rich atmosphere. Still no effect was observed relating to crystal growth on the cylindrical substrates. As suggested by Lee (2007), a post-treatment by placing the solidified layer into solvent rich atmosphere could enhance crystallinity after solidification of the layer [157].

A) Post-treatment of the semi-conductive layer in solvent rich environment (toluene)

Dip-coated and solidified TIPS-pentacene layer synthesized, dried, and was placed in solvent rich atmosphere for 24 h. After 24h, the crystals in TIPS-pentacene layer deposited on the polyimide coated copper plate showed less definition (Figure 164).

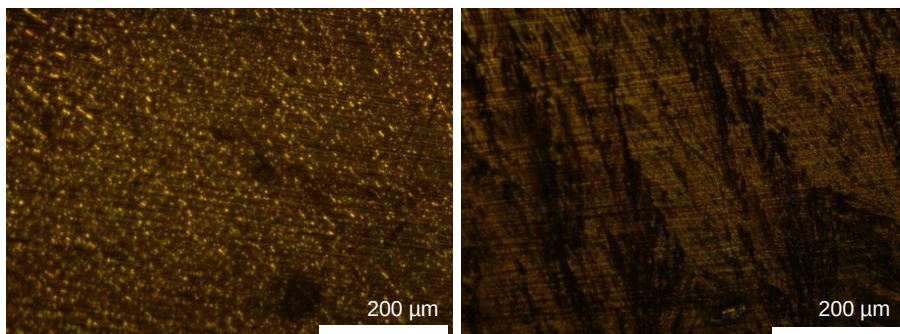


Figure 164 TIPS- pentacene layer dried at 60°C for 2 h (left) and layer dried in solvent rich atmosphere in ambient temperature for 3 h (right) on polyimide coated copper plate after post-treatment in solvent rich atmosphere for 24 h at room

On the cylindrical substrates, the polyimide coated copper wire and the polyimide and copper coated polyester filament, some small crystals became visible after the post-treatment (Figure 165 and Figure 166).

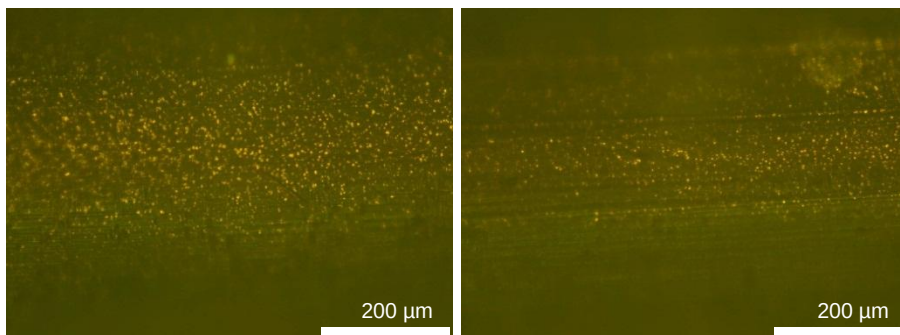


Figure 165 TIPS-pentacene layer dried at 60°C for 2 h (left) and layer dried in solvent rich atmosphere in ambient temperature for 3 h (right) on polyimide coated copper wire after post-treatment in solvent rich atmosphere for 24 h at room temperature

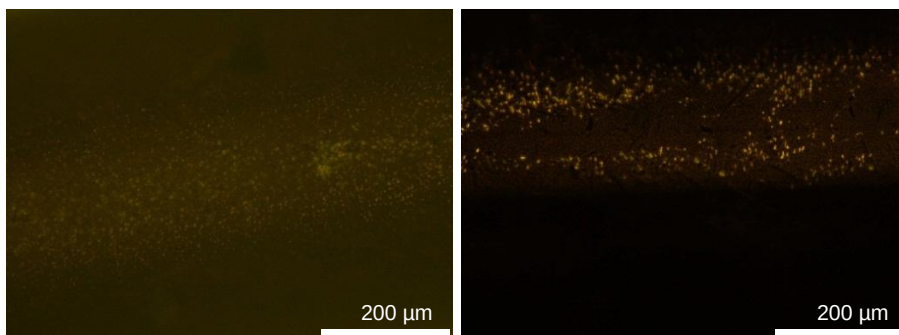


Figure 166 TIPS-pentacene layer on polyimide and copper coated polyester filament after post-treatment in solvent rich atmosphere for 24 h at room temperature (based on layer dried at 60°C for 2 h (left) and layer dried in solvent rich atmosphere in ambient temperature for 3 h (right))

On the polyimide coated copper wire, the amount of crystals was higher, however, since the final application of the TIPS-pentacene is supposed to be applied on the polyester filament only, the layer on this substrate was targeted for optimisation.

To investigate the effect in reducing the drying time in solvent rich atmosphere after dip-coating, the time was decreased to 90 min. Again the cylindrical substrate did not show any crystal growth, whereas on the polyimide coated copper plate the crystals grew in a more spherical arrangement than when drying in solvent rich atmosphere for 3 h. The change in structure of the crystals is shown in Figure 167.

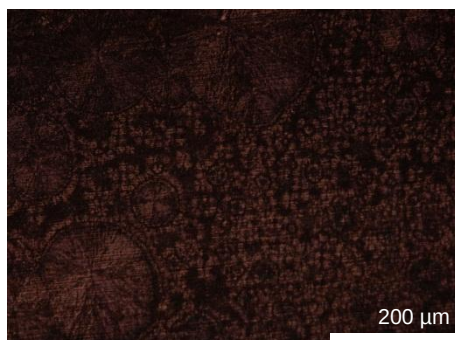


Figure 167 TIPS-pentacene layer on polyimide coated copper plate after drying at reduced time for 1.5 h at room temperature solvent rich atmosphere

B) Drying of the semi-conductive layer in solvent rich environment (ethanol)

In a final experiment in this preliminary test series, the three different substrates were dip-coated in TIPS-pentacene at 100 mm/min and dried in ambient conditions as well as in solvent rich atmosphere. To test the effect when changing the solvent, this time ethanol instead of toluene was placed into the desiccator. In Figure 168, the TIPS-pentacene layer on the polyimide coated copper plate is shown.

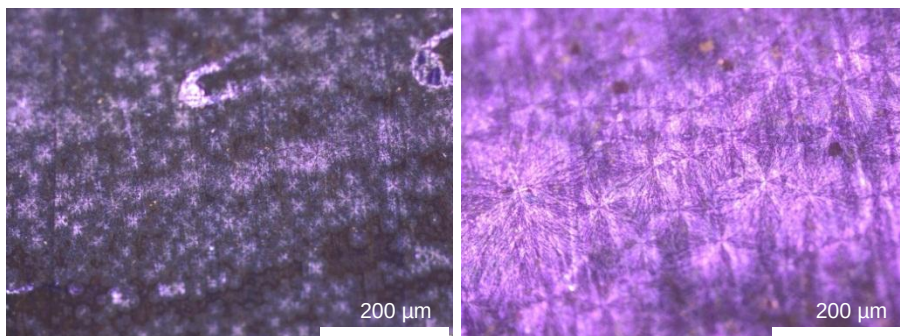


Figure 168 TIPS-pentacene layer on polyimide coated copper plate dip-coated at 100 mm/min, after drying at reduced time for 1 h at room temperature in solvent rich atmosphere (left) and drying in ambient conditions (right)

Also on the cylindrical substrates crystals were detected as shown in Figure 169 and Figure 170. The crystal structure was enhanced in those layers dried in ambient conditions.

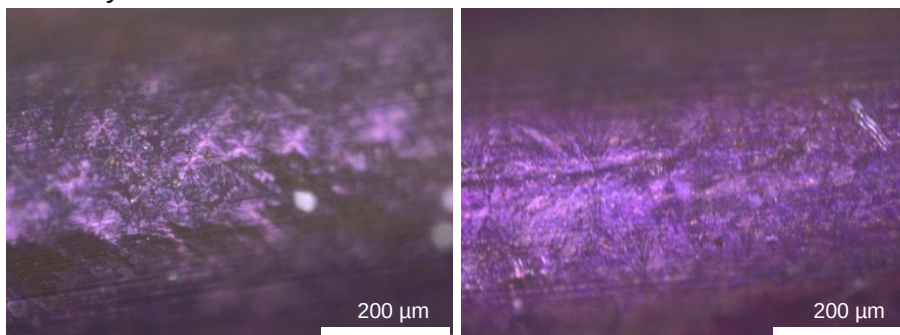


Figure 169 TIPS-pentacene layer on polyimide coated copper wire dip-coated at 100 mm/min, after drying at reduced time for 1 h at room temperature in solvent rich atmosphere (left) and drying in ambient conditions (right)

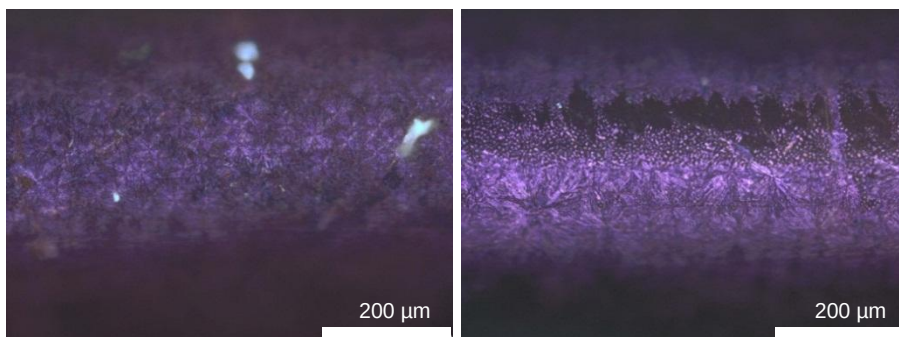


Figure 170 TIPS-pentacene layer on polyimide and copper coated polyester filament dip-coated at 100 mm/min, after drying at reduced time for 1 h at room temperature in solvent rich atmosphere (left) and drying in ambient conditions (right)

Based on the experiments above, it was concluded that drying in solvent rich environment does not improve crystallisation in terms of their shape or size. Drying in ambient conditions led to superior results. Furthermore, crystal growth on flat substrates seems to be easier to achieve than on substrates with a curvature. Whereas the crystals show increased growth on the copper coated substrate compared to the copper wire substrate. It is highly likely that the roughness of the layers as deposited below TIPS-pentacene influence the growth on the filament.

C) Drying of the semi-conductive layer at elevated temperature

Because the organic semi-conductor TIPS-pentacene was known to be sensitive to humidity, air and light [154], it was decided to keep the drying conditions at 60°C to avoid humidity. In addition the influence of temperature was investigated. Drying time was reduced to 60 minutes at 60°C with an additional 30 minutes in ambient conditions in the dark.

As for the drying process, a range of combinations were tested. Drying was completed in two steps, the duration of the first step was 30 minutes, and the second had duration of 60 min. The various combinations of drying condition as well as the investigated dip-coating speeds are shown in Table 9. The quality of crystals was assessed and colour coded. Three levels could be achieved, namely

good, sufficient and insufficient. Good quality, indicated in green, showed an even distribution of crystals in the analysed section of the layer. The size of the crystals is big and the shape is feathery with long crystal growth. The level of insufficient marked in orange, shows an uneven distribution of crystals which are small in size and spherical in shape. Indicated in light green colour, is level sufficient. This layer is the intermediate level, in which at least one of the factors (distribution, size, shape) is insufficient or its overall assessment is not convincing.

Table 9 Overview of experiments related to drying conditions at various dip-coating speeds (v)
Colours indicate quality of crystals in solidified layer: green = very good, light green = sufficient, orange = insufficient

Step 2 – 60 min Step 1: 30 min	V [mm/min]	Ambient	45°C	60°C	desiccator – Solvent rich Toluene
Ambient	25				
	50				
	75	x			
	100				
	150				
desiccator – Solvent rich Toluene	25				
	50				
	75				
	100				
	150				
60°C	25	x			
	50				
	75				
	100			x	
	150				

The best results after repeated dip-coating experiments were confirmed for and are marked with an additional x in Table 9. The results suggest that dip-coating at lower speeds lead to more defined crystals. Dip-coating at 25 mm/min and drying for 30 min at 60°C with an additional drying period of 60 min at ambient conditions, was perceived as giving the best results in terms of shape, size and distribution of the crystals. The layer resulting from this combination of speed and drying steps is shown in Figure 171.

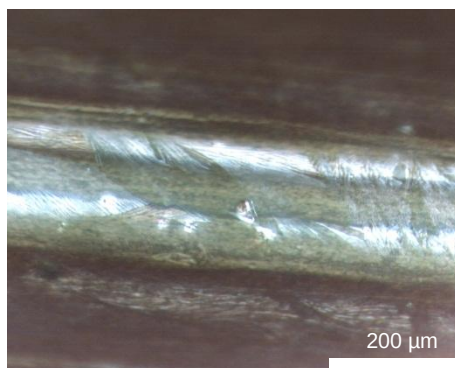


Figure 171 TIPS-pentacene layer dip-coated at 25 mm/min on polyimide and copper coated polyester filament dried in two steps, first Conclusion on drying conditions on crystallinity in TIPS-pentacene layer on polyimide and copper coated polyester filament

Experiments confirm that crystallinity in the semi-conductive TIPS-pentacene layer can be influenced by rendering the drying procedure of the layer during solidification after dip-coating. Drying in solvent rich atmosphere and elevated temperature has been tested and best results were achieved when applying a two-step drying process, i.e. drying the layer at 60°C for 30 min in dry conditions in combination with a following drying period of 60 min at ambient conditions in the dark. Furthermore, it was recognized that lower dip-coating speeds led to improved crystalline growth and morphology. The effect of the dip-coating speed is further investigated in the following section.

iii. Effect of dip-coating speed on crystallinity in TIPS-pentacene layer detected by optical microscopy

As shown above [p. 257], previous experiments resulted in better layer morphology in terms of crystal distribution, size and shape, when dip-coated at lower speeds. Hence, the effect of dip-coating speed on the crystallisation of TIPS-pentacene layer was investigated.

a) Dip-coating at different dip-coating speed on polyimide and copper coated polyester filament

A range of dip-coating speeds and the effect on the crystallisation in the semi-conductor layer was investigated. Dip-coating was completed at 1 mm/min, 5-50 mm/min (in steps of 5mm/min), 75, 100, 125, 150 mm/min. In Figure 172 till Figure 187, two microscopic pictures at a magnification of 25x are shown for each dip-coating speed. The TIPS-pentacene layer has been deposited onto a the polyimide layer which was dip-coated at 100 mm/min and a at solution concentration of PI/NMP 15w%. The experiment only has been conducted on the polyimide and copper coated polyester filament.

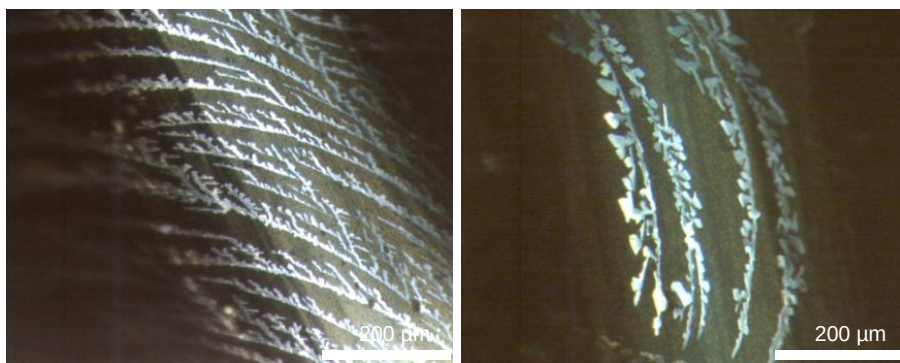


Figure 172 TIPS-pentacene layer dip-coated at 1 mm/min

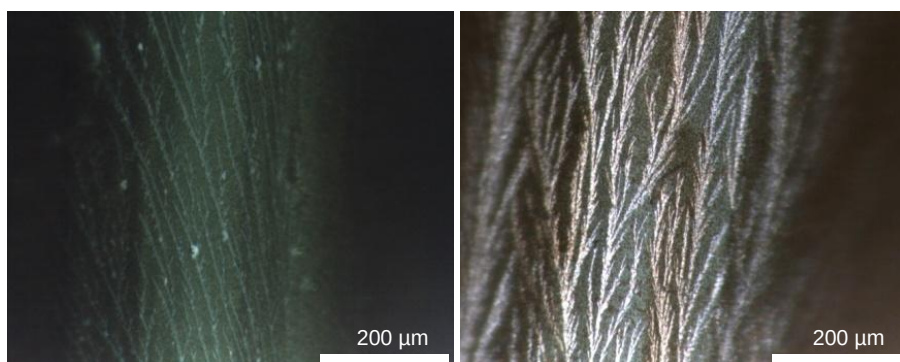


Figure 173 TIPS-pentacene layer dip-coated at 5 mm/min

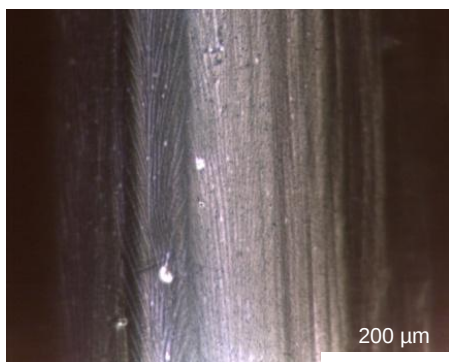


Figure 174 TIPS-pentacene layer dip-coated at 10 mm/min

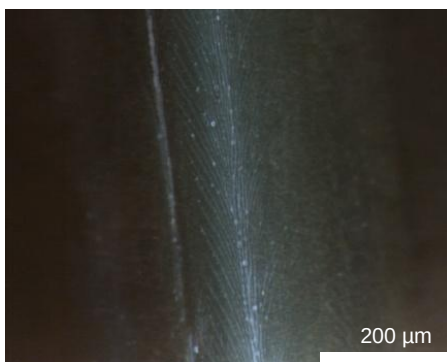


Figure 175 TIPS-pentacene layer dip-coated at 15 mm/min

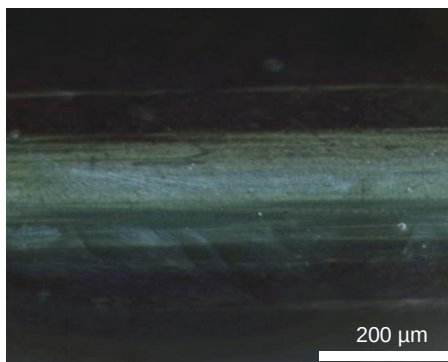
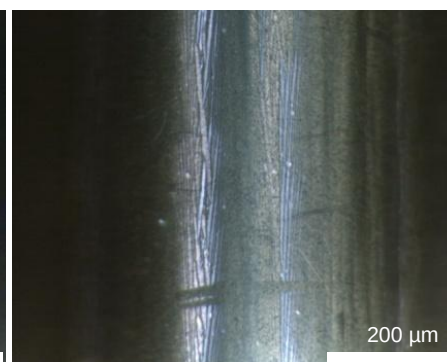
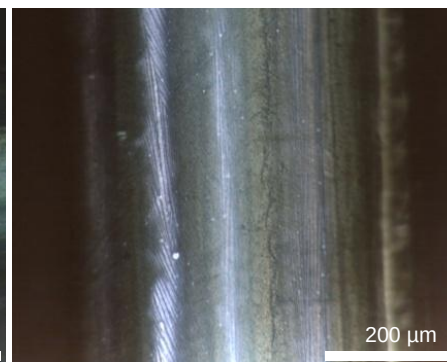


Figure 176 TIPS-pentacene layer dip-coated at 20 mm/min



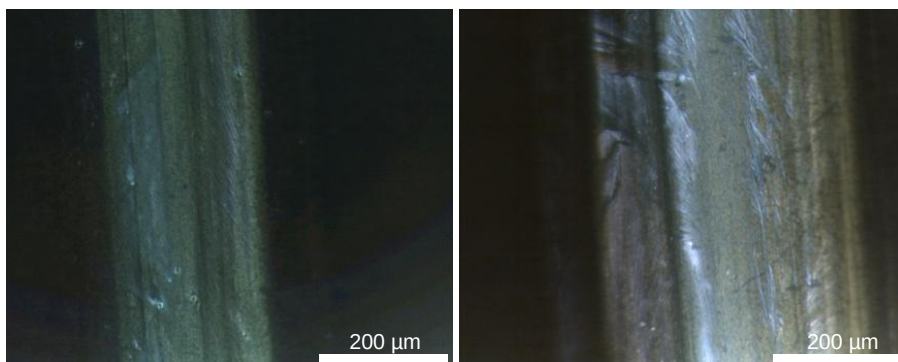


Figure 177 TIPS-pentacene layer dip-coated at 25 mm/min

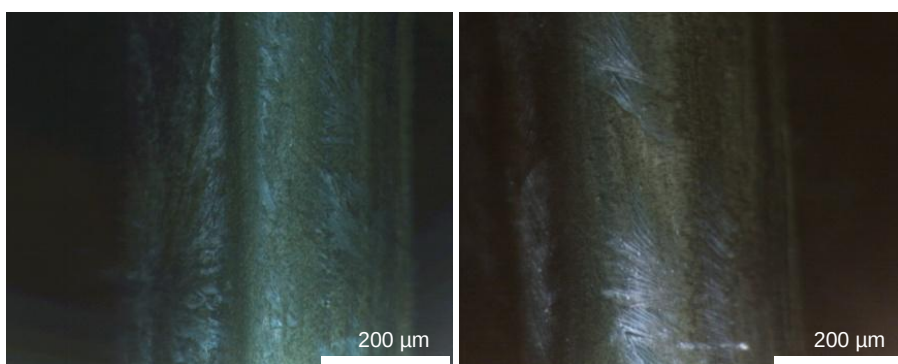


Figure 178 TIPS-pentacene layer dip-coated at 30 mm/min

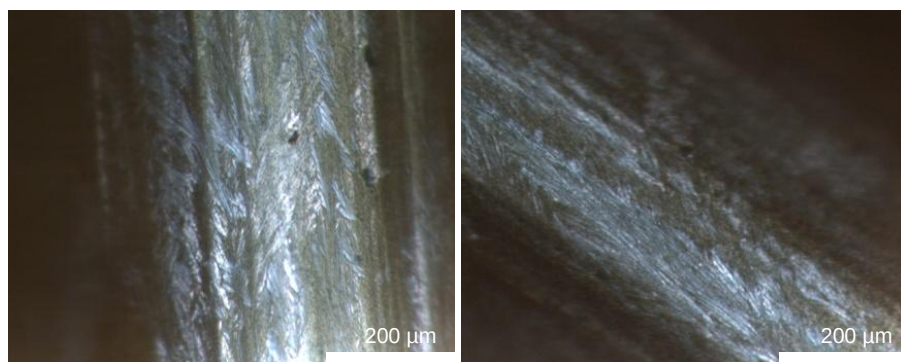


Figure 179 TIPS-pentacene layer dip-coated at 35 mm/min

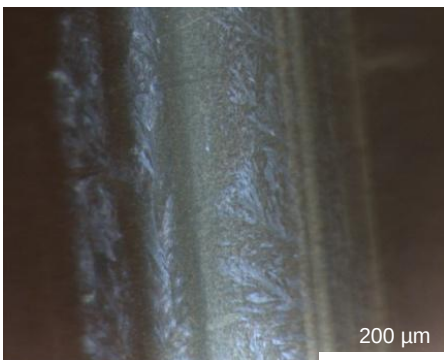


Figure 180 TIPS-pentacene layer dip-coated at 40 mm/min

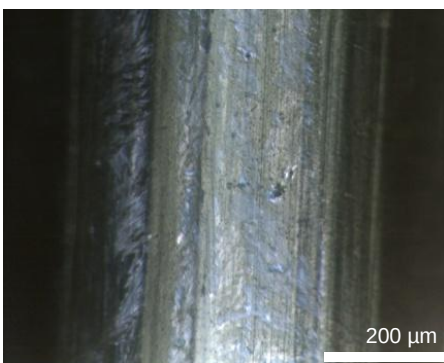
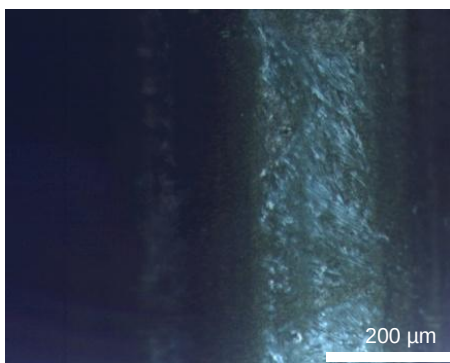


Figure 181 TIPS-pentacene layer dip-coated at 45 mm/min

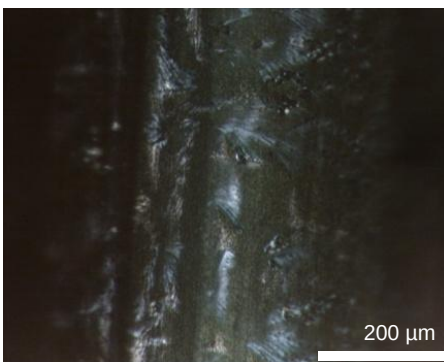
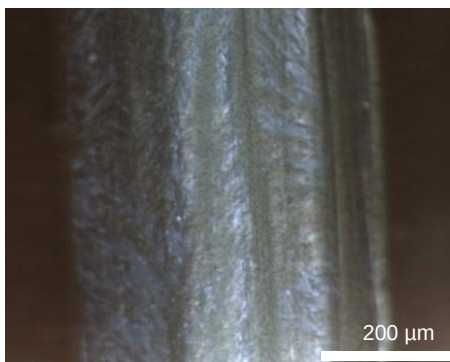


Figure 182 TIPS-pentacene layer dip-coated at 50 mm/min

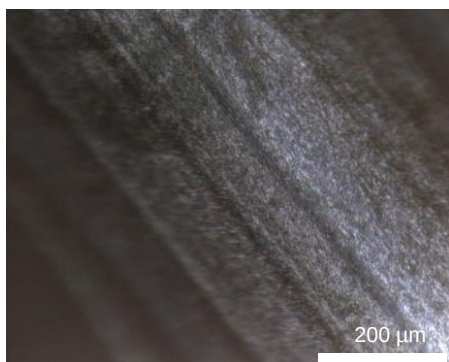


Figure 183 TIPS-pentacene layer dip-coated at 75 mm/min

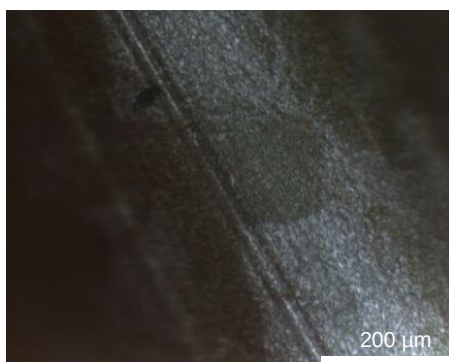
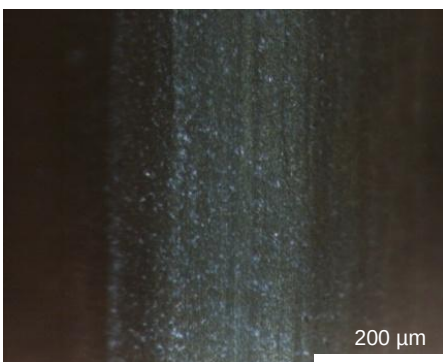


Figure 184 TIPS-pentacene layer dip-coated at 100 mm/min

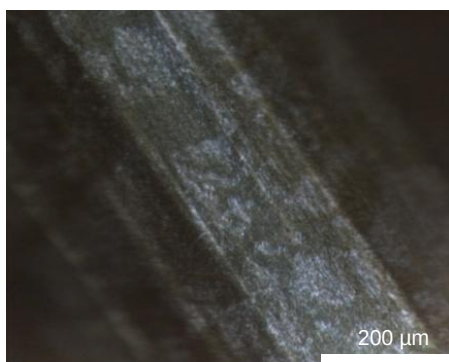
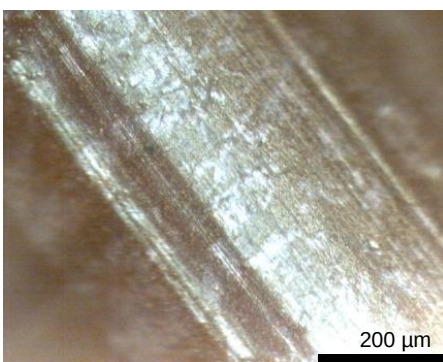
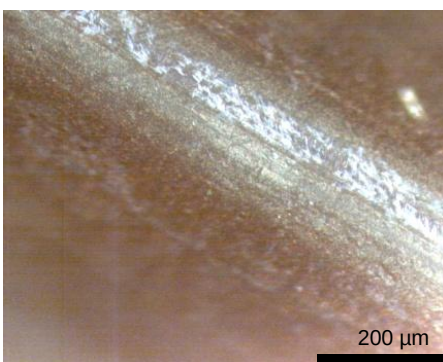


Figure 185 TIPS-pentacene layer dip-coated at 125 mm/min



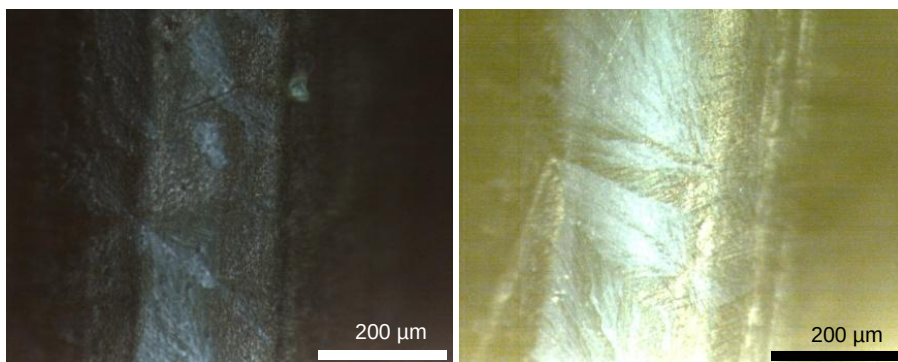


Figure 186 TIPS-pentacene layer dip-coated at 150 mm/min

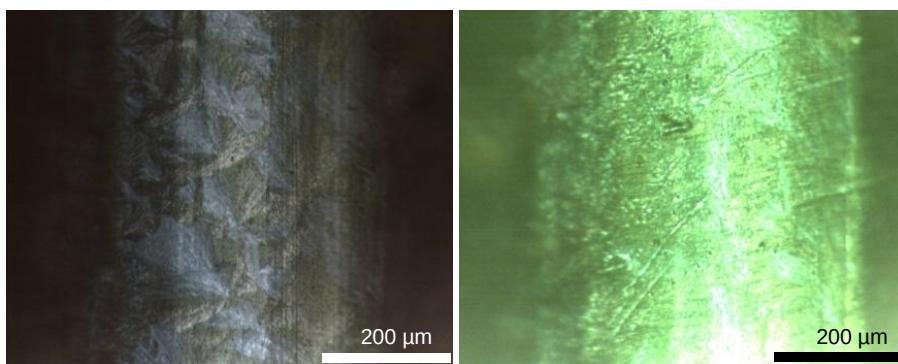


Figure 187 TIPS-pentacene layer dip-coated at 175 mm/min

b) Evaluation of the images obtained by optical microscopy

A clear effect of dip-coating speed on the semi-conductive layer crystalline morphology was recognised. The layer was assessed qualitatively in view of three factors, namely crystal distribution, size and shape. This list of factors might be increased based on the conducted microscopic analysis. Not only the distribution of crystals but also their amount per area analysed was taken into account. The fineness of the feathery shaped crystals which is seen in relation to the size and clear structure (definition in shape) of the crystal as well as the alignment of the crystal in comparison to the filament's axis, where clearly affected by the dip-coating speed. Once again, all those factors were solely assessed in terms of quality. A summary of these factors is shown in Table 10.

Table 10 Summary of factors related affected by variation in dip-coating speeds

	dip-coating speed (v)	
	low	high
distribution	even	uneven
size	big	small
amount	less	much
crystals fineness	higher	lower
definition in shape	more defined	less defined
alignment in filament axis direction	parallel	perpendicular

Besides this qualitative assessment based on the scheme as shown above, it was made the attempt to qualitatively assess two factors within the listed, i.e. crystal length and crystal orientation in filament axis direction. For this reason a software tool during optical microscopy was used for measuring distance and angles within the generated picture.

As recognised during practical application of the tool, the data gathered strongly depends on the manual input or influence by the operator of the microscope. Point for start and end of a distance have to be set manually and therefore are highly influencable, the same accounts for point while measuring angles.

Based on the assessment of quality (as shown above), the attempt was made to assess the quality of two listed factors i.e. crystal length and crystal orientation in filament axis direction. For this reason the tool during optical microscopy were used for measuring distance and angles within the generated picture. As observed during practical application of the function, the gathered data strongly depends on the manual input or influence by the operator of the microscope. The start and end points of distance have to be set manually and therefore are highly susceptible to influence by the operator, the same is applicable to points, when measuring angles. The two images in Figure 188 and Figure 189 give an indication regarding the function, which could be further optimised for future investigation.

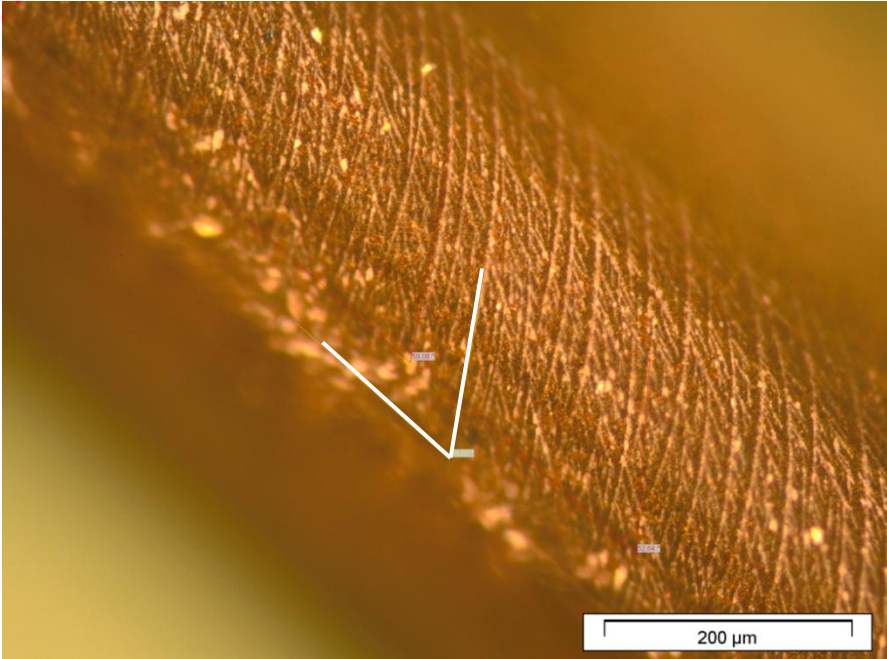


Figure 188 Measuring angles in crystal growth by software in optical microscopy

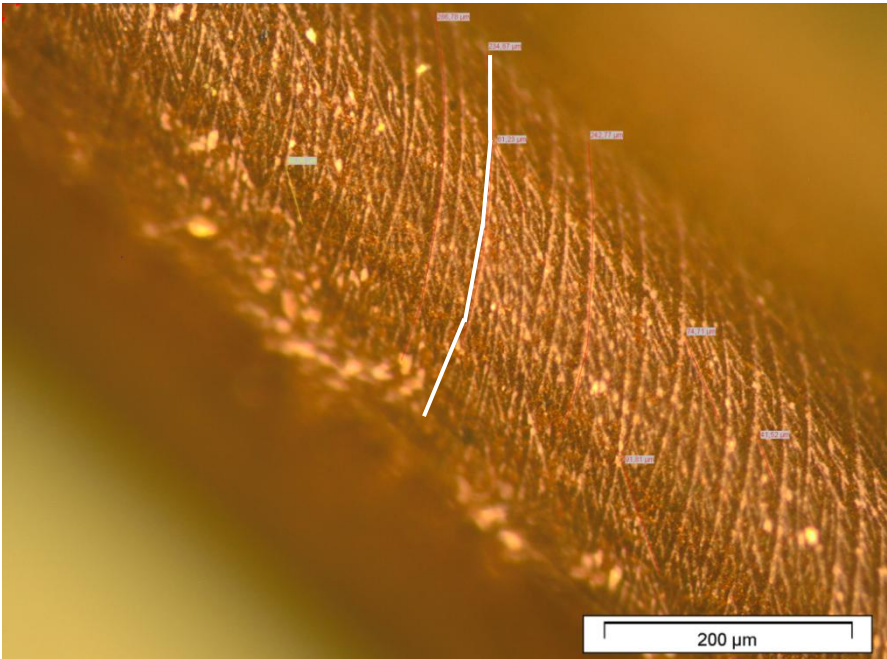


Figure 189 Measuring lengths of crystal growth by software in optical microscopy

c) Conclusion for possible effect of dip-coating speed during deposition of semi-conductive layer

The effect of dip-coating speed during TIPS-pentacene layer deposition on the crystalline morphology within the same layer after solidification has been investigated. The dip-coating speed was varied from 1 mm/min up to 170 mm/min and clear changes in the crystal outline within the deposited layer were detected.

A list of factors related to the crystals influenced by the varied dip-coating speed was developed offering a scheme based on quality for evaluation. Also by utilizing optical microscopy, an attempt was made to quantitatively evaluate the two factors, namely crystal length and crystal orientation in filament axis direction. This method was not further pursued since the resulting data was unreliable. Overall best results for crystal morphology of the TIPS-pentacene deposited layer on the polyimide and copper coated filament were achieved at a dip-coating speed of 5 mm/min.

iv. Temperature of filament

Chen *et al.* (2007) suggests that elevated temperature of the substrate itself during the dip-coating process affects crystal growth during solidification of the layer [158]. All polyimide-coated substrates were stored in dry conditions at 60°C prior to dip-coating. By using a thermographic camera it was investigated which temperature the substrate had reached when being dip-coated. A thermographic image was taken of the samples stored in the oven at 60°C. Then an image was taken during dip-coating. From the images it is apparent that the sample temperature drops fast from 60°C when stored in the oven to room temperature (approximately 22,6°C) due to transport and handling time until the dip-coating process can be started. Therefore heating the substrates prior to dip-coating could not have an effect on layer morphology. Storage at elevated temperatures reduces the risk of humidity on the surface of the polyimide dip-coated substrate before subsequent dip-coating in TIPS-pentacene (Figure 190).

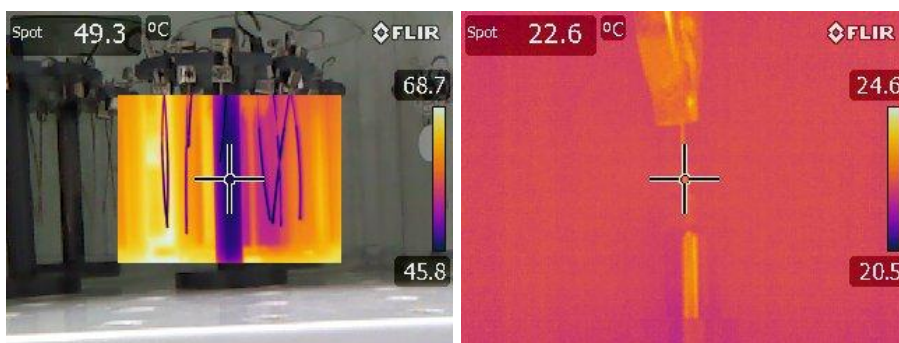


Figure 190 Thermographic images of filament during storage (door of oven was opened causing a temperature drop of about 10°C) and during the dip-coating process

v. Electrical characterization of the TIPS-pentacene layer

As discussed in chapter 9, contacting thin layers poses many challenges. This chapter deals with identification of additional challenges in the further development of the measuring setup from leak current measurement to transistor function measurement and measurements conducted within this partially new setup. Furthermore, the evaluation of the data gathered in respect to the layer's electrical properties are discussed.

a) Methodology on coated copper plate and challenges for application on coated filament

As stated in paragraph 9.7, attaching a copper wire with conductive ink to the surface of the copper plate was not very convenient. Often the wires broke off or the ink for fixating the wire spread across the edges creating short circuits, both rendered the contacts useless. In addition, this practice was only feasible on a flat copper plate but not on a small diameter surface of the polyester filament. Here the amount of ink to be applied to incorporate the copper wire, would not have stuck to the surface of the filament, due to gravity. In addition, accuracy in channel dimensions could not have been followed with this technique. Using nano-silver ink-jet printing ink to deposit the top-electrodes on the surface in combination with a new sample holder was a new approach to be tested. It shall be clarified that those

sample holders used during the coating, drying or storage processes cannot be used for the electrical characterization. Since testing equipment for fibrous transistors is unavailable to date, the developments with regard to further optimization of available testing methods should be described here.

- b) Development of a fibrous transistor probe station for conducting electrical measurements applying two top-contacts

Based on the leak current measurement conducted in electrical characterization of the polyimide layer, a new setup integrating two top-contact electrodes had to be developed.

- i) Sample holder for leak current measurement with one top electrode

For the leak current measurements of the polyimide dielectric layer deposited on the copper-coated polyester filament, a holder for fixation of the sample as well as for positioning a contact with a probe was developed. The first sample holder prototype, which was used for the leak current measurements in which at once only one top-contact is used, was composed out of an office paper clip and two small Plexiglas sheets, thus creating a groove at the bottom when placed into the clip. To avoid using sharp probe tips as described in chapter 9.7, probes with a flat tip were purchased. In addition to being flat, those tips also incorporate a spring which compressed when force was applied, touching the sample surface. Using this probe it was possible to avoid piercing through the semi-conductive thin film to be electrically characterized. A picture of the first prototype is shown in Figure 191.

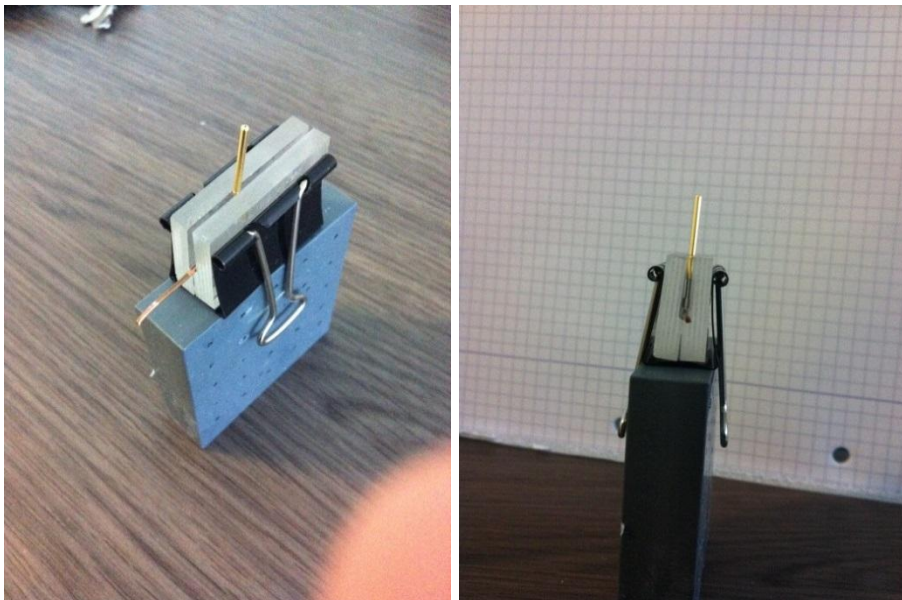


Figure 191 First generation sample holder for testing leak current on TIPS-pentacene, polyimide and copper-coated filaments

ii) Sample holder for transistor function measurement with two top electrode

When testing transistor properties, two electrodes had to be applied i.e. positioned and gently brought into contact with the surface of the filament. The first prototype required positioning two separate electrodes, at the same time opening the clamp to gently contact the surface simultaneously. With the first and the second contact In addition, dimensions of the sample holder, probe and sample itself were small and therefore handling all parts simultaneously was challenging. Positioning of the two probes and contacting was almost impossible without damaging the deposited layer. Even if the probe was fixed on its top by the clap, the probe still could slide to the sides at the bottom i.e. sliding on the surface of the filament if not positioned in exactly 90° . Since crocodile clamps were used to connect the probes with the measuring setup, slightly moving the probe was almost unavoidable. To reduce the risk of damaging the layer and to simplify the measurement procedure, a second generation sample holder including the contact probes was

developed. A schematic drawing and a picture of the developed transistor filament probe station are shown in Figure 192.

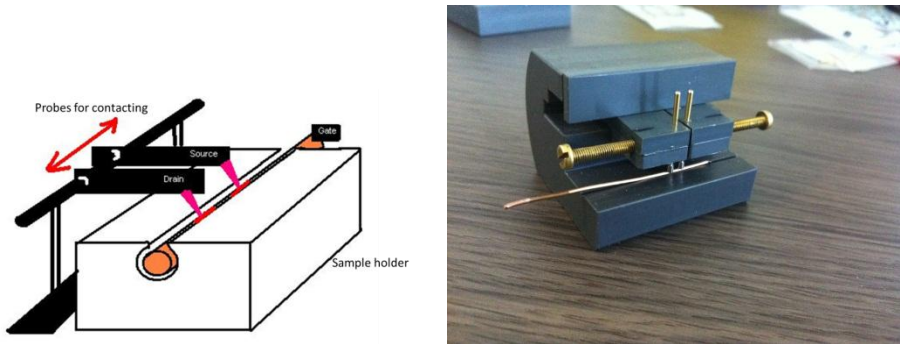


Figure 192 Schematic drawing for building a filament probe station (left) and its realization (right)

A new construction enabled the filament to be positioned in a groove which was engraved into the probe station. This groove had a diameter of $1000\text{ }\mu\text{m}$ fitting to a filament diameter of about $800\text{ }\mu\text{m}$. It prevented the filament from rolling away on contacting. The two contact probes were movable in vertical direction but also horizontally. Hence, the probe could be lowered until reaching the surface of the sample and then lowered an additional fraction to ensure close contact by compressing the integrated spring. Consequently, the probe could be fixated in this position by using a screw. The second probe could be dealt with individually or even taken off the system if not required. The handling of the thus fixated sample was much improved. The probes were not as prone to sliding and the connection between the holder and the measuring setup were more robust and could be connected with crocodile clamps as commonly used in electronics.

iii) Conclusion for application of the new measuring setup

The new sample holder or transistor filament probe station created a link between electrical characterization techniques as applied in electronics, and the textile substrate with a cylindrical shape. It is taken as read that these solutions create real bridges in bringing the different scientific fields in textronics together.

c) Investigation of electrical properties of the OFET on a polyester filament

The TIPS-pentacene layer was applied onto the polyimide and copper coated polyester filament by dip-coating at a speed of 5 mm/min. The dip-coating solution was prepared as 2w% TIPS-pentacene in toluene. The drying process included two steps, namely 30 min at 60°C and 60 min at room temperature. After application of the top-contacts by drop-casting of nano-silver conductive ink jet printing ink the transistor properties using the new fibrous transistor probe station were measured.

By increasing the voltage applied at the gate layer V_{GS} from 0 to 1.6 V, no visible change in the conductivity of the semi-conductive layer could be achieved. The transistor did not function as an electrical switch (Figure 193). In comparison to the non-typical transistor behaviour, the variation in applied voltage did change the electrical properties of the layer at $V_{DS} = 0$ V with varying V_{GS} . Firstly, it was assumed that by applying the increased voltage at V_{DS} an irreversible change in the electrical properties of the TIPS-pentacene layer was caused. This was not confirmed when conducting a measurement testing for hysteresis.

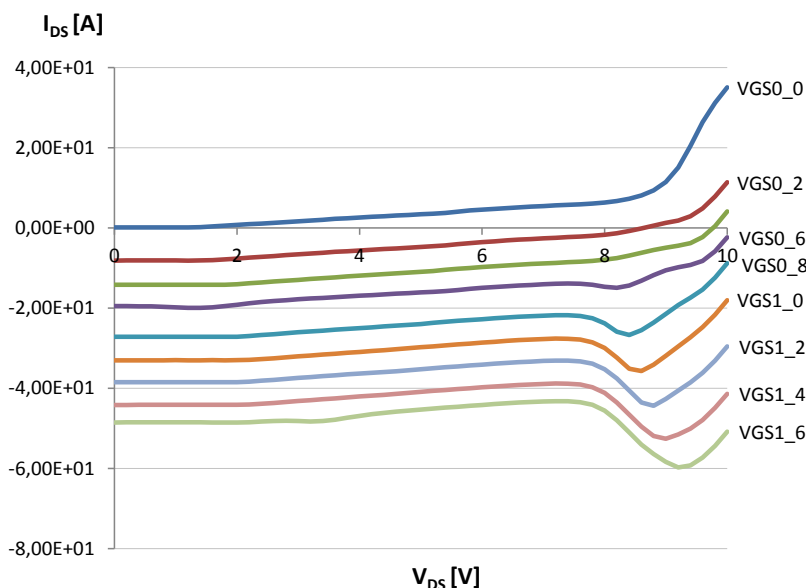


Figure 193 I/V curve at voltage levels applied on source and drain (V_{DS} 0 – 10 V) and gate (V_{GS} 0 to 1.6 V) as measured on fibrous transistor

When depicting the change in I_{DS} at constant $V_{GS} = 0$ and increasing V_{DS} , clearly linear behaviour was observed (Figure 194).

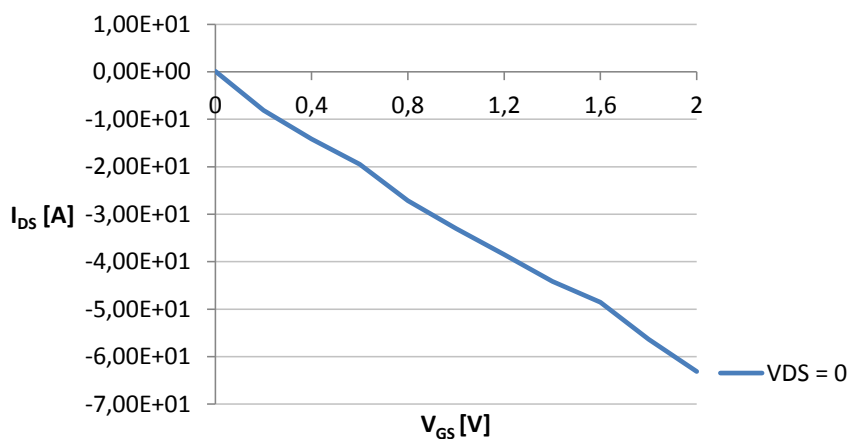


Figure 194 I/V curve at increasing V_{GS} for $V_{DS}=0$, as measured on fibrous transistor

Leak current measurement between the top contacts at different V_{GS} and constant $V_{DS} = 0$ V are shown in Figure 195.

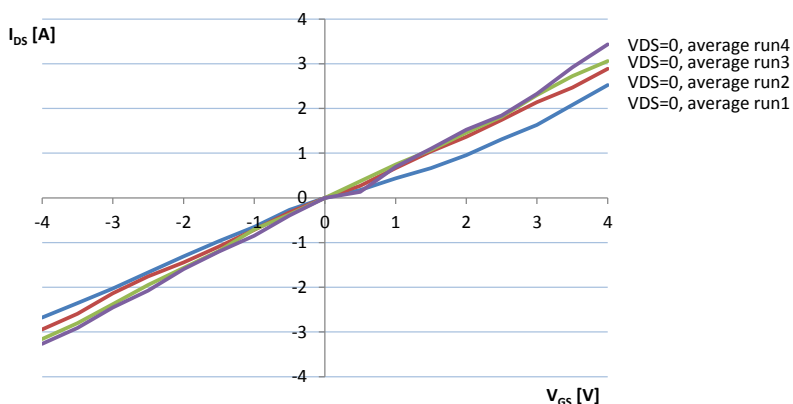


Figure 195 Leak current at constant $V_{DS} = 0$ V and increasing $V_{GS} = -4$ to $+4$ V

When comparing the insulating properties of the polyimide layer (see chapter 9) with the leak current values after application of the TIPS-pentacene layer, a decrease in the electrical insulation is shown. Hence, during the application of the semi-conductive layer, the polyimide layer is affected in its insulating properties.

In summary, the sensitivity of the organic material deposited by dip-coating under the described conditions leaves a huge number of uncontrollable factors which can affect the material's properties. Also device composition i.e. the interaction between the various layers might influence the behaviour of the semi-conductive layer. Based on the findings of the experiments, it remains unknown at present what could have influenced the change in properties of the dielectric layer but it also remains unknown why the semi-conductive material did not change electrical properties once an electrical field was generated by applying a voltage at the gate layer.

10.3. Overall conclusions – semi-conductive layer deposition

Toluene was chosen as suitable solvent for preparing the TIPS-pentacene dip-coating solution at a concentration of 2w%. Degradation of the compound in solution and in the deposited layer has been investigated which lead to optimisation of handling and material storage minimising the risk of degradation.

Different analysis techniques have been tested and XRD after optimising the methodology has been evaluated as one technique with high potential for analysing crystallinity in the deposited layer. Because of that the technique, at present, is not suitable for the entire component manufacturing process, XRD was not used for further analysis of the layer. Instead, optical microscopy using polarised light was chosen as most adequate technique for analysing the layer's morphology with regards to its crystallinity.

A list of factors which are likely to be susceptible to influence by varying the dip-coating speed' was drawn up, e.g. size, distribution and shape

Experiments confirm that crystallinity in the semi-conductive TIPS-pentacene layer can be influenced by rendering the drying procedure of the layer during solidification after dip-coating. Both, drying in ambient, solvent rich atmosphere and elevated temperature as well as a post-treatment in solvent rich atmosphere, have been tested and best results were achieved when drying the layer at 60°C for 30 min in dry conditions in combination with a following drying period of 60 min at ambient conditions in the dark.

The effect of dip-coating speed during TIPS-pentacene layer deposition on the crystalline morphology within the same layer after solidification has been investigated. The dip-coating speed was varied from 1 mm/min up to 170 mm/min and clear changes in the crystal outline within the deposited layer were detected. Overall best results for the layer's crystal morphology (TIPS-pentacene deposited on the polyimide and copper coated filament were achieved at a dip-coating speed of 5 mm/min.

During electrical characterization of the layer, a new sample holder (transistor filament probe station) was developed ensuring a link between electrical characterization techniques as applied in electronics and the textile substrate with a cylindrical shape. With this setup the change in resistivity of the deposited layer when applying a voltage at the gate layer was investigated. Unfortunately, the semi-

conductive material did not change electrical properties once an electrical field was generated by applying a voltage at the gate layer.

We assume that the sensitivity of the organic material deposited by dip-coating under the described conditions does still leave to much room for other factors to influence the performance of the layer and therefore the device. The transistors in their current configuration do show behaviour similar to a resistor. Though, its leak current compared to the dielectric layer as described in chapter 9, is higher. We also assume that device composition i.e. the interaction between the various layers might have an effect on the behaviour of the semi-conductive layer. It remains unknown which factors influenced the detected behaviour and further investigation is recommended.



Part III Conclusion and future perspectives

In Part I a new classification scheme based on technical integration levels was developed for e-textiles as subgroup of smart textiles. This classification system enables the comparison between different e-textiles. In Part II the technical hurdles have been discussed in relation to integration level 4B (single), based on an Organic Field Effect Transistor on a polyester monofilament. Part III of this dissertation leaves room for summarizing conclusions and a look into perspectives for continuation of the research in chapter 11.

11

Conclusions

Chapter 11 summarizes the conclusions made in Part I and II of this dissertation. In addition, further research directions regarding fibrous field effect transistors are suggested.

The conclusions in Part I and Part II are summarized below. Furthermore, overall conclusions are summarized section 11.3.

11.1. Part I

Part I reviewed and analysed the field of smart textiles with particular reference to commercial products, patent applications and research in the field, identifying a need for development of shared definitions of concepts within smart textile systems and the e-textile active components on a technical level. Therefore a scheme for classifying e-textile active components was designed. This scheme makes it now possible to compare developments on basis of their integration level and therefore technical approaches. Five different integration levels have been established, products, patent applications and research were classified accordingly and examples were given for each integration level. Based on this, integration level 4 “textronics” was described and clear definitions were developed to define related components of integration level 4. Textronics as part of e-textiles are active components within smart textile systems. They are mainly fabricated on the textile substrate. This means that the electronic function is directly integrated in or constructed on the textile substrate. This textile structure can be planar (Integration level 4A), cylindrical (Integration level 4B) or on a material level (Integration level 4C). By classifying e-textiles, technologies can now be easily compared and obstacles to product development identified and discussed in relation to the e-textile’s integration level.

In addition to the technical aspect, the classification scheme facilitates better communication across this multi-disciplinary field, enabling specialists with different background knowledge to understand each other and discuss issues at the same technical level. As experience in project work (SMARTpro) shows, the integration level is always a discussion point in product development. The integration level determines development costs of new products to a large extent. Research and development (R&D) are one of the most expensive activities in developing new products. Starting product development at a lower integration level could reduce R&D expenses for the company. Therefore, in case companies wish to produce a product at integration level 4, the company must be aware

of the costs and time incurred in conducting research. This might not only be applied research but also elementary for example in layer deposition as demonstrated in Part II of this dissertation. Therefore, decision makers can easily be appraised of product development costs based on this original the classification scheme. In addition, researchers are able to use the scheme to justify approaches investigating higher integration levels. Finally, the classification might also be useful in terms of developing funding programs aiming to explore different integration levels. This would not only cover applied but also fundamental research.

11.2. Part II

Part II of this dissertation presents the development and characterization of a fibrous organic field effector transistor (OFET) The experimental work was structured according to the different layers applied successively onto a polyester filament using thin film technology. A polyester filament was copper-coated by electroless deposition, dip-coated in polyimide and subsequently in TIPS-pentacene, an organic semi-conductor. On top of this layered architecture, source and drain electrodes were deposited by a variety of techniques. Following the results are described per deposited layer.

i. Gate electrodes – conductive

The gate layer was deposited as discussed in literature onto a polyester filament with a diameter of 800 μm . Technical challenges have been identified due to the substrates' shape and dimensions. Measures for up-scaling the production of copper-coated polyester filaments per batch on lab scale were not successful. In this respect, different substrate holders used in the production process and during storage of the samples were investigated.

The sensitivity to degradation of the chemicals used in the coating process as well as the sensitivity to mechanical influences of the deposited layer was pointed out.

ii. Dielectric layer - insulating

Best results were achieved with a polyimide NMP dip-coating solution of 15w% and a dip-coating speed of 50 mm/min resulting in a layer thickness of 600 nm and good insulating properties (threshold $< 10^{10}$ Ωcm). To avoid phase separation and water penetration, drying in dry conditions ($< 5\%$ humidity) for a minimum of 7 h were found to produce optimal results. This meant that roughness and consequently thickness of the layer could be decreased.

Layer roughness was mainly influenced by the uptake of humidity in the layer when in liquid conditions. During water penetration, cavities developed increasing the thickness and roughness of the layer. The penetration of water was influenced by the choice of solvent in terms of its boiling point as well as the ambient conditions during drying of the dielectric layer.

With the above indicated deposition of polyimide solved in NMP a roughness of 34 ± 5 nm could be achieved. The roughness also was decreased by using the right drying conditions.

During dip-coating, it had been observed that the dried polyimide layer is sensitive to bending. Cracks were formed when the substrate leading to an increased number of closed circuits during electrical characterization of the polyimide layer.

iii. Active layer - semi-conductive

The semi-conductive layer was deposited by dip-coating the polyimide and copper coated polyester filament in 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-Pentacene) at a solution concentration of 2w%. To increase stability of the organic semi-conductor in solution, toluene was chosen as a solvent.

Different analysis techniques were tested. XRD was evaluated as a technique with high potential for analysing crystallinity in the deposited layer. Using XRD though is very time consuming. Therefore optical microscopy using polarised light was chosen as most adequate technique for analysing the layer's morphology with regards to its crystallinity. Regarding the analysis by optical

microscopy, a list of factor which could be influenced by varying the dip-coating speed was drawn up, e.g. size, distribution and shape.

Experiments confirm that crystallinity in the semi-conductive TIPS-pentacene layer could be influenced by rendering the drying procedure of the layer during solidification after dip-coating. Best results in matters of crystallinity within the layer were achieved when drying the layer at 60°C for 30 min in dry conditions combined with a second drying period of 60 min at ambient conditions in the dark.

The effect of dip-coating speed on the crystalline morphology was investigated. The dip-coating speed was varied from 1 mm/min up to 170 mm/min and clear changes in the crystal outline within the deposited layer were detected. Overall best results for the layer's crystal morphology were achieved at a dip-coating speed of 5 mm/min.

During electrical characterization of the layer, a new sample holder (transistor filament probe station) was developed. This holder ensured a link between electrical characterization techniques as applied in electronics and the cylindrical shaped textile substrate. With this setup the change in resistance of the deposited semi-conductive layer when applying a voltage at the gate layer was investigated. Unfortunately, the semi-conductive material did not change electrical properties once this electrical field was generated.

We inferred that the sensitivity of the organic material deposited under the above described conditions does still leave too much room for other factors influence the performance of the layer and therefore the device. The transistors in its current configuration did show a similar behaviour to a resistor.

Surprisingly, the leak current after deposition of the semi-conductive layer was increased if compared to being measured on the dielectric layer only. We also assumed that device composition i.e. the interaction between the various layers influence the behaviour of the semi-conductive layer. It remains unknown which factors had an

influence on the observed behaviour and further investigations are recommended.

iv. Source and drain electrodes – conductive

A range of deposition techniques were investigated for application regarding the TIPS-pentacene, polyimide and copper coated polyester filament. Due to the substrate cylindrical shape not all techniques were successfully applied.

Drop-casting with nano silver conductive jettable ink was assessed as the most suitable deposition technique to be applied on the filament. Acceptable to good results in matters of contact dimensions (size) and accuracy as well as with regard to time-savings and ease for application. Drop-casting is a technique in which a drop is manually applied onto the surface of the substrate and does not yield reproducible dimensions in matters of the shape of the electrode.

As silver does have a lower work function than the semi-conductor, the use of nano gold conductive ink might a better option. Unfortunately, gold has to be sintered at even higher temperatures (300°C) which might make it impossible to use if the organic semi-conductor is applied beforehand. Optional, a bottom-gate-bottom contact (BGBC) transistor architecture in which the semi-conductor is applied after the deposition of the contacts, could make the application of nano gold conductive ink more feasible.

11.3. Suggestions for further research

The experimental part in this dissertation generated an extensive list of problems to be resolved if a transistor fibre were be manufactured with the current technologies. As each layer was investigated in previous chapters and suggestions for improvements were made (see: chapters 7-10) suggestions will be made here, which major changes would need to be introduced to achieve a working transistor on a filament.

In this respect, the entire production process should be re-examined from the start to finish.

Even though a reliable copper coating was established in previous work, the process is still too sensitive and can easily be disrupted. Eventually a polymeric material which is already equipped with a conductive coating would be a solution in reducing production time. Eventually, as used by TU Darmstadt a polymer-coated glass fibre could be an interesting substrate to work with. Also instead of following the route of electroless deposition of copper, dip-coating in an organic conductive polymer PEDOT:PSS might be interesting to test.

During the experiments which were carried out for this study, it became evident that the top-electrodes are more important than previously assumed. If the contacts cannot be reliably applied on the cylindrical substrate in a way that suits not only the substrate but also the characterization instruments, none of the underlying layers are in position to be characterized electrically. The electrodes are a prerequisite for evaluating the function of the transistor as well as the quality of each individual layer.

Depending on the substrate, the coating processes as well as characterization techniques do vary greatly.

If the studies are continued on the cylindrical substrate type, working with a fibre-like substrate does seem to be the best choice, wires or filaments can be an option, too. Substrate diameter of 1000 μm proved to be a good size for applying the layers but also for characterization. Smaller diameters can be troublesome in microscopy and during dip-coating whereas bigger sizes might be difficult to cut which is a prerequisite for some characterization techniques.

If it is decided to change to a planar substrate type, it is recommended to apply technology used in the micro-electronics industry, i.e. slit-film technology. In slit-film technology, thin tapes are equipped with the active components by thin film deposition techniques. It is currently possible to produce these micro-electronic components on tapes. In comparison, the entire production process for micro-electronics on textile substrates or in particular, cylindrical

substrates requires re-development from scratch. Therefore, it is more likely that the textile industry might further process these tapes with a textile current production system. Necessary modification of the production chain can be achieved at lower costs and effort.

As has been described in previous chapters, there are a lot of obstacles to overcome to produce a working fibrous OFET. What should have become clear is that this scientific endeavour cannot be completed with the current setups available. Both, substrate and material do need special often custom-made accessories to make conducting experiments possible.

It is hoped that by identifying many remaining obstacles as well as finding resolutions to some of the problems mentioned, this study contributed successfully to the continuation of research with regard to fibrous organic field effect transistors.

A

Annex A: Project descriptions

A.1. Project description CleverTex

CleverTex



Funding scheme: Sixth Framework Programme

Proposal acronym: CleverTex

Grant agreement no.: FP6-2003-NMP-TI3-main

Starting date: 01/10/2005; closing date: 30/03/2008

CleverTex aims at develop a master plan and a framework for future actions in research, education and technology transfer in the fields of multi-functional intelligent textile materials in Europe for transforming the industry into a dynamic, innovative, knowledge-driven, competitive and sustainable sector by 2015.

Context:

In the EU 25, textile and clothing sector can be sum up in four figures:

- 4% of the total manufacturing production
- 7% of the manufacturing employment (2.9 million employees)
- 186, 000 companies (most of them are SME)
- 220 billion € of turnover

Even if this sector is still one of the mean industrial sectors in Europe, it has to face the relocation of production facilities to low-wage countries.

A way to fight against this phenomenon is to focus attention on products' functionality, flexibility and quality, and to develop SMART TEXTILE. That is to say, high value-added products.

That is why the new challenge for Europe consists in achieving a successful development of technologies and knowledge to be the leader of multifunctional intelligent textiles.

Objectives

CleverTex project aims to contribute to the economic and social progress in the European Union by transforming the industry into a dynamic, innovative, knowledge-driven, competitive and sustainable sector by 2015.

To that a master plan and framework for future actions in research, education and technology transfer in the field of multi-functional intelligent textile materials in Europe will be developed.

The objectives of this project are to:

- map the possible future technological developments in the intelligent textile sector from a socio-economic (non-technological) and technological perspectives
- prioritise these possible developments in the actual socio-economic environment (technology foresight)
- identify needs, breakthroughs and bottlenecks in order to answer to these developments
- help the transformation of the European Textile and Clothing industry

Project partners:

- Institut Français du Textile et de l'Habilliment, IFTH, France
- Scientific and technical centre of the Belgian Textile industry, CenTexBel, Belgium
- Ghent University, UGent, Belgium
- University of Lodz, ULodz, Poland
- Euratex, Euratex, Belgium
- Smartex, Smartex, Italy
- Verstraete-Hahn, BONFORT, Belgium
- Nota, Nota, Greece
- Alcatel, Alcatel, Greece
- Engineering Maille Technologie, EMT, France

A.2. Project description SYSTEX



Funding scheme: Seventh Framework Programme

Proposal acronym: SYSTEX

Grant agreement no.: 224386, THEME ICT-2-3-6 Micro/nanosystems

Starting date: 01/05/2008; closing date: 30/11/2011

Proposal full title:

Coordination action for enhancing the breakthrough of intelligent textile systems (e-textiles and wearable microsystems)

SYSTEX is an ICT project co-ordination initiative based on 12 partners from 5 European countries to build up a market-driven framework and orientation in the area of e-textiles and wearable micro systems.

SYSTEX aims at collecting technological and non technological information on relevant projects at various levels and classifies them in a transparent knowledge based information platform, structuring the relevant data of the entire e-textiles value chain according to the requirements of the interacting partners. The analysis of the available and ongoing research activities in e-textiles and wearable micro systems and the respective results will be edited in the framework of an interactive website and thus enhance cross-sectorial synergies and speed up the exchange of project results. Access to this new data pool shall be a true added value for every party involved in intelligent textile systems and offers a clear competitive advantage. The objective of SYSTEX is to identify the hurdles in the interdisciplinary knowledge transfer and to initiate actions to overcome them.

Systex has a strong market-driven focus and is geared to foster cooperation between the different knowledge carriers: industry, academic, government institutions, research & development and users of the technology.

SYSTEX aims at developing a framework for current and future actions in research, education and technology transfer in the field of e-textiles and wearable micro systems / electronics in Europe to support the textile industry in the most efficient and effective way to transform into a dynamic, innovative, knowledge-driven competitive and sustainable sector.

Project partners:

- Ghent University, Department of Textiles, BE
- Smartex s.r.l., Pisa, IT
- CEA, French Atomic Energy Commission, Grenoble, FR
- UNIPI, University of Pisa, IT
- CNR-INFM, National Institute of physics of Matter – National Research Council, Centre S3, Modena, IT
- IMEC, independent research center in nanoelectronics and nanotechnology, Gent, BE
- Philips Research department of photonic materials and devices, Eindhoven, NL
- Multitel, Mons, BE
- IFTH, Institut Français Textile et habillement, Lyon, FR
- Anne Demoor bvba, legal advisor, BE
- IHOFMANN, Wiesbaden, DE
- Plastic Electronics Foundation, Eindhoven, NL

A.3. Project description COLAE



Funding scheme: Seventh Framework Programme

Proposal acronym: COLAE

Grant agreement no.: unknown

Starting date: 01/05/2012; closing date: 31/08/2014

Europe's leading organisations have united to form COLAE – Commercialisation of Organic and Large Area Electronics – a project designed to simplify and speed up the commercialisation and adoption of organic electronics technology through the creation of industry clusters.

COLAE aims to raise awareness of the diverse range of applications utilising OLAE technology and to reduce the delivery time to market of these products while demonstrating the major business opportunities that can be explored and exploited, especially for SMEs across Europe.

As the organic and large area electronics market continues to grow and evolve at speed through the promise of new products, developed with lower cost, low energy processes using environmentally friendly materials, COLAE will provide European organisations access to an unparalleled knowledge base and the know-how to implement OLAE technology.

COLAE has harnessed the resources and expertise of its project partners and made it available to both the existing organic electronics industry and new organisations entering the market. Members can access high quality training and workshops, technical and business feasibility support, the best pilot production and manufacturing facilities, as well as gaining an opportunity to create regional clusters.

The project aims to connect all players within the industry to create and develop a dedicated supply chain that delivers tangible value and benefits. In addition, COLAE is focused upon engaging with end-

users of the technology and raising awareness among manufacturers of the potential applications of organic and large area electronics.

18 partners are committed to working together to develop and produce world class solutions for the benefit of all European businesses and organisations that are currently or could in the future utilise OLAE technology.

Through the creation and promotion of regional clusters – a regional cooperative entity with research, industry and government representation – represented by one of the project partners, COLAE will facilitate the sustainability of a strong European OLAE industry.

Project partners:

- VTT/PrintoCent:Finland, Oulu
- Plastipolis: France, Lyon
- CEA; France, Grenoble
- OES: Germany, Dresden
- InnovationLabs: Germany, Heidelberg
- Fraunhofer/EMFT:Germany, Munich
- Holst: Netherlands, Eindhoven
- KMC/Innovation Fab:Netherlands, Eindhoven
- CIKC: UK, Cambridge
- CPI: UK, Sedgefield
- CSEM: Switzerland, Basel
- CETEMMSA/PEC4:Spain, Barcelona
- AUTH: Greece, Thessaloniki
- Acreo: Sweden, Norrkoping
- Centi: Portugal, Famalicao
- StOLAE: Austria, Weiz
- IMSC: Belgium, Gent

A.4. Project descriptions SMARTpro



Project Acronym: SMARTpro – Smart Textiles and wearable Intelligence: from intelligent prototypes to industrial and practical products

Grant agreement no.: IWT 120779

Starting date: 01/10/2013; closing date: 30/09/2017

Major trade fairs are showing an increasing number and variety of smart textile and wearable intelligence prototypes for all kinds of applications that will eventually alter our lives.

Specialists consider safety and intervention, (home) care and medical, military, sports and leisure applications as the major growth markets for these products. The presence of (Flemish) companies on these markets is growing but they still encounter open questions and deficits.

Knowledge on smart textiles and wearable intelligence, industrial processing and communication possibilities, distribution channels, maintenance... are some of these issues.

By stimulating the collaboration across the ICT, electronic and textile sectors and confection companies by means of the collective project (Trajectory) SMARTpro we aim at supporting companies in application-specific product development and production.

We define smart textiles and wearable intelligence as the collection of (textile) materials and (textile-based) products incorporating one or more electronic components and/or communication capabilities.

In this context, Centexbel, Sirris, IMEC, HoGent, KHBO, DSP Valley, UGent, KULeuven and iMinds have initiated the SMARTpro project financed by IWT.

The project does not focus on the development of “new electronic systems or prototypes” but on the industrial processability and applications of smart textiles and wearable intelligence in:

- safety and intervention
- (home) care
- sports and leisure
- technical applications

Therefore, we choose to work exclusively with reliable and modular electronic systems and software. We are building on the knowledge already acquired in many European and other R&D projects.

Complex systems are therefore avoided. “Keep it simple” and “less is more” are guidelines determining the selection of e-systems and industrial application or assembling techniques.

Who are the end-users and industries who may benefit from mature smart textiles and wearable intelligence technologies?

The project involves companies (suppliers, manufacturers, process equipment developers.) from a variety of backgrounds, such as textiles, confection, ICT and electronics.

By simultaneously engaging the end-users and other actors (care providers, sports clubs, security services, intervention services, laundries, recycling companies...) in the project, we are also focusing on the users’ specifications and needs in the different application fields.

Belgian project partners:

- Centexbel
- Sirris
- DSP Valley
- IMEC
- UGent
- HoGent
- iMinds
- KULAB

Cretecs

B

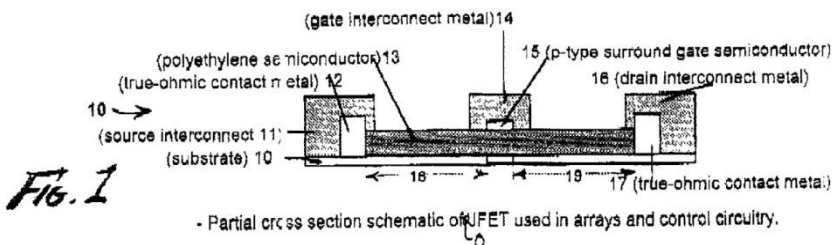
Annex B: Patent applications analysed

B.1. Examples of Integration Concepts in Patents at Integration Level 4A (fabric)

Woven or Ink Jet printed Arrays for Extreme UV and X-Ray Source and Detector

US20020008464

Filed 2001



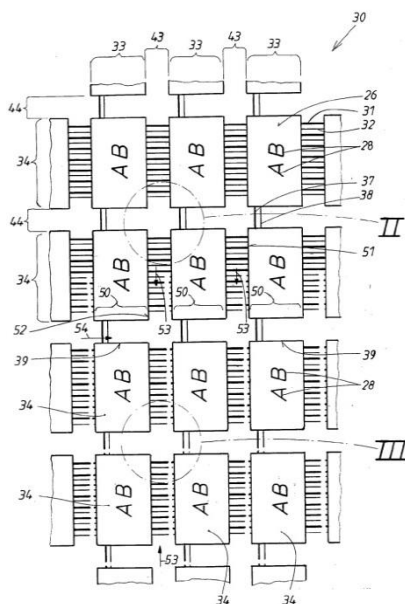
The device can sense and emit UV radiation (λ) at the range of 145 nm to 100 nm. The claims refer to the architecture only, as for the actual description of the production of the woven structure, they refer to an earlier patent (US09218233) which was published with the final

patent number US6229259 (as mentioned above).

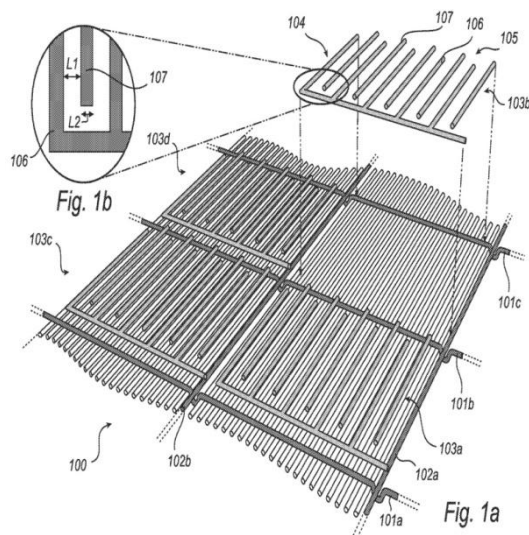
Verfahren zur Herstellung eines gewebten Etiketts (methods for producing a woven tag)

DE102004032569

filed 2005



The invention describes the general production method of woven tags with an intelligent add-on. In the woven structure, metalized yarns are introduced into the structure as weft insertion. Once the tags are cut apart, the ends of two conductive threads can be joined by soldering. If an increased temperature is applied to the structure, a thermoelectric voltage is generated which is then collected by other conductive threads. This thermovoltage can then be used to power a device.



In this arrangement the electrodes are arranged in a comb-like outline and the light is generated in the space between two adjacent conductive lines in one plane. The distance between the comb's digits (electrodes) can be adjusted from 50 to 200 μm allowing a voltage difference between the fields of less than 100 V. The electrodes themselves can be less than 50 μm in diameter to create the electroluminescent field. The overall structure is described as a matrix, a clear statement on the textile process to produce such matrix is not mentioned.

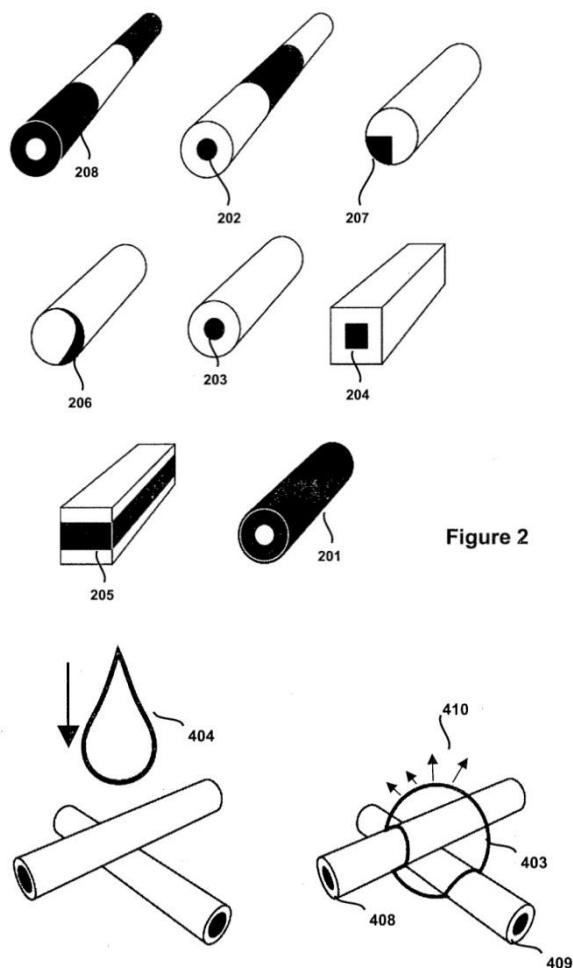


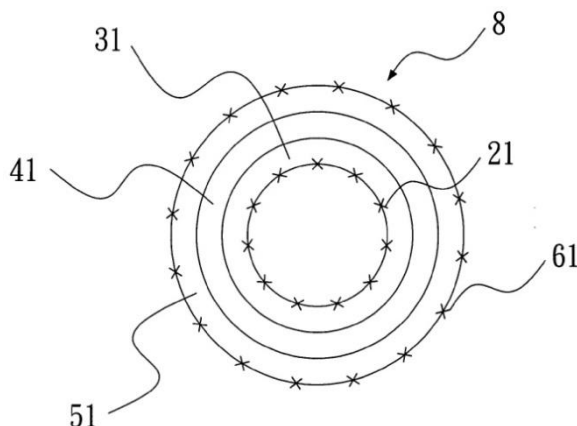
Figure 2

A variety of textile substrates like mono filament, hollow fibres, ribbons, yarns and bundles are addressed. All these structures partly consist out of electro-active material. Two fibres are interlaced, at the crossing point the function is generated, e.g. color change. As for components which use electrolyte at the junction of two fibres, an electro-chemical transistor, a field effect transistor as well as light emitting cells are mentioned. Furthermore, a number of textile integration techniques are listed as well as examples of all materials used in this composition are described.

Apparatus for Making Tubular Film Transistors

US20100108177

filed 2008



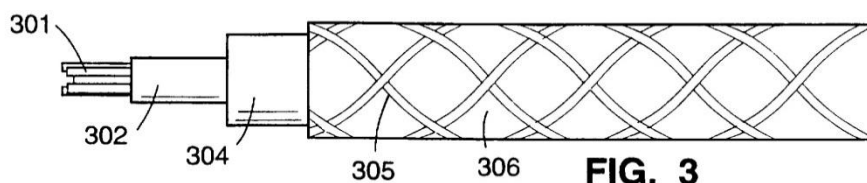
A complete new approach for making transistors is suggested. By weaving conductive fibres into a tubular structure the substrate is generated onto which the various layers are applied. A first and a second catalyst films, with a photo-exchange membrane in between, are applied. Finally, a second weaving process weaves conductive fibres into a tubular shape which is added as the outer layer of this architecture.

B.2. Examples of Integration Concepts in Patents at Integration Level 4B (filament, multiple parts)

Electroluminescent Filament

WO9724015

filed 1996



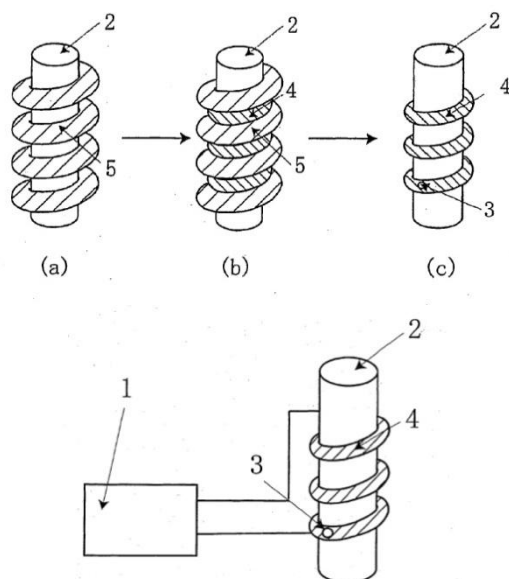
A conductive multifilament is surrounded by an insulating layer, following another conductive layer and a layer of electroluminescent phosphor. Optionally, another insulating layer can be applied on top of this construction into which the braided outer electrode is embedded, alternatively onto which the braided electrode is placed.

The braided outer electrode covers about 50% of the surface. This is only an example of the concept, material and architecture can be adapted accordingly.

Columnar Electric Device and Its Manufacturing Method

US20070108556

Filed 2007

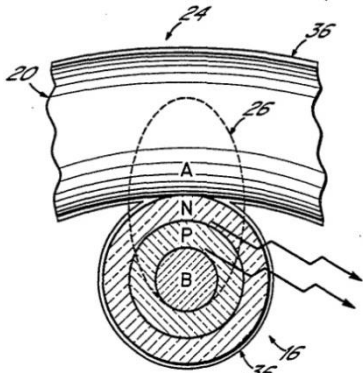
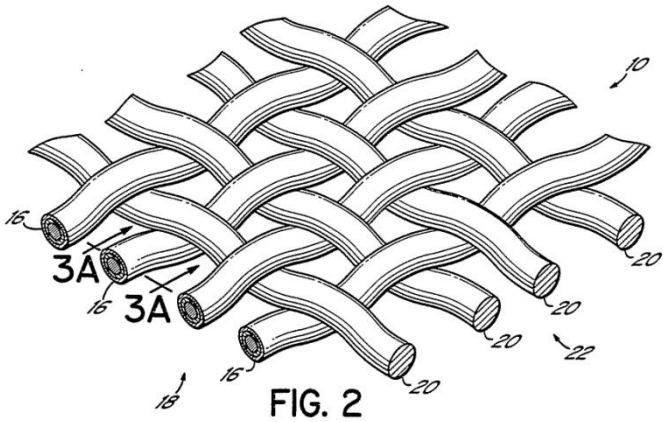


A sensor that is based on a columnar body is described. A semiconductor is applied onto the structure by vacuum deposition or coating with a melt, solution or gel. Following, a number of insulating wires is wrapped around this coated columnar core, of which some are removed after the process. The core is preferable made from fibres, besides others, polyester, polypropylene and nylon are options mentioned in the patent. The first wire removed, creates a space that is filled with copper by vacuum deposition. Aluminum will be deposited equally on the space when removing a second wire. The resistance between the two conductive spaces, silver (Ag) and copper (Cu), changes with the amount of light falling onto the semiconductor, thus an optical sensor is generated. By adding semi-conductive wires into the structure, different devices but also simple heat sensors can be build.

B.3. Examples of Integration Concepts in Patents at Integration Level 4B (filament, one parts)

Flexible Flat Color Display

WO0210809 | filed 2001

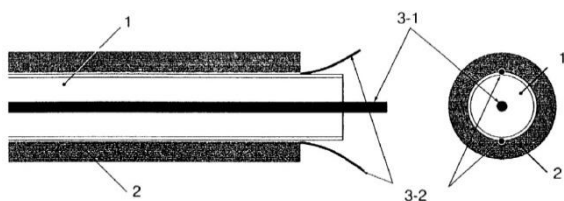


The woven structure includes a Light Emitting Diode Fiber matrix. This matrix is formed together with conductive fibres in weft direction, the fibre LED is positioned in warp direction. The LED fibre itself is made from a conductive core that is coated with a p-type semiconductor as well as with an n-type semiconductor of a light-emitting polymer.

Electroluminescence Fiber

US20020130624

Filed 2002

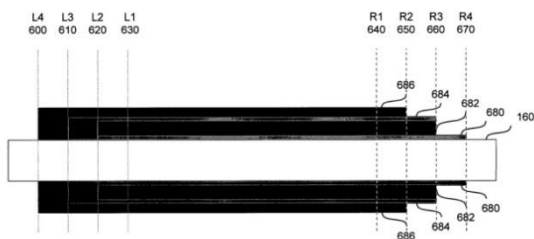


On two opposite sides of electroluminescent device as core of the structure, two electrodes are located; this entire structure is coated with thermoplastic resin, a thermosetting resin or a Ultraviolet-curing resin. The resin is shaped with respect of final application supporting mounting the EL fibre on wall surface or alike. The architecture can equally be applied on two separate electrode fibres which would lead to a classification in integration level 2B multiple, similar to patent WO9724015.

Thin-Film electrochemical devices on fibrous or ribbon-like substrates and method for their manufacture and design

WO03023880

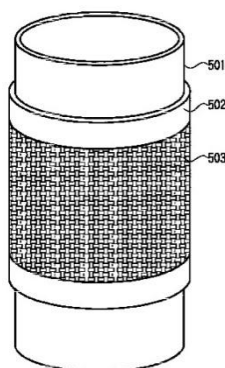
Filed 2002



This invention focusses on batteries on flexible, fibrous, ribbon-like structures whereas the suggested production methodology can be applied to a variety of devices. In reference to the variety of devices, also the materials which can be applied on the structure is huge e.g. semiconductor layer, optically transmissive layer, transparent conductive layers, etc. For evaporation of the material is suggested to use a tubular or hollow cylinder shadow mask.

Electronic Device Formed of Three-dimensional Textile Structure

20033309278 (JP)

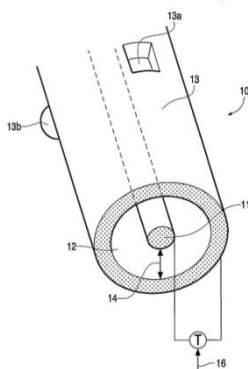


A cylindrical shape is the basis in this patent. It is understood that an insulating sheet is attached to the surface of the cylindrical textile structure, more information is not retrievable due to the language of the original document which is Japanese.

Electro-Optic Filament or Fiber

WO2004055576

Filed 2002



The filament core is surrounded by polarizable material and an outer electrode. This outer electrodes as well as the core are electro-conductive. Hence, applying an electrical potential, can generate an electrical field on the polarizable material. This material can have different functions, being e.g. change in color, polarization of reflectivity. The filament can be woven, knitted or crocheted.

Fiber Comprising and Integrated Electronic Component, Electronic Woven Material and use Thereof

WO02095839

Filed 2002

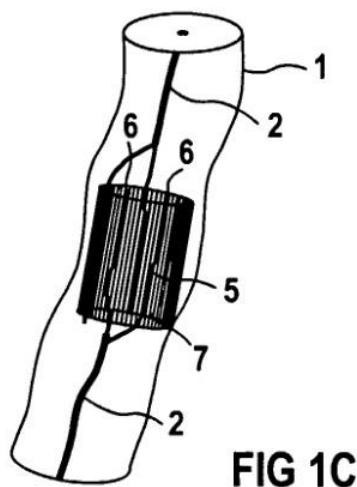


FIG 1C

The patent is suggesting the integration on fibre level by introducing electronic components. The fibre material itself serves either as conductive track, insulating or semi-conductive layer and therefore is essential element in the function of the device. Examples of electric component to be integrated are:

- Passive: resistors, capacitors, or coils,
- Active: diodes or transistors.

Since passive components are in the classification according to integration level of less importance, only active the components are reviewed. In the active component fibre, besides being the shell for integration of components, the fibre takes over a part in the architecture of the component. The production process of integration is not disclosed. Integrating the function during spinning the fibre might be an option.

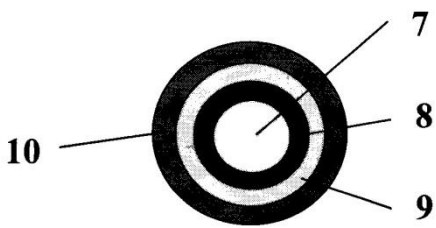
Translucent Conductive Wire-Shaped Material, Fibrous Phosphor and Woven Fabric Type Display Device

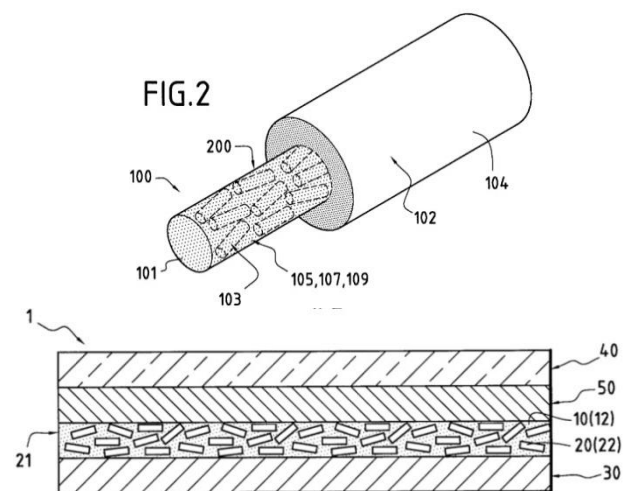
2002258775 (JP)

Filed 2001

No picture

The patent concentrated on the integration of displays into textile substrates. Electrical switches and LED fibres are produced and subsequently places into a woven structure.

<i>Textile Solarzellenanordnung</i> (Textile Photovoltaic Arrangement)	
DE10305162	Filed 2003
	
In this patent two concepts are described, the first was already explained in the previous section of Integration level 2C, here a composition of a PV on a single filament, a so-called lateral PV, is the focus. Conductive filaments are generated through galvanization of polyamide filaments with silver. Optional gold or platinum can be added in a subsequent process. The production process uses different fields of voltage and light detection to generate the patterned outline of the lateral PV.	

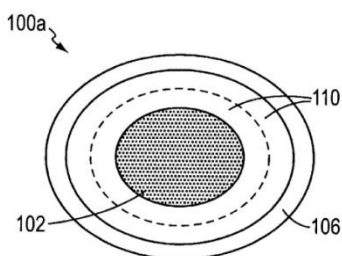
<i>Dispositif Comprenant Au Mains Un Type De Nanostrutcture Tubulaire Sous Forme de Fiber</i>	
2856197 (FR)	filed 2003
	
The patent presents the option for integrating nanotubes into a	

filament core. Carbon nanotubes are embedded in a polymeric matrix forming the fibre core. Additional layers are applied onto the core acting as electron donor or receptor thus generating the function of a photovoltaic cell

Photovoltaic Fiber

US20050040374

Filed in 2003

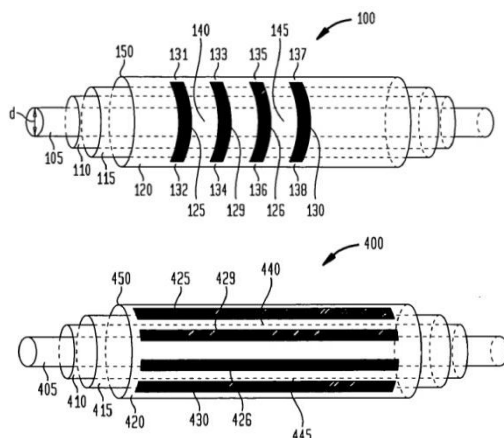


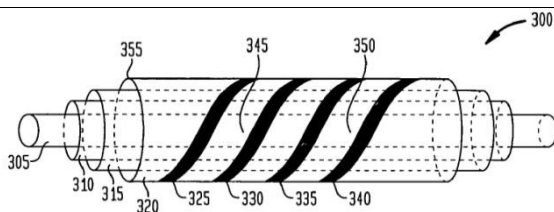
In the patent, photovoltaic material and methods of photovoltaic cell fabrication in form of a fibre are described. The electrical conductive core is surrounded by photoconversion material and a light transmitting electrical conductor (60%). The photoconversion material is composed out of photosensitized nanomatrix and a carrier material. As for the conductive cores, its shape is not limited to circular cross sections; square, rectangular, elliptical, etc. or any other irregular shape is suitable for application as core.

Polymeric Coatings and Methods of Making

US20050227059

filed 2004



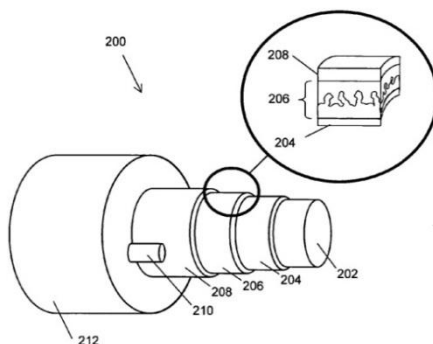


The architecture of a transistor is described. The core of the filament is of insulating nature. On this core, a gate electrode layer followed by a gate dielectric, a semiconductor as well as a patterned source/drain layer are applied. The source/drain electrodes are evaporated through a mask in either perpendicular or longitudinal or even diagonal direction. The gate dielectric is made from different materials, one option is polyimide and therefore might be of particular interest in the experimental part of this thesis. Also the US patent US7385220 filed in 2004, with the title *Fiber Having Dielectric Polymeric Layer on Electrically Conductive Surface*, elaborates on the topic.

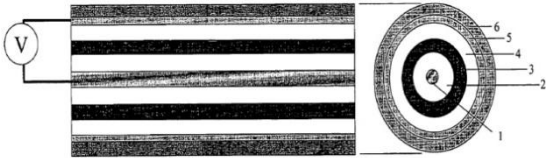
Organic Devices Having a Fiber Structure

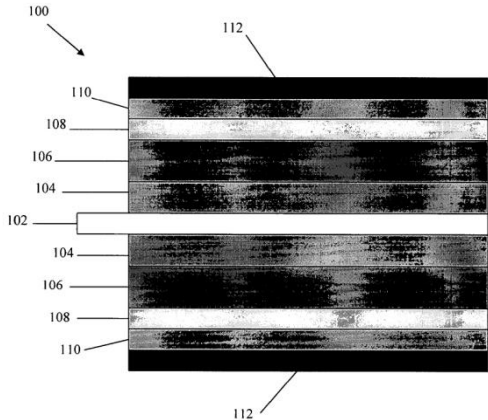
US20060013549

filed 2004



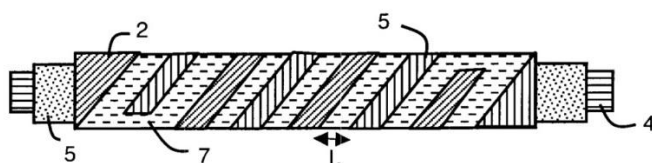
A photovoltaic fibre and the method to manufacture such a fibre are disclosed. In this concept, the core is of conductive material representing the first electrode. A semi-conductor surrounds the electrode. Following, a transparent second electrode is applied, and optionally, also additional layers such as blocking layer or smoothing layers can be applied. The core can be a nylon fibre, a metallic or an optical fibre. Alternatively to said second electrode layer, an auxiliary conducting fibre can be wound around the coated core substituting the second electrode.

<i>EL Fiber and Photocatalyst Reaction Vessel</i>	
20070126341	filed 2004
	
Also in this architecture, the core of the EL fibre is composed out of conductive material that is surrounded by insulating and active layer. The outer electrode completes the structure.	

<i>Organic Optoelectronic Devices and Applications thereof</i>	
WO2007130025	Filed 2006
	

The patent suggests the concept of a photovoltaic device with a fibre core. Surrounding layers are an transmissive first electrode, a photosensitive organic layer and a second electrode layer. Materials used within the concept are for instance metallic or of organic kind. In particular, polymeric materials are mentioned. This invention is further elaborated on in the PCT patent WO2007130972, filed in 2006, *Fiber Photovoltaic Devices and Applications Thereof*.

<i>Transistor Effet De Champ Forme Sur und Fiber et Procede de Realisation</i>	
FR2922684	filed 2007

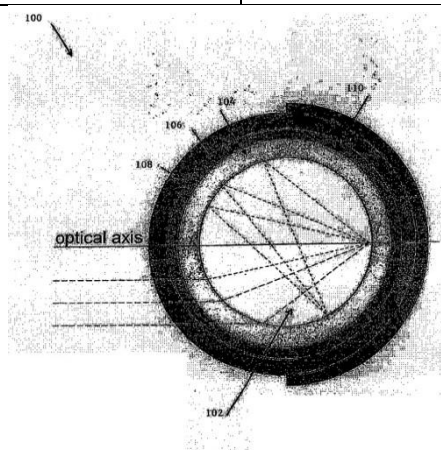


The concept of using a multiple times coated fibre core is also elaborated on in this patent. The invention addresses the placement of the top electrodes (source and drain) in particular. A preceding patent (US20050253134) points at different outlines for the application of two electrodes. The patent suggests two methods: longitudinal or perpendicular to the fibre axes. Creating the channel in transversal direction or in fibre direction. The French patent though suggests creating the two electrodes as a double-helix around the fibre.

Lateral Organic Optoelectronic Devices and Applications Thereof

WO2009059303

Filed 2008

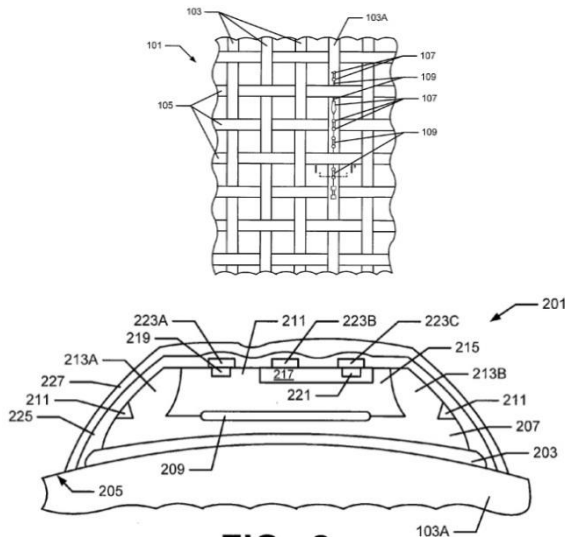


An optical fibre core is the basis in this architecture for building a photovoltaic (PV) cell or electromagnetic coil. The fibre core is coated with a radiation transmissive first electrode, an active layer (photosensitive) and a non-radiation transmissive second electrode. As had in previous patents, material and dimensions are variable.

Deposition of Electronic Circuits on Fibers and Other Materials

US20090053950

Filed 2008



The concept of placing the microelectronic component directly on a fibre is described. It could be argued that this invention should be classified in integration level 3 onto, but because of the inseparability of the fibre and the device, the integration level set to 2B single. The electrical component is directly formed on the fibre surface which then can be integration into e.g. woven structures representing the circuit. As in previous concepts different layers are deposited onto the fibre sequentially. Opposite to these previous patents, the layer formation is located mainly on the “top” of the filament, i.e. is not circumferential. The components itself are manufactured with conventional circuit fabrication technologies. Circumferential application of the material is preferred. A protective layer and a shielding layer prevent from damages or interference in the operation of the transistor’s function.

B.3. Complete list of patents analyzed

Title	number
Integrated Light Emitting Device	US5546413
Textile Light System	GB2396252
Electrochemical Process For the Production Of Conducting Polymer Fibers	US 1995/5423956
Process for Producing Thin Layers of Conductive Polymers	US 1996/5498761
Textile Fabric with integrated sensing device and clothing fabricated thereof	US 2000/6080690
Soluble Polyimide Resin, Process For Preparing the same, and Polyimide Resin Solution Composition	US 2000/6100365
Flexible Panel Display Having Thin Film Transistors Driving Polymer Light Emitting Diodes	US 1998/5747928
Light-Emitting Element and Device	US20060250075
Line Element and Method of Manufacturing the line Element	US20050253134
Columnar Electric Device and Its Manufacturing Method	US20070108556
Fiber Based Electric Device	US20090103859
Fiber Based Electric Device	US20110308077
Apparatus for Making Tubular Film Transistor	US20100108177
Deposition of Electronic Circuits on Fibers and other Materials	US20090053950
Dispositif Comprenant Au Moins Un Type De Nanostructure Tubulaire Sous Forme De Fibre	2856197
EL Fiber and Photocatalyst reaction Vessel	US20070126341
Electroluminescence Fiber	US20020130624
Electro-optic Filament or Fiber	WO2004055576
Fiber Having Dielectric Polymeric Layer on Electrically Conductive Surface	US7385220
Fiber with Polymeric Coatings and Methods of making the Same	US20050227059
Fibril Solar Cell and Method of Manufacture	US20050194035
Flexible Flat Color Display	WO0210809
Organic Devices Having A Fiber Structure	US20060013549

Title	number
Organic Optoelectronic Devices And Applications Thereof	WO2007130025
Photovoltaic Fibers	US20050040374
Transistor A Effect De champ Forme Sur Une Fiber Et Producede De Realisation	2922684
Textile Solarzellenanordnung	DE10305162
Electronic Circuitry Integrated in Fabric	WO2008066458
Photovoltaic Device	US20100000599
Photovoltaische Einrichtung	DE102006047045
Pixelated Electroluminescent Textile	WO2008001250
Verfahren zur Herstellung eines gewebten Etiketts	DE102004032569
Woven or Ink Jet Printed Arrays For Extreme UV and X0Ray Source and Detector	US20020008464
Illuminating Textile Article	US20100259925
Lichtemittierende Anordnung	DE10323472
Intelligent Textile Technology based on Flexible Semiconductor Skins	US2006255433
Method for Electrically Connecting and Elctrical Conductor to an Electronic Component, and Device	WO 2005/067042
Flexible Electrochromic devices, electrodes therefor, and Methods of Manufacturing	US20100245971
Antistatische Schutzbekleidung	DE 44 02 578
Verfahren zur Herstellung von metallisiertem textilem Flaechengebilde, metallisiertes textiles Flaechengebilde und Verwebung des so hergestellten metallisierten textilen Flaechengebildes	DE 10 2005 062 028
An Apparatus Comprising Electronic and/or Optoelectronic Circuitry and Method for Realizing said Circuitry	WO 2000/67539
Conductive (Electrical, Ionic and Photoelectric) Membrane articlars, And Method for Producing the same	US 2001/0045547
Conductive Composite Material and Method for Manufacturing the same	WO 2007/114645
Electrically Conductive Elastic Composite Yarn, Method for Making the same, and Articles Incorporating the same	WO 2004/097089

Title	number
Electroconductive Fiber, a fiber Complex Including an Electroconductive Fiber and Methods of Manufacturing the same	US 2011/0204297
Elektrisch leitfaehiges Garn	DE 10242785
Energy Active Composite Yarn, Methods for Making the same, and Articles Incorporating the same	WO 2007/020511
Fabric, a Device with Fabric and a Manufacturing Method for Fabric	US 2011/0217892
Gewebe, Vorrichtung mit Gewebe sowie Herstellungsverfahren fuer Gewebe	DE 10 2009 033 510
Konzentrationssystem zur Buendelung von Sonnenlicht auf photoaktive Polymere	DE 10 2007 008 875
Metal Coated Nano Fibers	WO 2005/021845
Method for Producing Conducting Polymer Fibers with Vinyl and Conducting Polymer Fibers with Conducting Polymer Fibers with Vinyl Produced Thereby	US 2005/0287366
Method for Producing Electrically Conductive, Flexible Flat Materials	WO 2005/020246
Method for Producing metalized textile fabric, metalized textile fabric, and use of the metalized textile fabric thus produced	WO 2008/155350
Method for Producing metallised Textile Surfaces Using Electricity0Genrating or Electricity0consuming elements	WO 2008/101917
Method for Producing Planar Metallised Textiled Textile Planar Metallised Textile Structure and Use of the thus Produced Planar Metallised Textile Structure	US 2009/0011674
Methods and Systems for slectively Connecting and Disconnecting Conductors in a Fabric	US 2003/0129905
Multi-Layer Woven Fabric Display	WO 2009/050629
Plural Layer Woven electronic Textil, Article and Method	US 2003/0211797
Elektrisch beheizbares Flaechengebilde	3433437
Woven Electronic Textile, Yarn and Article	US 2004/0009729
Method and Apparatus for Attaching Chip to a Textile	US 2010/0071205

Title	number
Process for Producing Transparent Conductive Films, Transparent Conductive Film, Process for producing conductive Fibers, Conductive Fiber, carbon nanotube/Conductive Polymer Composite Dispersion, Process for Producing Carbon nanotube/Conductive Polymer Composite Dispersions, and Electronic Device	US 2012/0145968
Conjugated Polymer Fiber, Preparation and use Thereof	WO 2006/084088
Electrospinning Ultrafine Conductive Polymeric Fibers	WO 2001/51690
Fabrication of Patterned Nanofibers	US 2011/0300347
Methods of Fabricating Nanostructures and Nanowires and Devices Fabricated Therefrom	WO 2002/080280
Methods For Controlling The Crystalline nanofibre Content of Organic Layers Used in Organic Electronic Devices	EP 2 200 103
An Organic Field Effect Transistor	WO 2008/090257
Biofabrication of Transistors Including Field Effect Transistors	US 2006/0052947
Donor Sheet, Method of Manufacturing the same, Method of Manufacturing TFT using the Donor Sheet, and Method of Manufacturing Flat Panel Display Device using the Donor Sheet	US 2005/0191448
Electrically Traceable and Identifiable fiber optic cables and connectors	US 2008/0273844
Electrochemical Device	WO 2002/071505
Electrochemical Device	US 2004/0211989
Electronic Assembly/System With Reduced Cost, Mass, And Volume And Increased Efficiency And Power Density	US 2008/0032461
Film Comprising Substrate-Free Polymer Dispersed liquid Crystal; Fiber, Fabric, and Device thereof and methods thereof	US20100279125
Function Element, Storage Element, Magnetic Recording Element, Solar Cell, Photoelectric Conversion Element, Light Emitting Element, Catalyst Reaction Device, and Clean Unit	EP 1 804 300
Method of Producing Devices Having Nanostructured Thin-Film Networks	US 2007/0120095

Title	number
Nanoscale Wires and Related Devices	US 2003/0089899
Organic Sensor Device And Its Applications	US 2010/0028209
Procedure For The Use of natural Cellulosic Material, Synthetic Material or mixed natural and synthetic material, simultaneously as physical and dielectric support in self-sustainable field effect electronic and optoelectronic devices	WO 2009/130551
Wrapped Optoelectronic Devices and methods for Making Same	US 2010/0313944
Elastic Conveyor Belt with Conducting Fibers for the Discharge of static Electricity and Leather Perching Machine Comprising such Belt	WO 2000/73177
Organic Sensor Device And Its Applications	EP 2091093
System, Method, and Computer Program Product for Textile Structured Waveguide Display and Memory	US 2005/0201674
Textile-Based Electrode	US 2006/0211934
Testing Electronic Textiles During Assembly and Electronic Textile Displays	US 2008/0182475
POD for Mounting Electronic Device to Footwear	EP 1 107 065
Semiconductor Device and manufacturing Method of the same	US 2010/0072583
Transistor a Source et Drain Filaires	EP 2 209 146
Fiber Photovoltaic Devices and Applications Thereof	WO2007130972
Fiber Photovoltaic Devices and Methods For Production Of Thereof	WO2009154986
Lateral Organic Optoelectronic Devices and Applications Thereof	WO2009059303
Thin-Film Electrochemical Devices on Fibrous or Ribbon-like Substrates and Method for their manufacture and Design	WO2003023880
Fiber Comprising an Integrated Electronic Component, Electronic Component, Electronic Woven Material, Production Method and use thereof	WO2002095839
Drapable Liquid Crystal Transfer Display	WO2005072455
Submount for Electronic Components	WO 2008/007237

Title	number
A Fully Textile Electrode Lay-Out Allowing Passive and Active Matrix Addressing	WO 2006/129272
Electrical Components and Circuits Constructed as Textiles	WO 2005/083164
Fabric and Yarn Structures for Improving Signal Integrity in Fabric Based Electrical	WO 2004/003273
Fabric or Garment with Integrated Flexible Information Infrastructure	WO 1999/64657
Silk Electronic Components	WO 2011/130335
Smart Skin Array Woven Fiber Optic Ribbon and Arrays and Packaging Thereof	0 506 298
Textile for Connection of Electronic Devices	WO 2008/044167
Textile for Connection of Electronic Devices	WO 2008/044202
Textile-Based Electronic Device and Manufacturing Method Therefore	WO 2009/037667
Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors and Fabricating Such Device	WO 2002/17362
Electrically Conducting And optically Transparent Nonwire Networks	WO 2008/127313
System and Process for Producing nanowire Composites and Electronic Substrates	WO 2005/017962
The Fabrication and Application of Nanofiber Ribbons and Sheets and Twisted and Non-twisted Nanofiber Yarns	WO 2007/015710
Silk Transistor Devices	WO2011026101
Apparatus, Method, and Computer Program Product For Unitary Display System	WO 2005/076714
Dye sensitized Solar Cell Based on Electrospun Ultra0fine Titanium Dioxide Fibers and Fabrication Method Thereof	EP 1 528 579
Electronic Assembly/System With Reduced Cost, Mass, And Volume And Increased Efficiency And Power Density	WO 2004/019657
Nanoelectronic devices based on nanowire networks	WO 2005/023700
Fabric or Garment with Integrated Flexible Information Infrastructure	WO 1999/64657

Title	number
Apparatus, Method, and Computer Program Product for Structured Waveguide including Recursion Zone	WO 2005/076722
System, Method, and Computer Program Product for Textile Structured Waveguide Display and Memory	WO 2005/076720
Physiological Monitoring Garment	EP 2 289 407
Apparatus, Method, and Computer Program Product for Substrated/Componentized Waveguided Goggle System	WO 2005/076721
Process For Using And Producing Paper Based On Natural Cellulose Fibers, Synthetic Fibers or Mixed Fibers as Physical Support and Storing medium For Electrical Charges in SelfSustaining FiledEffect Transistors with Memory Uding Semiconductor Oxides	WO 2009/115913
System and Process for Producing nanowire Composites and Electronic Substrates	WO 2005/017962
Apparatus, Method, and Computer Program Product for Substrated/Componentized Waveguided Goggle System	WO 2005/076721
Fiber Photovoltaic Devices and Applications Thereof	WO2007130972
Fiber Photovoltaic Devices and Methods For Production Of Thereof	WO2009154986
Lateral Organic Optoelectronic Devices and Applications Thereof	WO2009059303
Thin-Film Electrochemical Devices on Fibrous or Ribbon-like Substrates and Method for their manufacture and Design	WO2003023880
Fiber Comprising an Integrated Electronic Component, Electronic Component, Electronic Woven Material, Production Method and use thereof	WO2002095839
Drapable Liquid Crystal Transfer Display	WO2005072455
Silk Electronic Components	WO 2011/130335
Wrapped Solar Cell	WO2009012465
Submount for Electronic Components	WO 2008/007237
Electrical Components and Circuits Constructed as Textiles	WO 2005/083164

Title	number
Fabric and Yarn Structures for Improving Signal Integrity Signal Integrity in Fabric Based Electrical Circuits	WO 2004/003273
Textile for Connection of Electronic Devices	WO 2008/044167
Textile for Connection of Electronic Devices	WO 2008/044202
Textile-Based Electronic Device and Manufacturing Method Therefore	WO 2009/037667
Inorganic Nannowires	WO 2005/067683
The Fabrication and Application of Nanofiber Ribbons and Sheets and Twisted and Non-twisted Nanofiber Yarns	WO 2007/015710
Silk Transistor Devices	WO2011026101
Apparatus, Method, and Computer Program Product For Unitary Display System	WO 2005/076714
Dye sensitized Solar Cell Based on Electrospun Ultra0fine Titanium Dioxide Fibers and Fabrication Method Thereof	EP 1 528 579
Electronic Assembly/System With Reduced Cost, Mass, And Volume And Increased Efficiency And Power Density	WO 2004/019657
Nanoelectronic devices based on nanowire networks	WO 2005/023700
Apparatus, Method, and Computer Program Product for Structured Waveguide including Recursion Zone	WO 2005/076722
System, Method, and Computer Program Product for Textile Structured Waveguide Display and Memory	WO 2005/076720
Physiological Monitoring Garment	EP 2 289 407
Apparatus, Method, and Computer Program Product for Substrated/Componentized Waveguided Goggle System	WO 2005/076721
Active Devices Using Threads	US6437422
Thin Film Transistors with Organic0Inorganic Hybrid Materials as Semiconducting Channels	US 2001/6180956
Woven Circuit Device	3479565
Transistor with Wire Source and Drain	KR20100084113
Electrically Active Textiles and Articles made therefrom	US 2001/6210771

Title	number
Woven Polymer Fiber Video Displays with Improved Efficiency and Economy of Manufacture	US6229259
Procedure For The Use of natural Cellulosic Material, Synthetic Material or mixed natural and synthetic material, simultaneously as physical and dielectric support in self-sustainable field effect electronic and optoelectronic devices	WO 2009/130551
Procedure For The Use of natural Cellulosic Material, Synthetic Material or mixed natural and synthetic material, simultaneously as physical and dielectric support in self-sustainable field effect electronic and optoelectronic devices	WO 2009/130551
Electronic Paper Device and Manufacturing Method thereof	US 2011/8040460
Intelligent Textile Technology based on Flexible Semiconducting Skins	US 7348645
Miniature Fiber Radio transceiver and related method	US 2008/8503949
Elektrisch leitend beschichtetes Siebdruckgewebe sowie Siebdruckanordnung	DE 20 2008 017 480
Electroluminescent Filament	WO9724015
Electronic Device Formed of Three-Dimensional Textile Structure	2003309278
Translucent Conductive Wire-Shaped Material, Fibrous Phosphor and Woven Fabric Type Display Device	20022258775
Electroconductive yarn for e-textile and woven or knitted fabric using the same	2011/074512
Woven Interconnection Structure	3631298
Electronic Fiber or Electronic Yarn and Fiber Product Using the same	2007/314925
Method and Apparatus for Making Conductive Yarns	US 1989/4813219
Textile Fabric with Integrated Electrically Conductive Fibers and Clothing Fabricated Thereof	US 2000/5906004
Wiring Structure, Magnetic Head for Printer and Magnetic-Head Printer Using the same	02185453

Title	number
Cloth Having Durable Antistatic Properties for use in Garments and Underwear	3586597
Conductive Wrist Band	US 1987/4654748
Crocheted Fabric Elastic Wrist Bracelet Bearing an Interior Conductive Yarn	US 1989/4878148
Polyaniline Compositions, Process For Their Preparation and Uses Thereof	WO 1991/05979
Manufacture of Polyimide Film by Solvent Casting	US 1987/4405550
Electronic Clothes	2005146499

C

Annex C: Copper layer deposition

C.1. Polypyrrole coating procedure on PES

1. Preparation of Substrate

Cut PES filament substrate to a length of 5 cm

Remark: The substrate material has been stored on a small weaving frame to straighten the filament. When the substrate was placed onto the frame, it has been treated with a hot air gun to ensure proper straightening of the filament. For practical reasons it is easier to handle the substrate if it is as straight as possible.

2. Cleaning of Substrate (IPA + NaOH bath)

Step 1: Iso-Propanol (IPA)

Clean fibre with IPA by pouring it over the fibre which is placed on a paper tissue to collect excess liquid.

Step2: NaOH

- Boil tap water for making a water bath with water kettle. Pour boiled water into huge beaker. Prepare NaOH solution in measuring cylinder (or preferably a short cylinder/glass container should be used for easy access to fibre after washing)

As for the NaOH solution, it is necessary to prepare a 2M NaOH solution containing:

1000ml:

50% NaOH: 105.6 ml / 1 L

100ml:

50% NaOH: 10.56 ml = 10 ml + 560 μ l

+ fill up with distilled water

(remark: here high accuracy is not required)

To obtain 1liter of a 2M NaOH solution, it is needed to give 105.6 ml of 50% NaOH in a glass beaker and fill up with distilled water till the 1 liter mark is reached. After the preparation of the solution, the yarn must be put in this solution for

- 30 minutes
- at the temperature of 80°C,

3. Rinsing of cleaned Substrate (distilled H₂O)

After the washing step, the yarn must be rinsed with distilled water and must be dried (with a hair dryer)

This rinsing step should be completed in a beaker filled with distilled H₂O, to avoid the mechanical impact of running distilled water (from the tap).

4. Polymerization (PPy bath)

Preparation of the Pyrrole solution in volumetric flask

For the polymerization reaction, first a 0.04M Py solution is needed:

100ml:

Py: 283 µl Py + fill up with distilled water

1000 ml: Py: 2.830 ml/L

25 ml: Py: $(2.830:10:4) = 2.830:40 = 0.0707$

+ fill up with distilled water

It is necessary to use 2.380 ml of Py and fill up with distilled water till we have 1 litre in the slops (Py must be well mixed with water). After that the yarn needs to be placed in this solution for

- 1 hour
- at room temperature.

After adding Py to H₂O, the solution needs to be shaken to ensure homogeneity, then it is poured into a beaker and the substrate is added.

Preparation of the FeCl₃ – BSA

The second solution for the bath is prepared in a volumetric flask and contains:

100 ml:

FeCl₃: 2.57061 g

BSA: 0.21526 g

1000 ml: FeCl₃: 25.7061 g/L; BSA: 2.1526 g/L

25 ml: 25.7061: 40 = 0.642 g; 2.1526:40 = 0.0538 g

+ fill up with distilled water

For 1000 ml, it is imperative to weight out 25.7061 g/L of FeCl₃ (iron chloride) and 2.1526 g/L of BSA (benzene sulphoric acid) and dissolve them in 1 liter of distilled water. This solution must be added to the yarn in the Pyrrole solution and the polymerization must go on for

- at least **180 min**
- at 5° C (fridge).

After adding the chemical and H₂O, the solution needs to be shaken for homogeneity, then it can be poured into the beaker which already contains the PPy solution and substrate.

The solution should be shaken gently after half of the time.

The polymerization can be stopped by taking the yarn out of the solution, when the color of the solution and of the yarn changed into a very dark greenish color.

(Waste: put rest solution into tank for pyrrole (Py) solution mix)

Rinsing

The Polypyrrole coated yarn must be rinsed with distilled water (in beaker to avoid mechanical impact of running water) until no coating residues are remaining on the yarn and the rinsing water appears clear in color. The coated substrate needs to be treated gently!

Rinse glass with rest of NaOH solution (overnight)

Drying

After rinsing, it is crucial to dry the coated substrate

First with paper (selectively to remove residues) and subsequently, with a hair dryer

Finally the coated substrate is placed into the oven

- at 40° C
- for 24 hours

Additional information:

Why do we coat the fabric first with PPy?

Previous experiments showed that an immediate deposition of copper on the fabric did not work out. However, for PPy coated surfaces it worked out. A possible explanation for this behavior might be that the nitrogen centers in the pyrrole structure act as an acceptor for growing the copper layer on it. Nitrogen has a great affinity to metals.

The pyrrole compound in the aqueous solution is oxidised and adsorbed to the textile surface to form a conductive polymeric film when in contact with a textile substrate.

BSA	doping agent, counter ion; needs to be added as only the doped polypyrrole is electrically conductive
Ferric chloride	oxidising agent (includes compounds of polyvalent metal ions, which means that it is capable of changing its valence) the amount of oxidising agent is a controlling factor in the polymerisation rate
Reaction temperature	at 5°C, the reaction takes place slower, but a higher degree of order (arrangement of pyrrole monomers on the textile surface) is achieved
pH	the ph of the solution should be between 1-3
Ultrasonic treatment	There is a difference between the concentration of the adsorbed species on the textile surface and the concentration of the species in the liquid phase exposed to the textile; the difference in concentration and deposition rate depends also on the available surface area of the textile and the amount of pyrrole polymer in the vicinity of the textile

Role of the PdCl₂/SnCl₂ solution

Before we can start with the copper deposition on the PPy fabric, the surface needs to be activated via chemisorption¹ of palladium. The

palladium centers which were created on the polypyrrole surface, form active sites, as it is illustrated in the following drawing:

Direct chemisorption of palladium at polymer surfaces is not possible; therefore the surface needs to be sensitized with a tin compound. The created seed layer of tin centers initiates the chemisorption of palladium, which in turn is used as a seed layer for the copper deposition.

After the sensitization/activation of the PPy coated fabric with palladium and tin, HCl is applied in order to remove the tin centers which were not replaced by palladium during the previous step.

Tasks of the different chemicals in the copper plating solution

CuSO ₄	to supply copper ions
Rochelle salt (sodium potassium tartrate tetrahydrate)	to complex the Cu ²⁺ and to prevent precipitation of Cu(OH) ₂
NaOH	to make HCHO effective as a reducing agent
HCHO	to reduce Cu ²⁺ -ions

Reaction mechanisms of the copper plating

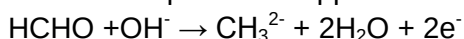
Formaldehyde oxidation reactions



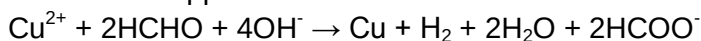
This reaction occurs on palladium.



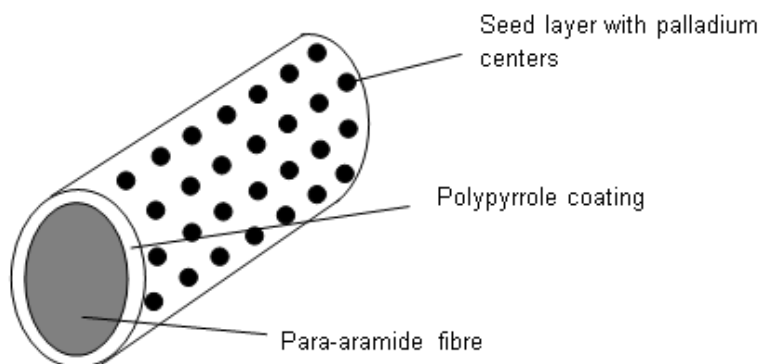
This reaction takes place on copper



Plating reaction of copper



Reduction of Cu²⁺ to metallic copper



C.2. Electroless deposition of copper on PPy modified PES filaments

1. Cleaning of substrate

To remove dust from drying procedure in oven, rinsing should be completed in a beaker, subsequent drying with hair dryer.

2. Preparation of the sensitization & activation solution

The solution should be prepared in a volumetric flask and contains:

500 ml:

PdCl₂: 0,5 g
HCl (37%): 30 ml
SnCl₂: 11 g

1000 ml:

PdCl₂: 1 g/L
HCl (37%): 60 ml/L
SnCl₂: 22 g/L

In a first step, 1 g of PdCl₂ is dissolved in 60ml of HCl (37%), which takes a few hours.

After that 22 g of SnCl₂ is added with 500 ml of distilled water. It is imperative to wait till the color of the solution has changed from dark greenish into dark brown, which takes 1-2 days (the longer the better. When the color has changed, add distilled water till 1liter is obtained.

3. Activation & sensitization of the PPy coated yarns

Immerse the yarn in the sensitization and activation solution for 20 min at room temperature. (Currently, the solution dated 12.08.2013 is used.)

In the meanwhile, prepare the copper plating solution:

100 ml:

CuSO₄: 1 g

Rochelle salt: 5 g

NaOH: 1 g $\rightarrow$ 1.3202 ml $>$ 1320,2 μ l

HCHO: 0.5 g $\rightarrow$ 12.478 ml/L $>$ 1247.8 μ l

1000 ml: CuSO₄: 10 g/L; Rochelle salt: 50 g/L ; NaOH: 10 g/L
 $\rightarrow$ 13.202 ml/L;

HCHO: 5 g/L $\rightarrow$ 12.478 ml/L

Dissolve CuSO₄ and Rochelle salt in water (this takes some time),

later add NaOH.

add HCHO and the necessary amount of distilled water to reach 1liter

just before the plating!

4. No Rinsing

Rinsing of the substrate has been skipped for further coating procedures. It has been tested that rinsing does not have any effect in this step. Remove the fibres from Pd solution, place on paper tissue to remove excess solution, then put into HCl solution

5. Acceleration

Perform the acceleration step by dipping the yarn in a 1% solution of HCl (37%) for 1 min. Wash the yarn subsequently again in a beaker with distilled water (gently!).

Rest of solution needs to be added into chemical waste container (HCl acid).

Prep of HCl solution 1%, based on 37% solution

>>> 360 ml H₂O distilled, 10ml of HCl 37 %

After this, rinse in H₂O distilled beaker, place on paper to remove excess liquid, then distribute into glass test tubes (1-2 per tube to avoid mechanical influence during coating)

6. Copper plating

Immerse the catalyzed and accelerated yarn in the plating bath solution.

Electroless copper plating is carried out at room temperature for 3-5 minutes (choice: 4 min), no agitation necessary. Take the yarn out of the plating solution as soon as it is uniformly coated with copper.

Fibers are placed afterwards directly into post-treatment solution

Solution needs to be poured into container for copper plating bath solution.

7. Post treatment

The post treatment solution contains:

Citric acid: 10g/L

Sodium hypophosphite: 10g/L

Mix the above mentioned chemicals with 1 liter of water. Treat the copper coated yarn in this post-treatment solution for 20 min. Do not rinse beforehand.

Take the samples out of the solution, rinse them under distilled water (in beaker to avoid agitation) and dry them immediately with the hair dryer.

Excess solution needs to be added to the acid container (effluent waste).

List of chemicals needed

Chemical	Category number	Supplier
Sodium hydroxide 50% solution in water	41541-3	Sigma Aldrich
Pyrrol 98%	13170-9	Sigma Aldrich
Benzenesulfonic acid hydrate 97% (BSA)	448737	Sigma Aldrich
Iron (III) chloride hexahydrate	F2877	Sigma Aldrich
Palladium (II) chloride	520659	Sigma Aldrich
Tin (II) chloride dehydrate 98%	243523	Sigma Aldrich
Hydrochloride acid fuming 37%	258148	Sigma Aldrich
Copper (II) sulfate pentahydrate 98%	209198	Sigma Aldrich
Formaldehyde 37% wt% solution in water	25254-9	Sigma Aldrich
Potassium sodium tartrate tetrahydrate (Rochelle salt)	21725-5	Sigma Aldrich
Citric acid monohydrate	C1909	Sigma Aldrich
Sodium hyphosphite monohydrate	71795	Fluka
Gold (III) chloride trihydrate	G4022	Sigma Aldrich
Sodium phosphate dibasic	S9763	Sigma Aldrich
Sodium thiosulfate pentahydrate 99,5%	217247	Sigma Aldrich
Sodium sulfite	23932-1	Sigma Aldrich

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