FLEXIBLE AND STRETCHABLE CIRCUIT TECHNOLOGIES FOR SPACE APPLICATIONS

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ABSTRACT

Flexible and stretchable circuit technologies offer reduced volume and weight, increased electrical performance, larger design freedom and improved interconnect reliability. All of these advantages are appealing for space applications. In this paper, two example technologies, the ultra-thin chip package (UTCP) and stretchable moulded interconnect (SMI), are described. The UTCP technology results in a 60 µm thick chip package, including the embedding of a 20 µm thick chip, laser or protolithic via definition to the chip contacts and application of fan out metallization. Imec's stretchable interconnect technology is inspired by conventional rigid and flexible printed circuit board (PCB) technology. Stretchable interconnects are realized by copper meanders supported by a flexible material e.g. polyimide. Elastic materials, predominantly silicone rubbers, are used to embed the conductors and the components, thus serving as circuit carrier. The possible advantages of these technologies with respect to space applications are discussed.

1. INTRODUCTION

The driving application for flexible and stretchable circuit technologies is consumer electronics, especially handheld and mobile devices, which benefit the most from the reduction in form factor, the increased functional density and enlarged user comfort that is made possible with these technologies. Reduced volume and weight, increased electrical performance, larger design freedom and improved interconnect reliability are benefits that are also appealing for space applications.

Traditionally, electronics and sensor circuits are fabricated on flat rigid substrates, like FR4 Printed Circuit Boards (PCBs). In this conventional technology, packaged integrated circuits (ICs) and passive components are assembled onto the rigid PCB by soldering. For many applications, especially for mobile, portable, wearable and implantable electronics, the circuit should preferably be seamlessly integrated into the object which is used for transportation, is carried along, or worn on or inside the body. The electronics should be comfortable and unnoticeable to the user. In general, standard circuits do not fulfil these requirements. The user comfort can be increased in two ways. Extreme miniaturisation of the circuit reduces the presence of the system. A second approach is to transform the flat rigid circuit into a three-dimensional, conformable variant, following the random shape of the object or body part onto which it is integrated.

In this contribution, two original technologies developed at imec-CMST are presented. The ultra-thin chip package (UTCP) technology embeds 20 µm to 30 µm thick chips in a stack of spin-on polyimide (PI) layers. Adding thin-film, fan-out metallization results in an extremely miniaturized, lightweight and flexible chip package with a total thickness below 100 µm. Next to flexible electronics, a number of technologies for dynamically or one-time deformable stretchable circuits are under development. The stretchable concept is based on the interconnection of individual components or component islands with meander shaped metal wirings and embedding in elastic polymers like silicone rubbers (PDMS), polyurethanes (PU) or other plastics.

Although these technologies were not explicitly developed for space applications, their unique features create the potential for use in this new application domain. Miniaturization through UTCP use and 3D integration through circuit random deformability significantly reduces system size and weight, which is an important advantage for space applications. An interesting point of view, further discussed in this paper, is the possible improvement in interconnect reliability that these new technologies offer. Thanks to the embedding in elastic materials, stretchable circuits could show a decreased sensitivity to vibration. UTCPs can be embedded in flexible or rigid PCBs using lamination, through-hole drilling, and via metallization. UTCP production and PCB embedding is completely solderless, thus avoiding associated reliability problems, usually encountered in harsh environments.

The following two sections describe the process flow and application examples for flexible chip packaging and stretchable electronics. Section 4 discusses the advantages these technologies can offer for space applications.

2. FLEXIBLE CHIP PACKAGING

One of the main drivers in packaging research is to integrate as much functionality into a single package as possible, without increasing the overall size of that

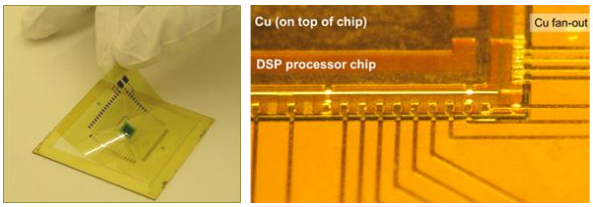


Figure. 1. Overall view of the ultra-thin chip package (left) and close-up of the fan-out circuitry (right)

package. The ultimate goal is a System-in-Package (SiP), where both active and passive components are integrated, realizing a standalone (sub)system with a given functionality. One of the current challenges is to match this increase in functional density with improved flexibility and reduced overall thickness. A key aspect herein is the use of thinned bare-die Si chips to minimize the package form factor.

Looking purely at the functional density, several SiP approaches can be applied to realize the high-density modules. Fan-out wafer-level packaging (FO WLP), where the package is reduced to its absolute minimum, and direct chip embedding are two examples of technologies that offer increased functionality in a reduced form factor. A European representative of the latter technology is described in the next section.

The overall thickness of these packages, however, remains in the order of hundreds of micrometres, strongly limiting the flexibility of the substrate onto which they are placed. The ultra-thin chip packaging technology described in section 2.2 combines a high degree of miniaturization with an inherently flexible chip package. The use of thin-film processing makes it possible to integrate chips with the highest complexity and a fine contact pad pitch.

2.1. Chip embedding

The Embedded Component Packaging technology from AT&S directly integrates the components in the core layers of the PCB [1]. The technology can be used for the embedding of both active and passive components. The main characteristics of the technology are the use of openings in the prepreg layers matching the location of the components and the microvia interconnections to the contact pads of the embedded component. The plated Cu microvia interconnection eliminates the need for solder or conductive adhesives, thus avoiding the associated failure modes. The thickness of the components (100 – 150 µm for chips, 150 – 300 µm for passive components) and their pad metallization (copper) need to be compatible with the lamination and metallization process steps, respectively. A broad range of embeddable passive components are currently available and manufacturers are continuously improving their product range with respect to available values, tolerances, and temperature and power ratings. Bare-die chips are more difficult to procure, especially for lower volumes, but are becoming more and more common.

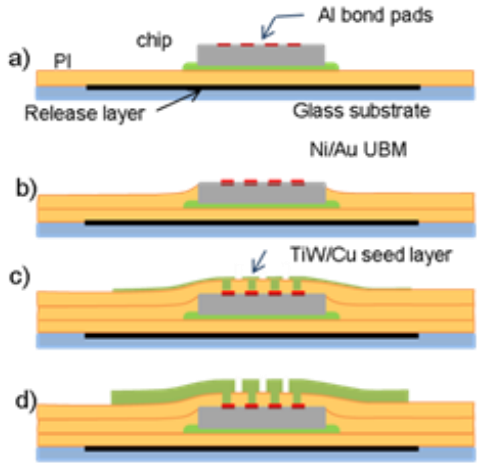


Figure. 2. Process flow for realizing the ultra-thin chip package

A standard PCB process flow starts with a double sided core, which is structured in the subsequent process steps and built up to a multilayer construction. In the case of embedding components, a so called “embedded core” is produced in the first phase of the process flow. The main process steps for embedding of components are printing of adhesive, assembly of components, lamination and drilling of vias and plated through holes. The suitability of embedding passive components for space applications is currently being investigated in the PCESA project (ESA/TRP) by imec, AT&S and QinetiQ Space.

2.2. Ultra-thin chip package

To achieve the requirements of form factor and flexibility, the total thickness of the chip package needs to be reduced by an order of magnitude, i.e. less than 100 µm. A suitable candidate is the ultra-thin chip package (UTCP) technology, developed and patented by imec-Cmst [2, 3]. This technology consists of an ultra-thin chip, embedded in polyimide layers and contacted using microvias and a fan-out interconnection scheme (Fig. 1).

Fig. 2 shows the process flow for realizing the UTCP. The process starts from a glass carrier substrate with a suitable release layer, onto which a polyimide layer is spun. The ultra-thin chip, with a thickness down to 20 µm, is subsequently placed in the desired location. A second, photosensitive polyimide layer is spun on top of the chip and consequently patterned to remove the polyimide in the area above the chip. The second polyimide layer thus acts as a planarization layer for the third polyimide layer that carries the interconnection circuitry. This metal layer is realized by vacuum depositing a copper seed layer which is electroplated to the desired thickness. As a final step, the metallization layer is patterned, resulting in a flexible interposer with a thickness of about 70 µm, mounted on a glass carrier. The design of the metal fan-out allows converting the

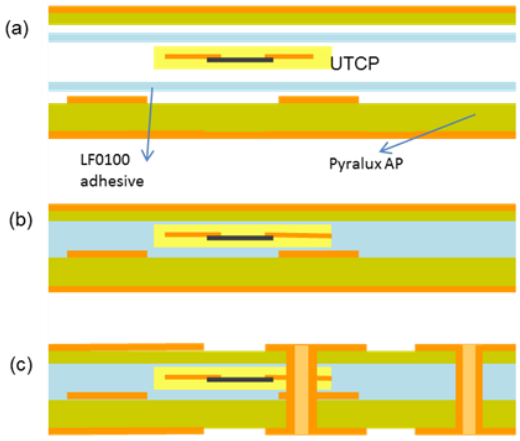
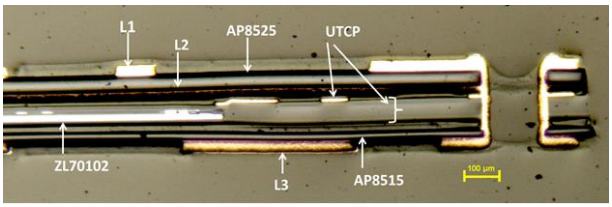


Figure. 3 Schematic process flow for UTCP embedding

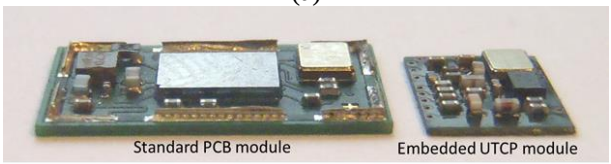
fine pitch (currently down to 65 µm) of the IC to a larger pitch compatible with the intended application, such as embedding or stacking. Furthermore, it is possible to create interconnections between several contact pads of the IC, reducing the required number of connections to the external substrate.

The embedded die can be used as a package (e.g. solder balls can be placed on the contacts and the package can be solder assembled on interconnection substrates). Alternatively the ultra-thin package can be embedded in a stack of rigid or flexible PCB layers. The UTCP can be tested before embedding, presenting a clear advantage compared to the direct embedding of bare dies.

Fig. 3 shows a schematic process flow for UTCP embedding, in this case between two polyimide copper-clad laminates. The UTCP is aligned to the copper pattern on one of the inner layers and encapsulated by the acrylic adhesive which is generally used for building multilayer flexible printed circuit boards. After lamination, holes are drilled though the stack and consequently metallized, realizing the interconnection between the UTCP and the board without needing microvia interconnection schemes. The embedding of



(a)



(b)

Figure. 4. A cross section of a board with embedded UTCP of a RF transceiver (ZL70102 from Microsemi) (top) and comparison between the embedded UTCP radio module and the original module (bottom)

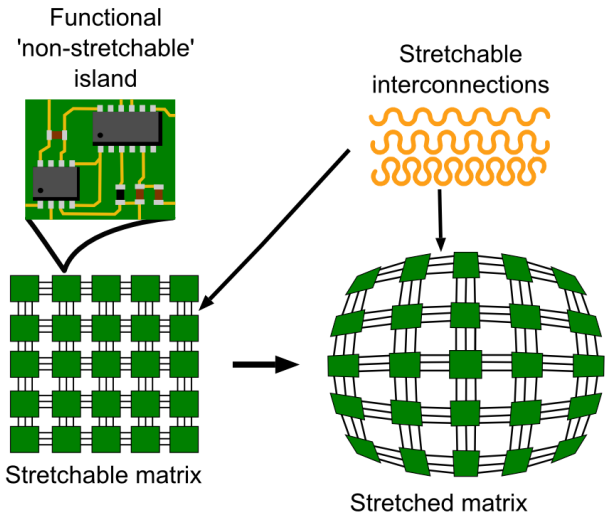


Figure. 5 Overall concept of a stretchable circuit

UTCPs has been demonstrated for a number of flexible and rigid materials, which need to offer good adhesion to the polyimide-based UTCP and be compatible with the through-hole metallization process.

A cross-section of the resulting board with embedded UTCP is shown in Fig. 4a. An UTCP of a RF transceiver (ZL70102 from Microsemi) is embedded in a three-layer flexible printed circuit board (FCB). The plated through-hole interconnecting layer 1 and 3 of the FCB to the UTCP can be seen on the right hand side. The total thickness of the FCB averages around 250 µm. Embedding the UTCP package inside the board not only avoids the use of bulky surface-mount packages but also frees up board space for mounting active or passive component. This three-dimensional packaging approach allows for a significant reduction in board size and thickness. As an example, Fig. 4b shows a comparison between an embedded UTCP radio module and the original module based on a chip-scale package (CSP). The total volume of the module is reduced to less than 60 % of the original.

Further miniaturization can be realized by integrating multiple ICs in a single package. This can be done by stacking multiple UTCP-packaged dies on top of each other using lamination technology, combined with the fabrication of the interconnections between the layers using via drilling and metallization by electroplating. Such a stacked UTCP is not flexible anymore, but an extreme degree of miniaturization is realized: in a package of about 300 µm thick, four dies can be embedded and interconnected [4].

3. STRETCHABLE ELECTRONICS

The overall concept of a stretchable circuit is illustrated in Fig. 5. The circuit is comprised of a number of rigid (or moderately flexible in some cases) component islands, where each island holds a single component or a limited number of components. The individual rigid

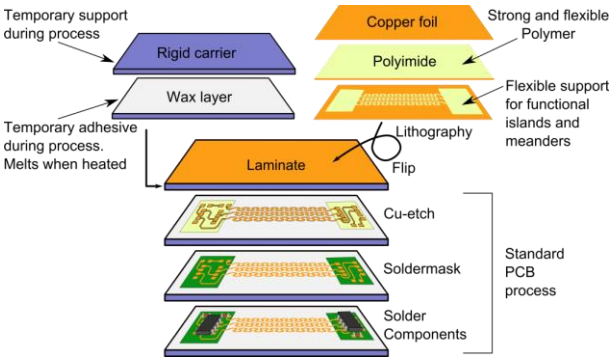


Figure. 6 First part of the SMI process flow

components or component islands are interconnected, not by straight Cu lines, as in conventionally designed PCBs, but by means of meander shaped Cu conductors instead. Once the meanders have been embedded in a mechanically elastic circuit carrier, they can dynamically elongate (stretch) under mechanical forces and come back to their original state, without losing their electrical interconnection function during this stretching. The meander shape in combination with the elastic carrier makes the conductor function as a two-dimensional spring. Realizing the planar meanders using the Stretchable Moulded Interconnect (SMI) technology developed by imec and Ghent University, requires only a minimal deviation from conventional PCB processing.

The first steps in the SMI process flow are shown in Fig. 6. A rigid carrier substrate is covered with a temporary adhesive, onto which a copper foil or polyimide-copper flexible laminate is mounted by lamination. The optional polyimide layer serves as support material for the copper meanders and for the component islands. Supporting the meanders with a PI carrier has proven to greatly improve the mechanical reliability and operational lifetime of the copper meander circuits.

Next, the samples go through a number of standard PCB manufacturing and assembly steps. Copper meanders, along with the standard design interconnections on the component islands, are patterned by photolithography and wet etching. The polyimide support layer is structured by laser cutting. If necessary, solder mask is locally applied by screen printing, contact pad finish is applied and components are mounted using a conventional reflow solder process. At this point, the circuit can be tested and repaired, if required. Fig. 7 shows an SMI substrate after component assembly.

The second part of the SMI process flow involves the

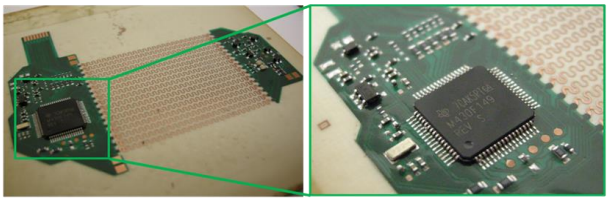


Figure. 7 Example of a stretchable system for respiratory monitoring before encapsulation

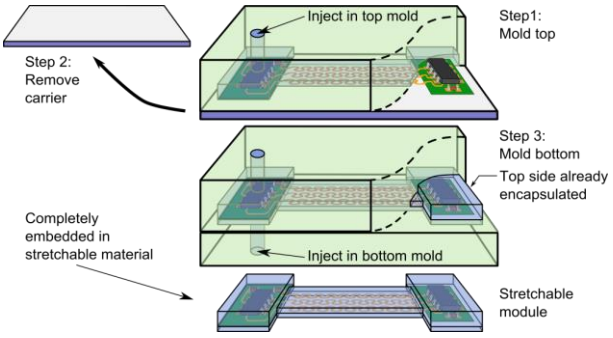


Figure. 8 Second part of the SMI process flow

application of the stretchable carrier material, giving the circuit its resilience (Fig. 8). In the first step, the top of the circuit is covered by a layer of stretchable material by liquid injection moulding (LIM) of a two-component Polydimethylsiloxane (PDMS) mixture. Alternatives for the application of the stretchable carrier material by LIM include cover lamination and spray coating. Besides PDMS, also polyurethane (PU) or any polymer for which a liquid precursor or a thermoplastic variant is available can be applied. In a second step, the assembly is removed from the temporary carrier. After cleaning, the circuit is completely embedded by applying a second layer of stretchable material at the bottom, (i.e., by a second LIM step).

A critical factor in the use of stretchable interconnections is the design of copper meanders. Extensive modelling was performed to minimize stress and strain concentrations in the meander under deformation. The current meander shape of choice is the horseshoe shape, as shown in Fig. 9. A horseshoe shaped meander is a connection of circular segments, offering a good compromise between sufficient stress distribution along the meander on one hand, and ease of design and circuit layout on the other. For minimal stress the width (W) of the track should be as small as possible. The minimum width is determined mainly by technological constraints. During the cycling elongation of the stretchable circuit, a permanent deformation or plastic strain is induced in the metal causing a fatigue failure. Therefore, in order to improve the fatigue reliability of the stretchable interconnect; the plastic strain has to be minimized.

The ratio R/W determines the maximum plastic strain in the meander for a given deformation. In general for

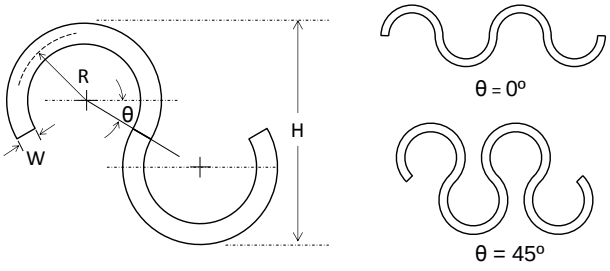


Figure. 9 Horseshoe shaped meander with relevant design parameters

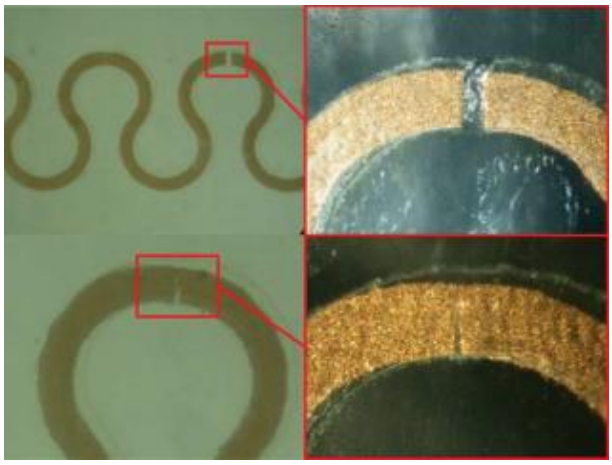


Figure. 10 Failures at the top of meanders with polyimide support. Upper picture shows complete fracture of the copper trace, while the bottom picture shows an initiated microcrack

deformations of 20% and less, the maximum plastic strain decreases with increasing R/W. High R/W ratios, however, also mean meanders with high overall width, and thus a low density of parallel running meanders. A ratio of R/W = 10 normally offers a good compromise between low maximum plastic strain in the meander and high number of parallel running meanders per unit width of the stretchable interconnect area.

A further improvement of the mechanical reliability of the meanders is achieved by supplying the meanders with a flexible support, i.e. a PI film. Numerical modelling showed that the PI width is the main parameter, reducing the maximum plastic strain in the Cu meander [5].

Focus of the reliability investigation for stretchable interconnections has been on the optimization of the performance under mechanical stress like e.g. periodic or random deformation of the circuit. No standard tests for stretchable circuits exist today. In order to quantify and assess the mechanical reliability of stretchable circuits uniaxial stretching tests are executed on samples that contain a number of parallel running meanders. The main test is cyclic stretching at moderate maximum elongation until conductor rupture.

Results of these cyclic stretching tests have been described extensively elsewhere [6]. The main conclusions are that supporting the Cu meanders with a flexible material like polyimide drastically improves the lifetime of the interconnection. As an example, a double sided PI-enhanced stretchable interconnect withstands more than 90.000 stretching cycles at 5 % elongation, and even for elongations up to 20 %, the PI-enhanced stretchable interconnect can survive more than 400 cycles.

Proper design and fabrication of the transitions between component islands and the stretchable interconnects is at least as important as the stretchable interconnects themselves. There is no quantitative structural design rule or optimized design available for solving this reliability issue. A qualitative rule is that the transition from rigid over flexible to stretchable circuit parts should be as smooth as possible.

Optical microscopy was used to analyse both types of samples after the endurance test. The copper interconnects break at the top of the meanders, the place where the highest accumulated plastic strain is present [7]. The start of the micro crack as seen in Fig. 10 is not detected by the resistivity measurements due to the very low increase of resistivity. On non-supported copper tracks, the crack propagates during one or just a few cycles leading to the sudden breakdown. Delayed crack propagation is observed for the meanders with PI support, which translates in a slowly increasing track resistance.

4. RELEVANCE TO SPACE APPLICATIONS

The need for thin, flexible packaging and stretchable interconnection is driven by the desire for increased functional density in a reduced or application-specific form factor. Reliability requirements for the typical use environments are not of the highest concern during the technology development phase. The improvements offered by these new technologies, such as increased functional density, form factor reduction and the possibility to adapt to any shape, are also interesting for space applications. In this application field, however, excellent reliability is an absolute priority.

From this point of view, it is interesting to evaluate what reliability improvements these new technologies could bring. Failure mechanisms for solder interconnections are well-documented [8, 9]. Although no legislative obligation is in place, lead-free solder issues become more and more relevant for space as well [10, 11]. Based on the Pb-free experience in consumer applications, failures related to the use of solder will only increase with this transition. Embedding of components in general, and of UTCPs in particular, offer a promising alternative by using plated interconnections in the form of copper microvias or plated though-holes. Both from a dimensional as from a material point of view, these interconnections have a thermo-mechanical advantage over bulky and brittle solder joints. Embedding the components inside the board also offers increased mechanical protection with respect to bending or shock.

By its very nature, stretchable interconnections offer an even larger potential for mechanical robustness. By dividing the large system into smaller sub modules that are interconnected by elastic interconnections which can absorb the mechanical stress from vibrations or shock, sensitive components can be protected without the need for bulky anti-vibration frames.

The authors are well aware of the fact that these statements are oversimplified and that the proposed technologies will suffer from or even introduce new failure modes. But it is thinking outside of the box, that put a man on the moon.

5. CONCLUSION

Two emerging technologies for flexible packaging and stretchable interconnections were discussed in this paper. The UTCP technology makes it possible to realize chip packages with a total thickness of less than 100 µm. Embedding these packages to exploit the third dimension results in a volume reduction of over 60 %.
Stretchable interconnections in the form of encapsulated meanders can survive tens of thousands of stretching cycles of up to 5 % elongation. It has been illustrated that mechanical reliability is strongly enhanced by introducing a flexible support material for the meanders and by providing smooth mechanical transitions between the rigid solder assembled standard components and the soft and conformable stretchable interconnects.
Compared to common assembly and interconnection technologies for space applications, the proposed technologies are still in their infancy. The possibilities for new form factors with increased functional density are obvious, but also a potentially improved reliability in harsh environments merits further investigation into applying these technologies to space applications.

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