Common-Mode Noise Reduction Schemes for Weakly Coupled Differential Serpentine Delay Microstrip Lines

Guang-Hwa Shiue, *Member of IEEE*, Che-Ming Hsu, Yu-Han Kao, and Yi-Chin Tsai, and Dries Vande Ginste, *Senior Member of IEEE*

***Abstract*—This work proposes design schemes to reduce the common mode noise from weakly coupled differential serpentine delay microstrip lines (DSDMLs). The proposed approach is twofold: we leverage strongly coupled vertical-turn-coupled traces (VTCTs) instead of weakly coupled VTCTs (conventional pattern) and add guard traces. Time- and frequency-domain analyses of the proposed schemes for reducing the common-mode noise are performed by studying the transmission waveform and the differential-to-common mode conversion using the circuit solver HSPICE and the 3-D full-wave simulator HFSS, respectively. Compared to the conventional design of the weakly coupled DSDMLs, the proposed solutions yield a reduction of about 54% of the peak-to-peak amplitude of the common-mode noise, while the differential impedance remains matched along the complete length of the DSDML. Moreover, the range of frequencies over which the magnitude of the differential-to-common mode conversion is now significantly reduced, is very wide, i.e. about 0.3~10GHz. Furthermore, the differential insertion and reflection loss introduced by the newly proposed designs are almost the same as the ones achieved by using the conventional design. Finally, a favorable comparison between simulated and measured results confirms the excellent common-mode noise reduction performance of the proposed schemes.**

Index Terms* — *Differential serpentine delay microstrip line, common-mode noise, guard trace, differential-to-common mode conversion, differential reflection loss, differential insertion loss.

I. INTRODUCTION

As clock frequencies and data transmission rates in semiconductor systems steadily increase beyond the GHz range, the timing control of high-speed clocks and digital data, propagating via signal traces on printed circuit boards (PCB) and packages, is becoming a critical issue in high-speed digital circuit design [1]. Although many methods for minimizing clock or digital data signal skew have been presented, delay lines are usually utilized in the critical nets of a PCB. For example, the conventional serpentine routing schemes are widely used in industrial PCB design. Additionally, differential signaling has become increasingly important in modern high-speed digital circuits. Compared to single-ended transmission lines, adopting differential lines leads to a reduction of harmful interference [2]. Notable applications include Serial Advanced Technology Attachment III (SATA III/6Gbps), High Definition Multimedia Interface (HDMI/5Gbps), PCI Express interconnect III (8Gbps), and USB 3.0 (5Gbps) devices. Since these high-speed digital systems rely on multiple differential

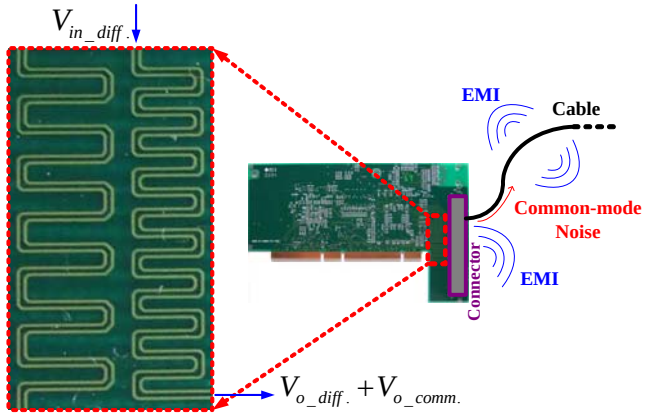
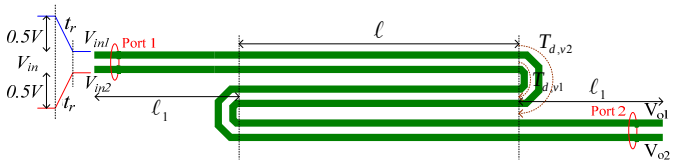


Fig. 1. Practical example of a differential serpentine delay microstrip line (DSDML) on an industrial printed circuit board (PCB).



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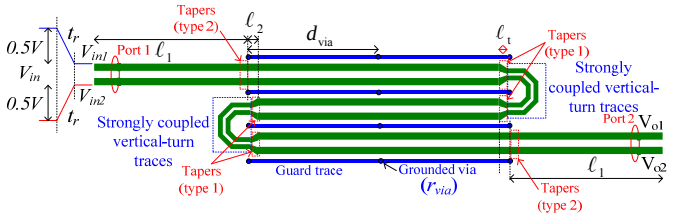

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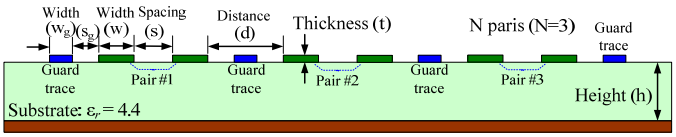


(c)

Fig. 2. Top view of (a) a conventional and (b) a newly proposed DSDML with three sections (N=3). (c) Cross-sectional view.

line pairs, timing synchronization has become a serious design issue. Therefore, the differential serpentine delay line has been recently employed.

In high-speed data links, cables and connectors are required to transmit differential signals between the various electronic devices or PCBs. This may cause electromagnetic interference (EMI), because common-mode noise couples to the I/O cables or connectors, which then behave as antennas [3] (Fig. 1). Hence, during the design of state-of-the-art electronic systems, reducing the common-mode noise induced by differential interconnects, is crucial. In a differential serpentine delay microstrip line (DSDML), the main contributions to common-mode noise originate from the length mismatch of the vertical-turn-coupled traces (VTCTs), the length of the parallel differential coupled traces, and the crosstalk between the parallel pairs of differential coupled lines [4]. In recent literature, several approaches to reduce the common-mode noise induced by differential bends have been proposed, such as adding capacitance to deal with the bend discontinuity [5] or by using tightly coupled microstrips [6]. Furthermore, the use of guard traces to reduce the differential near-end and far-end crosstalk noise between parallel differential lines has been investigated [7].

In a previous study [8], noise reduction schemes were developed for a weakly coupled DSDML by adopting strongly coupled VTCTs instead of the weakly coupled VTCTs (conventional pattern) and adding guard traces, as shown in Fig. 2(b). The effectiveness of the noise reduction for the combined structures was verified in the time domain and the frequency domain, merely using the 3-D full-wave simulators CST and HFSS, respectively. So, no thorough theoretical analyses or measurement results are yet presented. By extending the results of [8], the recent paper thoroughly investigates the common-mode noise reduction schemes for a weakly coupled DSDML. First, the common-mode noise reduction is analyzed in the time-domain by studying the transmission waveform using the circuit solver HSPICE. Thereto, an equivalent circuit model is developed. Second, the time-domain results of the proposed schemes are validated using the 3-D full-wave simulator CST [9]. Third, the magnitude of the differential-to-common mode conversion, $|S_{cd21}|$ [10], is determined by frequency-domain simulations with the simulator HFSS [11]. Furthermore, this work also presents theoretical implications of the mechanisms that are leveraged to reduce the common-mode noise. Finally, common-mode noise measurements were performed in the time domain and the frequency domain, clearly validating and illustrating the newly proposed designs.

The paper is organized as follows. Sections II and III describe the problem of interest and present the equivalent circuit model for a DSDML with the newly proposed design patterns, respectively. Section IV examines the mechanisms of the common-mode noise reduction in a weakly coupled DSDML, as obtained by the proposed structures. For verification purposes, Section V compares simulated and measured results. Finally, conclusions are drawn in Section VI.

II. Statement of the Problem

The DSDML is formed by coupled microstrip lines with multiple parallel differential trace pairs. For simplicity, a DSDML with three sections (N=3) is adopted in this work, as shown in Fig. 2. The conventional pattern is shown in Fig. 2(a); the improved DSDML of Fig. 2(b) will be further discussed in Section III. The presented top and cross-sectional views of the DSDML specify all structural parameters, i.e. the trace width (W) of the differential lines, the trace width (W_g) of the guard traces, the length (ℓ) of the parallel coupled traces, the length (ℓ_1) of the parallel coupled traces that are connected to a port, the height (h) of the substrate, the dielectric constant (ε_r) of the substrate, the thickness (t) of the signal trace, the spacing (d) between the members of the differential trace pairs, and the distance (S) between the differential serpentine traces.

The common-mode voltage $V_{c,out}$ is defined as [3]

$$V_{c,out} = \frac{V_{o1} + V_{o2}}{2} \tag{1}$$

where V_{o1} and V_{o2} denote the two voltages at the receiving end of the DSDML. Additionally, the coupling coefficient of the differential lines is defined by [12]

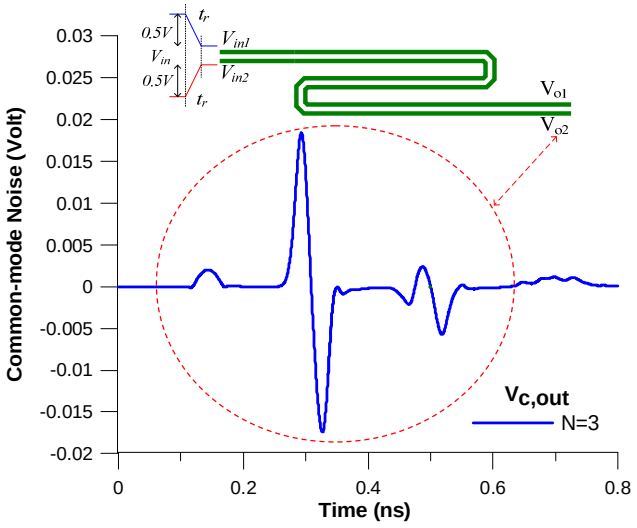
$$k = \frac{Z_{0,even} - Z_{0,odd}}{Z_{0,even} + Z_{0,odd}} \tag{2}$$

where $Z_{0,even}$ and $Z_{0,odd}$ denote the even-mode and odd-mode characteristic impedances of the differential traces, respectively.

Consider a conventional DSDML with N=3 on an FR4 PCB, as presented in Fig. 2(a), with the following geometrical parameters: (W, S, h, d, ℓ, ℓ_1, t) = (7.5mil, 9.5mil, 5.5mil, 17mil, 535mil, 100mil, 1.7mil). The dielectric constant ε_r and loss tangent of the substrate material are 4.4 and 0.02, respectively. According to (2), the coupling coefficient is approximately 0.1 and hence, the coupling is weak. An ideal differential ramped step source with a magnitude of ±1V and a rise time (t_r) of 50ps is now driving the DSDML. Although the dual back-to-back VTCTs do not introduce a length difference between the two traces of a DSDML, similar to dual back-to-back coupled bends in differential traces [5], the common-mode noise is not completely compensated by the VTCTs [4]. The contributions to the common-mode noise originate from the mismatch of the trace lengths of the individual VTCTs, the length of the parallel differential coupled traces between two

VTCTs and the crosstalk between the parallel pairs of differential coupled lines [4]. The time-domain common-mode voltage at the receiving end of the DSDML is shown in Fig. 3(a). This result was obtained by means of a simulation using CST. Fig. 3(b) compares the simulated magnitude of the differential-to-common mode conversion for a conventional DSDML with N=3 with that of straight pair of differential lines of equivalent length. This simulation was performed in HFSS. Clearly, the conventional DSDML induces a much larger amount of differential-to-common mode conversion than the straight differential lines.

From both simulated results, in the time domain and the frequency domain, it can be concluded that the common-mode noise at the receiving end of a DSDML is large. Consequently, the reduction of common-mode noise induced by DSDMLs is very important as this prevents EMI generated by cables or connectors, which can seriously degrade electronic systems.



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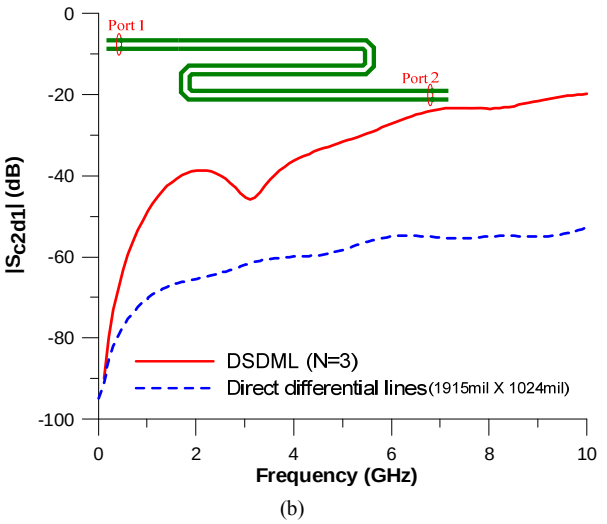

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Fig. 3. (a) Time-domain simulated common-mode noise at the receiving end of a conventional DSDML with N=3. (b) Differential-to-common mode conversion induced by a conventional DSDML with N=3 and by a pair of straight differential lines of equivalent length.

III. Proposed Common-Mode Noise Reduction Schemes and Circuit Modeling

A. Proposed Structure

Fig. 2(b) illustrates the proposed common-mode noise reduction techniques for conventional weakly coupled DSDMLs. The noise reduction approach is twofold: (a) strongly coupled VTCTs are used as substitutes for weakly coupled VTCTs and (b) guard traces are added. The separation between two grounded vias of the guard traces is d_{via} (250mil). The strongly coupled VTCTs and weakly coupled differential traces are connected via coupled tapers of type 1, as presented in Fig. 2(b). To keep the differential impedance (Z_d) matched and to avoid strong discontinuities, differential traces with different cross-sectional dimensions are connected via coupled tapers of type 2, as also shown in Fig. 2(b). The length of the tapers is set to approximately 7.5mil. The geometrical parameters of the strongly coupled VTCTs and the guard traces are the trace width (W_s) of the differential lines, which is 4mil, the separation (S_s) between the differential traces, which is 4mil, and the trace width (W_g) of the guard traces, which is 9mil. The coupling coefficient and differential impedance of the parallel sections of the strongly coupled VTCTs are about 0.2 and 105Ω, respectively. The other geometrical and material parameters are the same as in the previous section.

B. Circuit Modeling

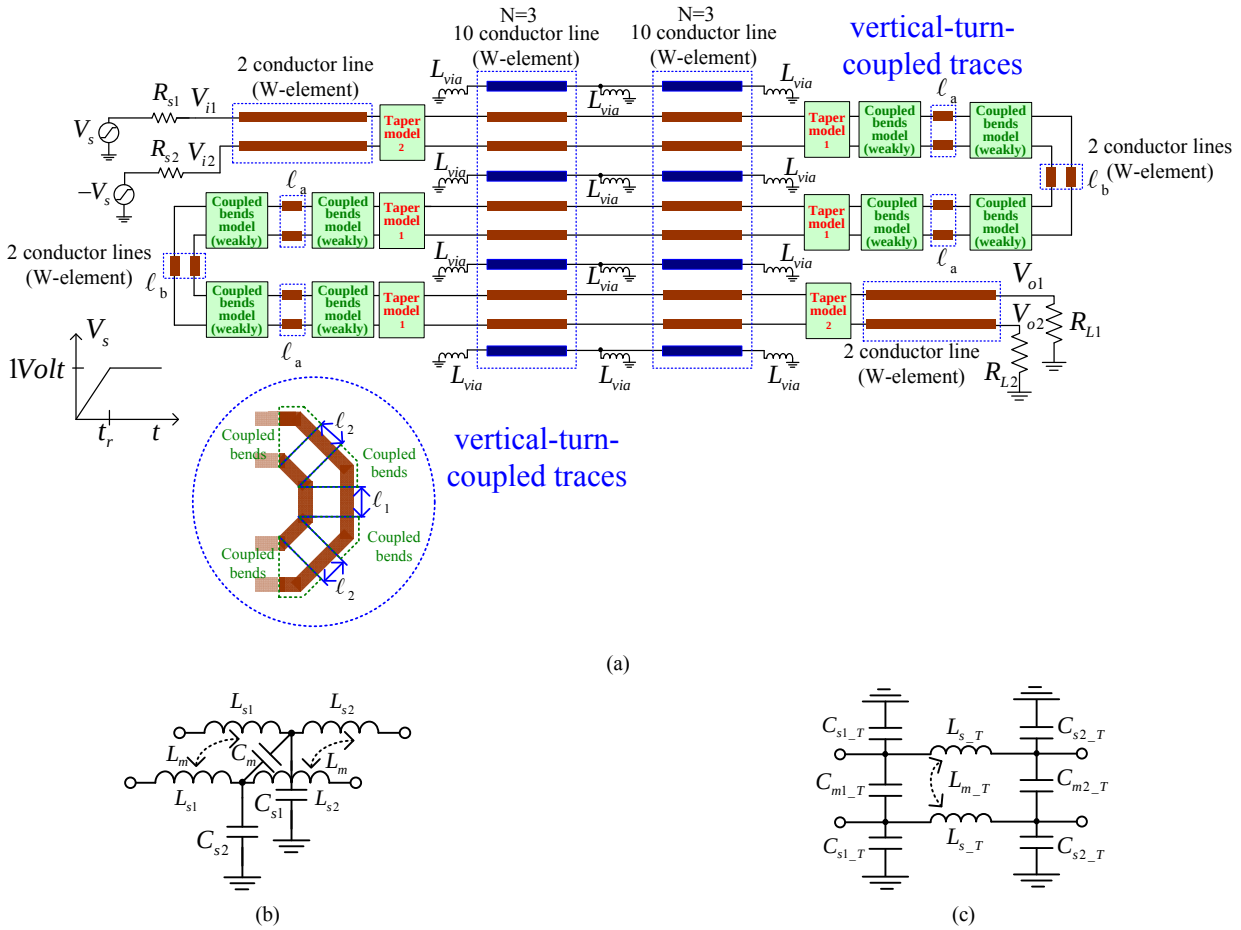
Fig. 4(a) presents the circuit model that is utilized in the HSPICE simulation of the DSDML with N=3 and with the above introduced common-mode noise reduction schemes. The multiple-coupled transmission lines, including the guard traces, are modeled using W-elements to take the finite transmission line losses into account. The coupled transmission lines of the VTCTs are also modeled using W-elements. The grounded vias of the guard traces are regarded as series inductances [13],

$$L_{via} = \mu_0 \frac{h_{via}}{2\pi}\left[\ln\left(\frac{2h_{via}}{r_{via}}+\sqrt{1+\left(\frac{2h_{via}}{r_{via}}\right)^2}\right)-\sqrt{1+\left(\frac{r_{via}}{2h_{via}}\right)^2}+\frac{r_{via}}{2h_{via}}+\frac{1}{4}\right] \quad (3)$$

where h_{via} (5.5mil) and r_{via} (4mil) are the height and radius of the grounded vias, respectively. Figs. 4(b) and (c) show the T-model of the 45° angle coupled bends [4], [14] and the π-model of the coupled tapers [6], respectively. Tables I and II present the extracted parameters [5], [6] of the equivalent circuit model of the 45° angle strongly coupled bends and the coupled tapers, respectively. The parameters of the circuit model of the 45° angle weakly coupled bends can be found in [4].

Fig. 5 compares the simulated differential reflection and insertion losses of the 45° angle strongly coupled bends and the coupled tapers obtained by using the equivalent circuit model on the one hand and the full-wave simulator (HFSS) on

the other hand. The favorable comparisons validate the proposed equivalent circuit models. (Validation of the model parameters of the 45° angle weakly coupled bends can be found in [4].)



(a)

(b)

(c)

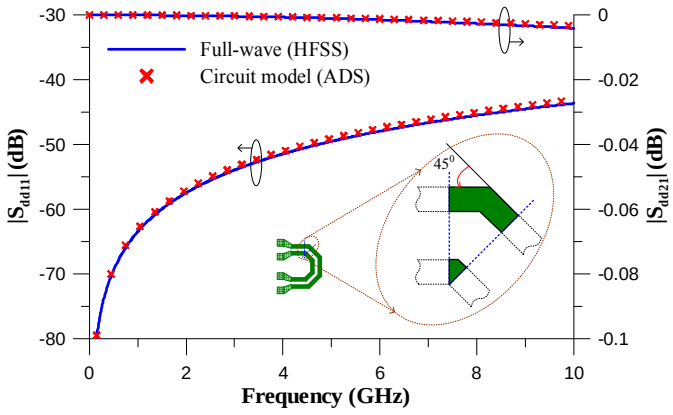
Fig. 4. (a) Graphical configuration of a simulation of a DSDML in HSPICE (N=3). Equivalent lumped circuit models of (b) 45° angle coupled bends and (c) coupled tapers.

Table I
Parameters of the equivalent lumped circuit model for 45° angle strongly coupled microstrip lines.

$(L:nH,\ C:\mu F)$	Trace width	Trace spacing	L_{s1}	L_{s2}	C_{s1}	C_{s2}	L_m	C_m
Strongly coupled 45° angle coupled bends	4 mil	4 mil	0.0096	0.042	0.0028	0.02	0.0033	0.0014

Table II
Parameters of the equivalent lumped circuit model for different types of coupled tapers.

$(L:nH,\ C:\mu F)$		Trace width	Trace spacing	L_{s_T}	L_{m_T}	C_{s1_T}	C_{s2_T}	C_{m1_T}	C_{m2_T}
Coupled Tapers (type 1)	Without GTs	7.5 mil/4mil	9.5 mil	0.102	0.0167	0.02	0.0175	0.0013	0.002
	Without GTs and Impedance Matched	6.9 mil/4mil	9.5 mil	0.115	0.0293	0.0193	0.0175	0.0012	0.002
Coupled Tapers (type 2)		7.5 mil/6.9mil	9.5 mil	0.1165	0.023	0.0203	0.02	0.001	0.0008



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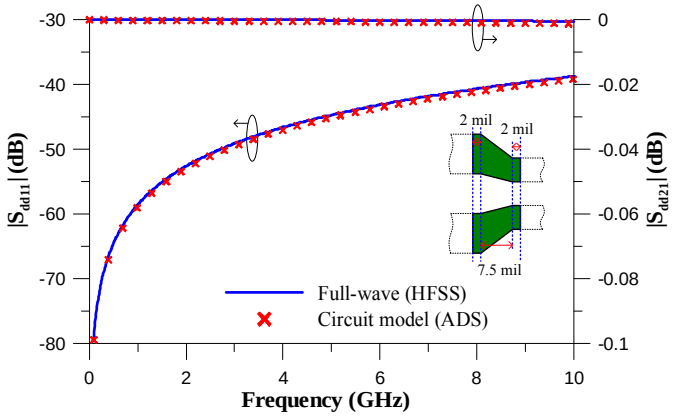

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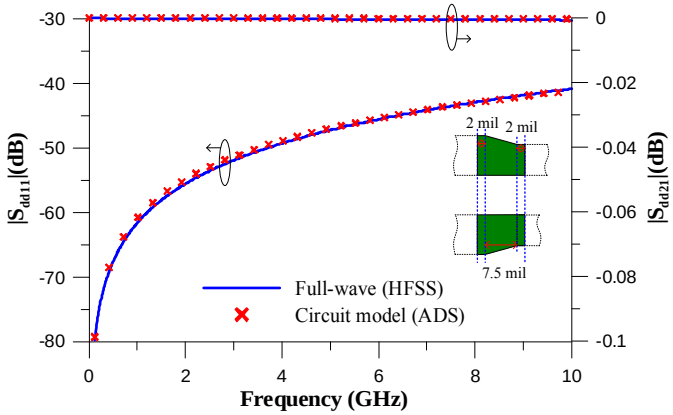


(c)

Fig. 5. Comparison of the differential reflection and insertion losses simulated using the equivalent circuit model and the full-wave simulator (HFSS) for (a) 45° angle coupled bends, (b) coupled tapers of type 1 and (c) coupled tapers of type 2.

IV. Simulation and Analysis

In a weakly coupled DSDML, the contributors to common-mode noise are the mismatch of the lengths of the VTCTs's traces, the length of the parallel differential coupled traces between two VTCTs and the crosstalk between the parallel pairs of differential coupled lines [4]. This work presents two schemes to reduce the common-mode noise induced by a weakly coupled DSDML, i.e. leveraging strongly coupled VTCTs and adding guard traces. The purpose of using strongly coupled VTCTs instead of weakly coupled VTCTs in a conventional weakly coupled DSDML is to diminish the time delay between the two traces of the VTCTs, as such reducing the common-mode noise. The purpose of adding guard traces in a DSDML is to reduce the effect of the length of the parallel differential coupled traces and the crosstalk between the parallel pairs of differential coupled lines. Combining the two newly proposed schemes in a DSDML reduces the common-mode noise in an optimal way. The following sections present a comprehensive analysis.

A. Using Strongly Coupled VTCTs

The first of the proposed common-mode noise reduction schemes is to use strongly coupled VTCTs in a weakly coupled DSDML, as shown in Fig. 6. The geometrical parameters of strongly coupled VTCTs are the trace width (W_s) and separation (S_s) of the differential traces, which are both 4mil, i.e. the lowest value that can still be reliably achieved in a PCB factory. The strongly coupled VTCTs and the weakly coupled differential traces are connected via coupled tapers of type 1. The differential impedance of the strongly coupled VTCTs is about 105Ω. Therefore, the deviation of the differential impedance is less than 5%.

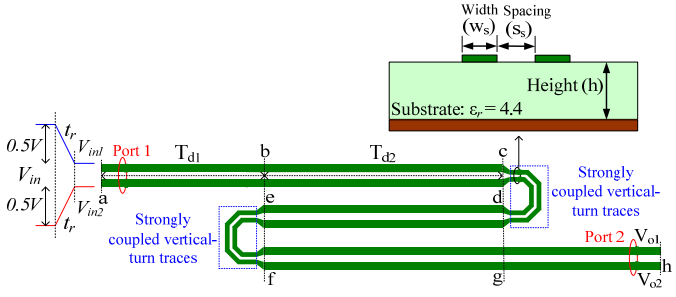


Fig. 6. First proposed common-mode noise reduction scheme: use of strongly coupled VTCTs in a conventional weakly coupled DSDML.

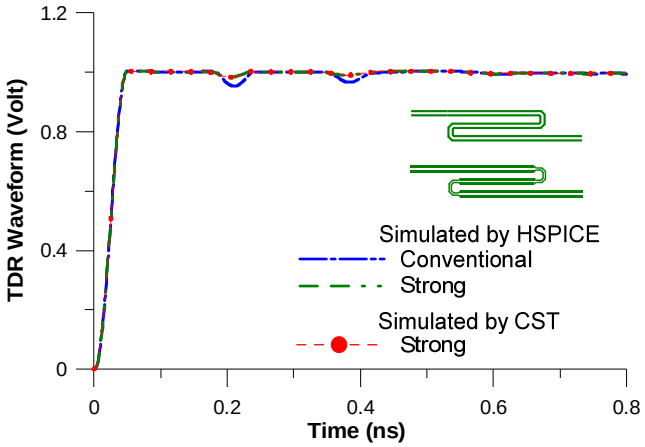
Fig. 7(a) compares time-domain reflection (TDR) waveforms of the conventional weakly coupled DSDMLs when using conventional VTCTs as opposed to strongly coupled VTCTs. In Fig. 7(a), the favorable comparison between the TDR waveforms obtained with HSPICE and CST again validates the parameters of the proposed equivalent

circuit models of the 45° angle strongly coupled bends and the coupled tapers. Interestingly, the voltage drops of the TDR waveform of a DSDML with conventional VTCTs are different from those of a DSDML with strongly coupled VTCTs.

Recall the mechanism of a TDR waveform on a DSDML: the voltage drops are caused by far-end crosstalk noise, which is coupled between the parallel differential line pairs [2]. Based on the mechanism associated with far-end crosstalk noise, the first voltage drop in the TDR waveform appears mostly after time $2T_{d1}+2T_{d2}+T_{d,v}$ (Fig. 6). The TDR waveform of VTCTs appears after time $2T_{d1}+2T_{d2}$. In the general case, $T_{d,v}$ is less than $2T_{d2}$. Accordingly, the TDR waveform of the VTCTs overlaps the far-end crosstalk voltages after time $2T_{d1}+2T_{d2}$. Hence, since in both cases the parallel differential line pairs have almost identical lengths and cross-sections, the voltage drops of the TDR waveform of a DSDML with conventional weakly coupled VTCTs are similar to those that originate from a DSDML with strongly coupled VTCTs [2].

Fig. 7(b) shows the simulated TDR waveforms of the DSDMLs with conventional and strongly coupled VTCTs, but this time without crosstalk between the parallel differential line pairs, obtained using HSPICE. It is observed that the TDR waveforms of conventional and strongly coupled VTCTs exhibit small negative and positive voltage waveforms, respectively.

According to the above analyses, it can be concluded that the total voltage drops of the TDR waveform of a DSDML with conventional weakly coupled VTCTs are larger than those of a DSDML with strongly coupled VTCTs (Fig. 7(a)). Restated, the performance of the TDR waveform of a DSDML with strongly coupled VTCTs is better than the one of a DSDML with conventional VTCTs.



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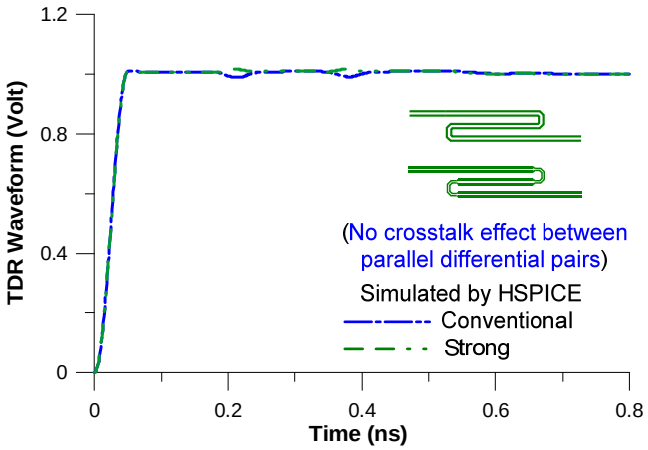


(b)

Fig. 7. Comparisons of TDR waveforms obtained by using different VTCTs and simulators for DSDMLs (a) with and (b) without crosstalk between the pairs of parallel differential lines.

A previous study revealed that the common-mode noise still exists, despite the fact that the total lengths of the two traces of the dual back-to-back VTCTs in a DSDML are the same [4]. The dual back-to-back VTCTs fail to completely eliminate the common-mode noise in a microstrip line structure because the velocities of the even-mode and odd-mode signals differ from each other. The maximum common-mode noise of dual back-to-back VTCTs of a conventional weakly coupled DSDML can be approximated by [4]

$$V_{c,f\_\max} \simeq \frac{V_{in}}{4t_r} \times \min[2T_{d,v}, \Delta t] \cdot \quad (4)$$

The time difference $\Delta t = (\ell / v_{even}) - (\ell / v_{odd})$ is related to the difference between the velocities of the common-mode and differential-mode signals, which propagate along the central differential traces section of the DSDML. In (4), $T_{d,v}$ = ($T_{d,v2}$-$T_{d,v1}$) denotes the difference between the delay introduced by the two traces of the VTCTs, where $T_{d,v2}$ refers to the time delay introduced by the outer trace and $T_{d,v1}$ corresponds to the time delay introduced by the inner trace, as also shown in Fig. 1(a).

The first of the proposed common-mode noise reduction schemes leverages strongly coupled VTCTs instead of the conventional weakly coupled VTCTs because then, obviously, the time difference $T_{d,v}$ becomes smaller. Assume that $T_{d,v}$ for the conventional and strongly coupled VTCTs can be approximated as $\Delta\ell / v_{average} (= \Delta\ell / ((v_{odd} + v_{even})/2))$ [5], where $v_{average}$ is the average velocity of the common-mode and

differential-mode signals and with $\Delta\ell$ the difference of the trace lengths of the VTCTs. Then, $T_{d,v}$ for the conventional and strongly coupled VTCTs can be estimated as 8.3ps and 3.86ps, respectively. According to (4), this will lead to a considerable reduction of the common-mode noise. This is confirmed by Fig. 8, where the peak-to-peak amplitude of the common-mode noise is shown when using strongly coupled VTCTs, compared to the noise obtained by using weakly coupled ones. When adopting strongly coupled VTCTs, the reduction of the peak-to-peak amplitude of common-mode noise is approximately 42%. Additionally, Fig. 8 also compares the simulated results obtained by using the circuit solver, HSPICE, with the simulated results obtained by using the 3D full-wave EM simulator, CST, as such again validating the proposed equivalent circuit models.

Fig. 9 compares the simulated magnitudes of the differential insertion loss ($|S_{dd21}|$), the differential-to-common mode conversions ($|S_{cd21}|$) and the differential return losses ($|S_{dd11}|$) obtained with the two types of VTCTs for the DSDMLs. The figure reveals that the differential insertion losses only vary slightly from low frequencies to 10GHz. The differential-to-common mode conversion is low when strongly coupled VTCTs are utilized. Above 3 GHz, an average improvement of about 10dB w.r.t. the conventional VTCTs is achieved. At frequencies below 3GHz, the differential-to-common mode conversions for both types of VTCTs is almost the same. The use of strongly coupled VTCTs cannot help to reduce common-mode noise at low frequencies, but fortunately, the mode conversion at low frequencies is already low anyway. At frequencies up to 4GHz, the differential return loss is slightly smaller when using strongly coupled VTCTs instead of the conventional ones. At frequencies above 4GHz, the differential return loss is smaller and larger by turns, but with a clear maximum obtained for the case with conventional VTCTs.

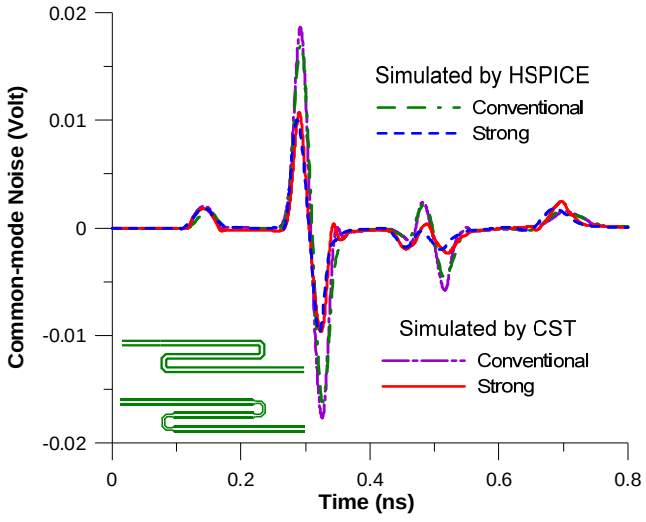
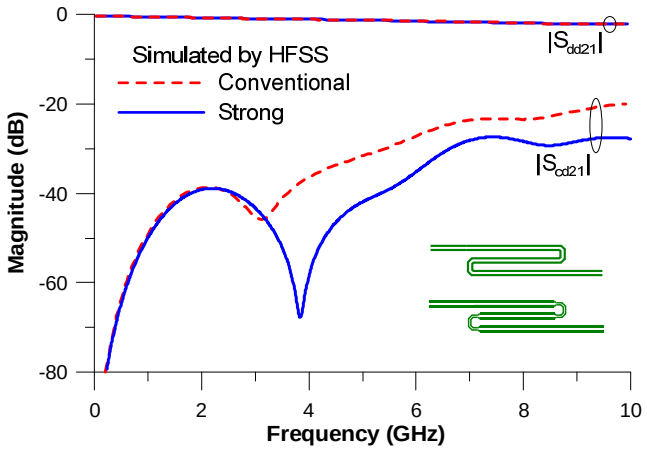


Fig. 8. Comparison of common-mode voltages of DSDMLs obtained using different VTCTs and simulators.



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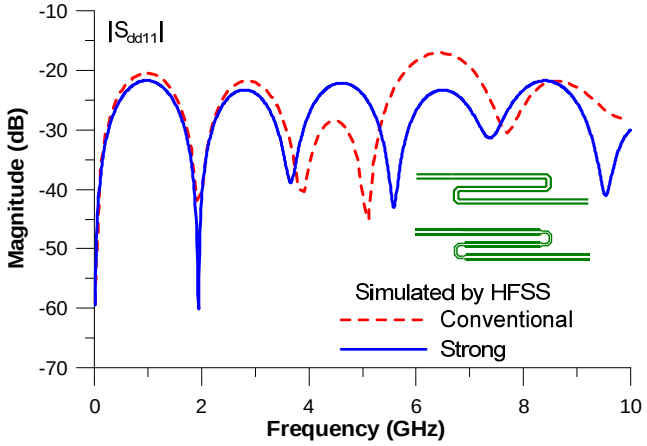


(b)

Fig. 9. Comparisons of simulated (a) differential insertion loss, differential-to-common mode conversion and (b) differential return loss of DSDMLs with the two types of VTCTs.

B. Additional Guard Traces

One of the contributors to the common-mode noise is the length of the parallel differential coupled traces between the two VTCTs. Additional guard traces can reduce the coupling and crosstalk [7] between the differential line pairs. Therefore, to further reduce the common-mode noise, we propose to add guard traces to the conventional DSDML, as presented in Fig. 10.

However, a trace that is grounded at its ends can become a half-wavelength resonator [15]. The resonant frequencies of the guard traces are those at which their length is an integer multiple of half of the wavelength:

$$f_{res.} = k\frac{c}{2d_{via}\sqrt{\varepsilon_{r,eff.}}} \quad k = 1,2,3,... \tag{5}$$

where c is the speed of light, d_{via} is the length of one segment of the guard trace, and $\varepsilon_{r,eff.}$ is the effective dielectric constant of the guard trace. Since, for large values of d_{via}, the resonator causes ringing noise (noticeable in time domain) and high

coupling peaks between the differential traces (noticeable in the frequency domain), serious signal integrity and electromagnetic interference (EMI) problems in high-speed digital circuits [16], [17] can appear. Therefore, to ensure that the first resonant frequency exceeds the highest frequency of interest, i.e. 10 GHz, the length (d_{via}) of one segment of the guard trace is set to 267mil. Using this value, the first resonant frequency is found at about 12.5GHz.

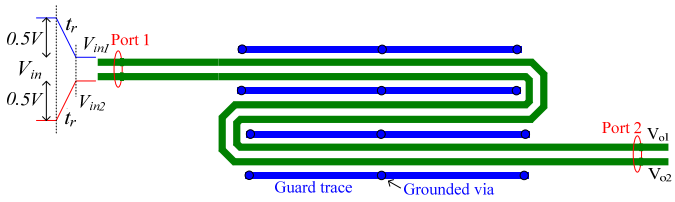


Fig. 10. Second proposed common-mode noise reduction scheme: use of additional guard traces in a conventional DSDML.

According to (4), adding guard traces helps to reduce the time difference (Δt) between the propagation times of the common-mode and differential-mode signals, subsequently reducing the common-mode noise. Indeed, since additional guard traces can weaken the coupling between the differential pairs of the dual back-to-back VTCTs in a DSDML, the coupling coefficient (k) of the differential pairs becomes small. Therefore, the difference between the velocities of the common-mode and differential-mode signals that propagate along the central pair of differential traces of the DSDML also becomes small [18]. The time difference Δt can be expressed in terms of the elements of the inductance matrix ($[L_{ij}]|_{i,j=1,2}$) and the capacitance matrix ($[C_{ij}]|_{i,j=1,2}$), as follows:

$$\Delta t = (\ell / v_{even}) - (\ell / v_{odd}) = (T_{even} - T_{odd})\,\ell = \left(\sqrt{(L_{11}+L_{12})(C_{11}-C_{12})} - \sqrt{(L_{11}-L_{12})(C_{11}+C_{12})}\right)\ell \quad (6)$$

The inductance and capacitance matrices are easily extracted using the simulator Q3D [19]. Table III compares the coupling coefficients and time differences Δt for differential traces without and with guard traces of various widths. It indicates that a wider guard trace yields a smaller time difference Δt .

Fig. 11 presents the simulated common-mode noise ($V_{c,f}$) induced by the central part of a DSDML with guard traces of different widths and without guard traces. It demonstrates that guard traces help to reduce the common-mode noise in a conventional DSDML. Moreover, according to (4), Table III and Fig. 11, a wider guard trace corresponds to a lower peak-to-peak amplitude of common-mode noise. In the simulated example, to obtain the lowest common-mode noise, the width of the guard traces was set to its maximum value, i.e. 9mil, because the minimum spacing (S_g) that can be obtained in PCB manufacturing technology is 4mil.

Table III

Comparison of the coupling coefficients k, and time differences Δt , for differential traces without and with guard traces of different widths.

Related differential trace dimensions (mil)				$\ell = 535mil$	
W	S	S_g	W_g	k	Δt
7.5	9.5			0.102	7.67ps
7.5	9.5	6	5	0.091	5.85ps
7.5	9.5	4	9	0.084	5.15ps

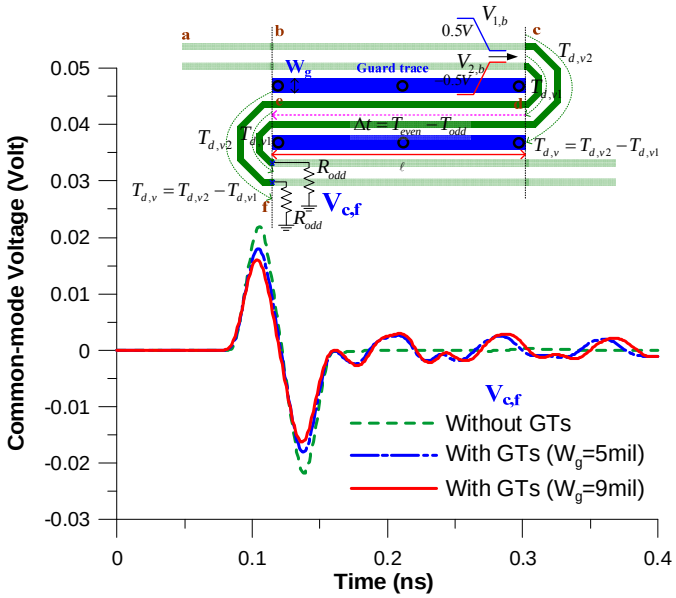


Fig. 11. Common-mode noise ($V_{c,f}$) induced by the central part of a DSDML: comparison between DSDMLs without and with guard traces of different widths.

Now we study the effect of the length of the parallel coupled traces. Fig. 12 shows the common-mode noise for dual back-to-back VTCTs in a conventional DSDML with and without guard traces for various parallel coupled trace lengths (ℓ). Clearly, the additional guard traces in the dual back-to-back VTCTs can reduce the common-mode noise. Without guard traces, the common-mode noise increases with the trace length ℓ up to approximately 1750mm ($\ell_{sat.\_wo}$), which is the saturation value. When guard traces are added, the common-mode noise increases with the trace length ℓ as well, but the noise is less than without guard traces. Additionally, because of the smaller time difference Δt between the central differential traces of the dual back-to-back VTCTs, the trace length at which the common-mode noise saturates is larger. When guard traces are added and as the trace length ℓ increases, the reduction of common-mode noise increases until the length reaches the saturation value ($\ell_{sat.\_wo}$), because the time difference Δt is proportional to the trace length ℓ . For even longer lines, the reduction of common-mode noise decreases again. So, according to this analysis, the reduction of common-mode noise that is achieved by using a weakly coupled

differential serpentine delay line with guard traces is the highest at the saturation trace length ($\ell_{sat.\_wo}$).

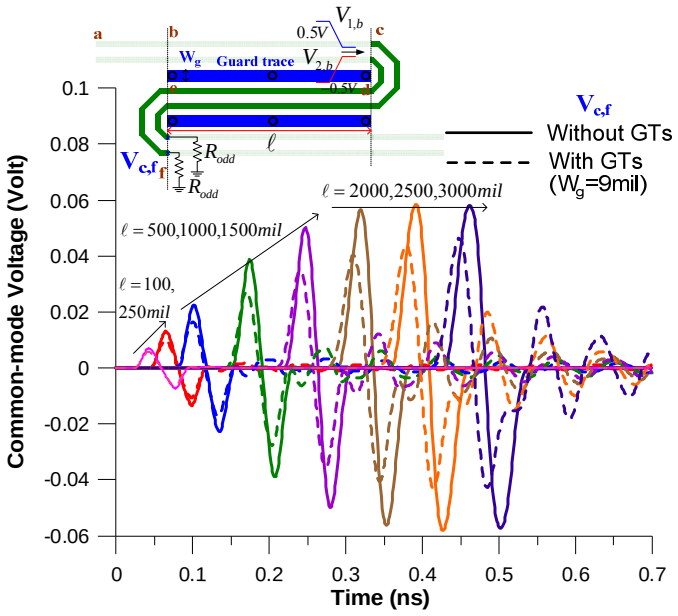


Fig. 12. Common-mode noise ($V_{c,f}$) induced by the central part of a DSDML with and without guard traces for different lengths (ℓ) .

Fig. 13 plots the common-mode noise for a complete conventional DSDML (N = 3) with and without guard traces. This figure reveals that the reduction of the peak-to-peak amplitude of common-mode noise achieved by adding guard traces is approximately 32%.

Now we present the results in the frequency domain. Fig. 14 compares the magnitudes of the differential-to-common mode conversions and the differential return losses for a conventional DSDML with and without guard traces. Fig. 14(a) demonstrates that, up to 10 GHz, the differential-to-common mode conversion for a conventional DSDML with guard traces is less than for a DSDML without guard traces. However, on average, the differential return loss using guard traces exceeds the differential return loss without guard traces. Here, this is due to impedance mismatch. Reduction of the width of the differential traces with guard traces will lead to a better impedance match, as is described in Section IV-C.

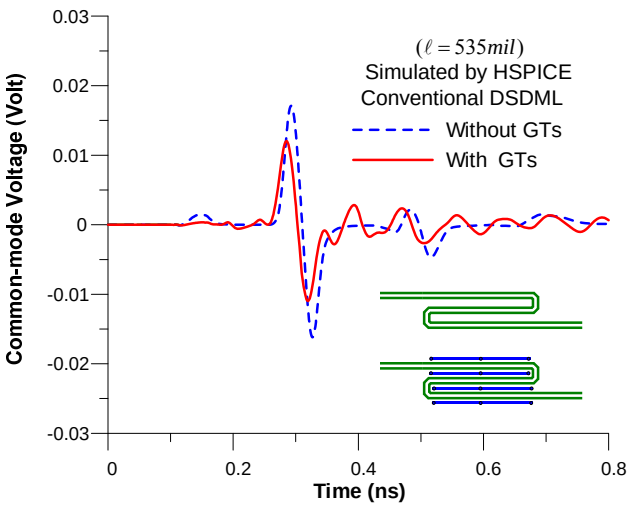
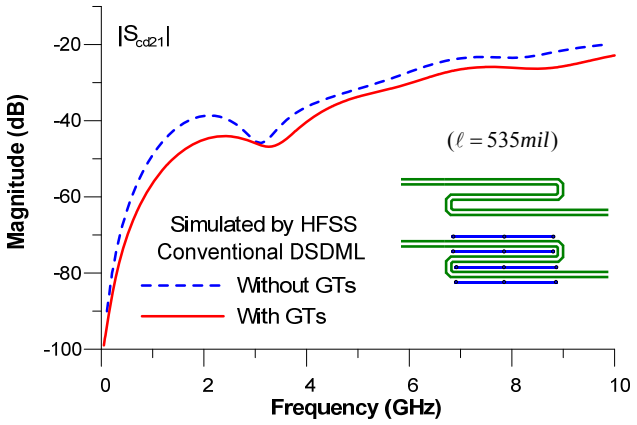
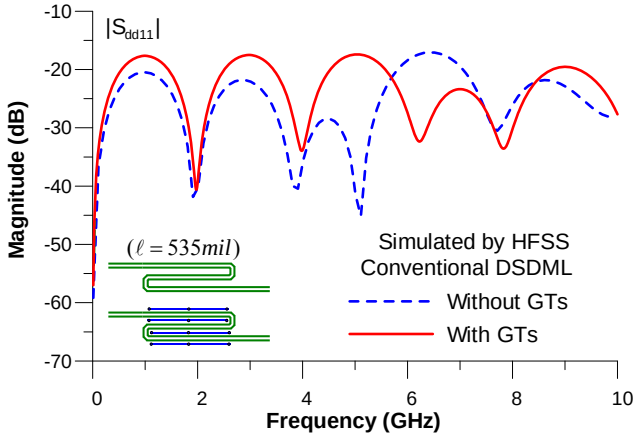


Fig. 13. Common-mode noise for a conventional DSDML with and without guard traces.



(a)



(b)

Fig. 14. Simulated magnitudes of (a) differential-to-common mode conversion and (b) differential return loss for a conventional DSDML with and without guard traces.

Further, the guard traces can mitigate the crosstalk noise between the parallel traces [15]. Now, we investigate the crosstalk effects in a conventional DSDML with and without guard traces. Based on the assumption of weak coupling, lossless lines and matched loads at both ends, crosstalk noise only slightly influences the signal on the active line. With respect to the ramped step voltage V_i on the active line, the saturated near-end crosstalk voltages (for $t_r<2T_d$) in the victim line can be expressed as [20]

$$V_n \approx V_i \times k_{near} = V_i \times \frac{1}{4}\left(\frac{L_m}{L_s} + \frac{C_m}{C_s + C_m}\right) \tag{7}$$

where L and C denote the inductance and capacitance; subscripts s and m indicate self and mutual terms, and k_{near} refers to the near-end crosstalk coefficient.

It is well-known that the near-end crosstalk V_n along the sections of a serpentine delay line accumulates in phase, appearing as a laddering wave in the TDT waveform [21]. The maximum voltage level of the laddering wave is approximately given by

$$V_{laddering,\max} \approx (N-1) \times V_i \times k_{near}. \tag{8}$$

Consider two conductors #1 and #2 that are driven antisymmetrically, i.e. with voltages V_2=-V_1 and charges Q_2=-Q_1, while the two adjacent conductors #3 and #4 form another pair. Via a simple calculation [2], it is readily seen that the self-capacitance C_s=|C_{11}+C_{22}-C_{12}-C_{21}|/2 and the mutual capacitance C_m=|C_{13}-C_{23}-C_{14}+C_{24}|/2. Similar calculations lead to the self-inductance L_s=(L_{11}+L_{22}-L_{12}-L_{21})/2 and the mutual inductance L_m=(L_{13}-L_{23}-L_{14}+L_{24})/2. Inserting both self and mutual capacitances and inductances into (7) allows us to compute the amount of differential near-end crosstalk for differential serpentine delay lines with guard traces.

Fig. 15 compares the simulated TDT waveforms for the conventional DSDML with and without guard traces. Clearly, the inserted guard traces significantly reduce the maximum amplitude of the laddering wave on the TDT waveform. According to (2), the coupling coefficients (k) of the differential traces are 0.1 and 0.087 for the DSDML without and with guard traces, respectively. Additionally, the table in the inset of Fig. 15 compares the simulation results of the maximum voltage level of the laddering wave with the results obtained by (8), demonstrating excellent agreement.

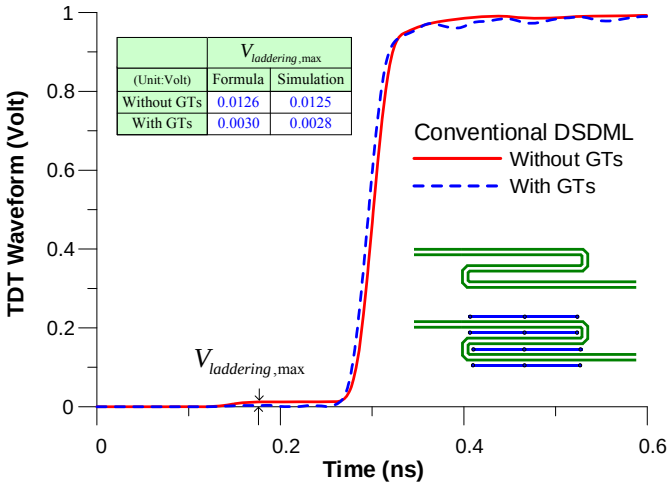


Fig. 15. Comparison of TDT waveforms for a conventional DSDML with and without guard traces.

C. Combination of the two proposed methods

In a conventional weakly coupled DSDML, the strongly coupled VTCTs and guard traces are now combined to optimally reduce the common-mode noise. Figs. 2(b) and 2(c) show the top and cross-sectional views of the combined structure. The proposed scheme, and in particular the presence of the guard traces, has changed the differential impedance (Z_d) of the differential traces adjacent to two guard traces from 100Ω to 95.5Ω. To achieve a differential impedance match, the width (W) of the differential traces adjacent to two guard traces is changed from W=7.5mil, S_g=4mil to W=6.9mil, S_g=4.6mil, as calculated by means of the Q3D simulator. The differential lines, with and without guard traces, are connected via coupled tapers of type 2, as shown in Fig. 2(b), as such keeping the differential impedance matched and minimizing the effects induced by discontinuities. Section III verified the parameters of the equivalent circuit model of the coupled tapers (type 2).

Fig. 16(a) presents the common-mode noise of the DSDMLs with the conventional layout and with the proposed noise-reduction patterns. For clarity of comparison, this section also presents the results of a simulation using only strongly coupled VTCTs in a conventional weakly coupled DSDML (i.e. without guard traces). Clearly, from Fig. 16(a) it is observed that the reduction of the peak-to-peak amplitude of common-mode noise achieved by using both strongly coupled VTCTs and guard traces and also keeping the differential impedance matched, is about 54%. Therefore, combining the two proposed schemes can significantly reduce the peak-to-peak amplitude of common-mode noise in a conventional weakly coupled DSDML.

Next, Fig. 16(b) compares the magnitude of the differential-to-common mode conversions in the frequency-domain, achieved by using DSDMLs with the conventional and proposed patterns. According to the aforementioned analyses, the use of strongly coupled VTCTs reduces the common-mode noise between 3GHz and 10GHz. Guard traces further reduce

the mode conversion within the complete frequency band. Therefore, the combined proposed structures with impedance matching considerably reduce the magnitude of the differential-to-common mode conversion from low frequencies up to 10GHz.

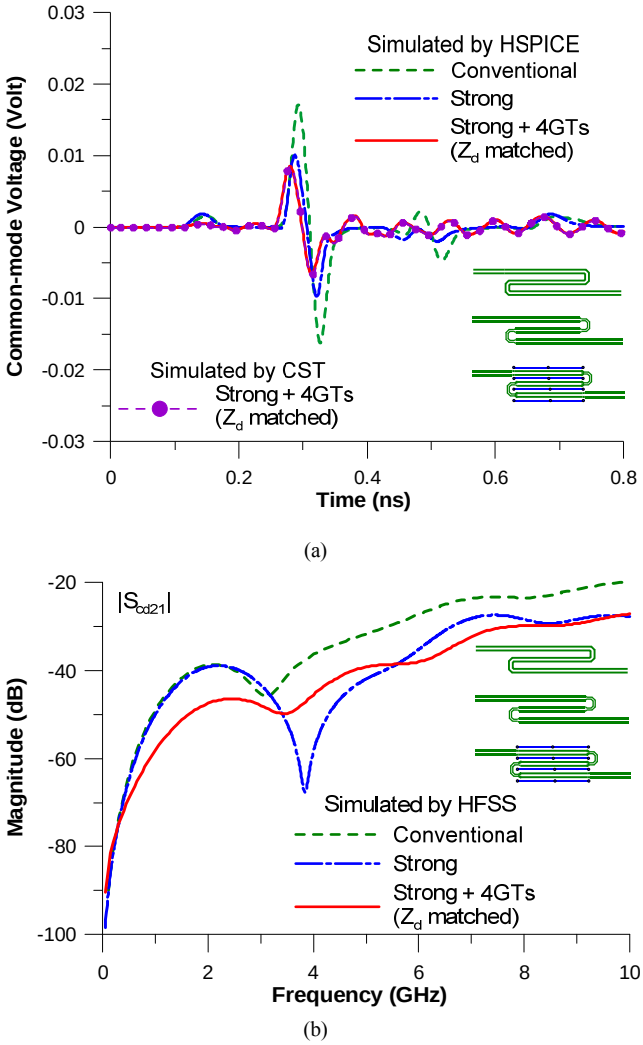


Fig. 16. Simulated (a) time-domain common-mode noise and (b) frequency-domain differential-to-common mode conversion of conventional and newly proposed DSDMLs.

The magnitude of the differential insertion loss induced by the DSDML with the conventional pattern is almost the same as the differential insertion loss coming from the DSDML with the proposed noise reduction schemes, as shown in Fig. 17(a). The differences between the magnitudes of the differential insertion losses are less than 0.4dB. Moreover, on average, the differential reflection losses for the conventional DSDML and the DSDML with the proposed patterns are almost equal, as presented in Fig. 17(b).

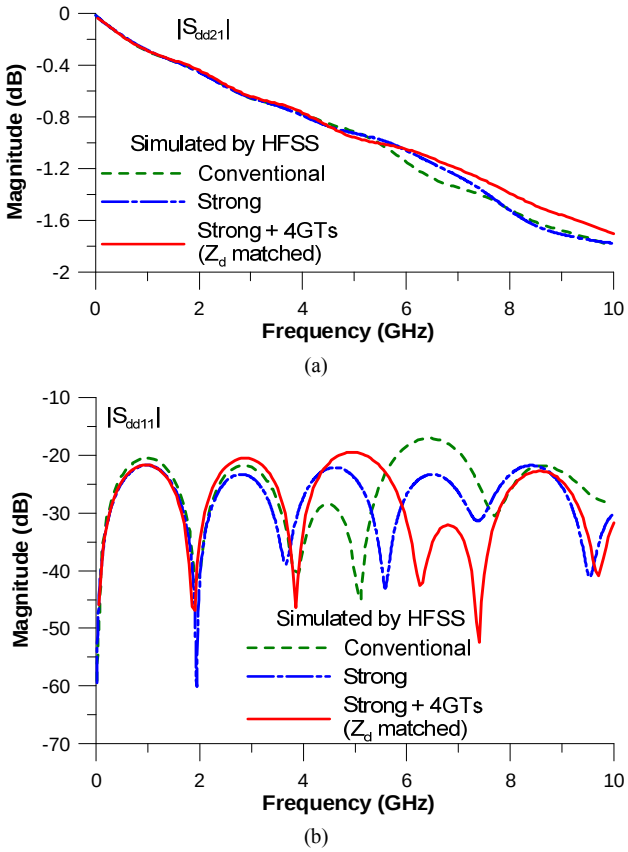


Fig. 17. Simulated (a) differential insertion loss and (b) differential return loss of the conventional and newly proposed DSDMLs.

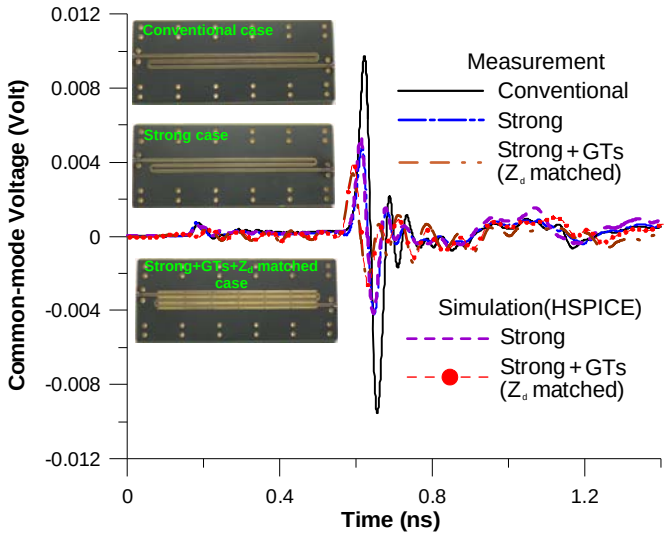
V. Measurement Validation

To verify the common-mode noise reduction achieved by using the proposed structures in a conventional weakly coupled DSDML, simulated and measured results are compared in both the frequency and the time domain. For clarity of comparison, three boards are designed: (1) a DSDML with conventional, weakly coupled VTCTs, (2) a DSDML with only strongly coupled VTCTs, and (3) a DSDML with strongly coupled VTCTs and guard traces while keeping the differential impedance matched. Photographs of the manufactured and measured boards are shown in the inset of Fig. 18(a). The manufactured DSDMLs have cross-sections with W=7.5mil (or 7.2 mil to keep the differential impedance matched when guard traces are added), S=9.5 mil, H=5.5 mil, t=1.7mil, W_s =4 mil, S_s =4 mil, N=3; the substrate material has material parameters ε_r =4.4 and loss tangent=0.02. The distance between the vias along the guard traces are d_{via}=250mil. For ease of measurement and cost considerations in our laboratory, the dimensions ℓ, ℓ_1, d and r_{via} were designed as 1500mil, 200mil, 26mil (26.6mil to keep the differential impedance matched when the guard traces are added) and 6 mil, respectively. To achieve a large noise reduction, the width (W_g) and spacing (S_g) of guard traces

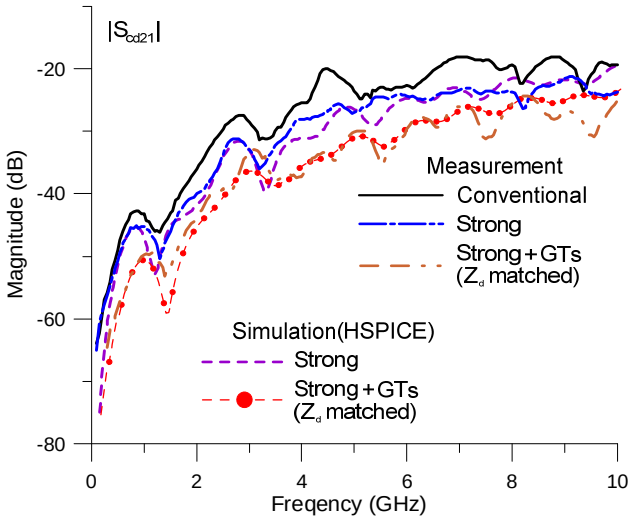
were chosen as 16mil and 5mil, which can still be manufactured in a reliable way. The equivalent circuit modeling method of Section III was applied to the manufactured structures. A time domain reflectometer TEK/CSA8000 and a frequency domain network analyzer Agilent/E5071B are utilized to obtain the experimental results, which are compared to HSPICE simulations of the equivalent circuit models. Both the source resistance and the load resistance were chosen to be 50Ω.

Fig. 18 shows the simulated and measured time-domain common-mode noise and the frequency-domain differential-to-common mode conversions ($|S_{c2d1}|$) for the DSDMLs with conventional VTCTs and with the newly proposed patterns. The results of the simulations agree closely with the measurements. The deviations between simulations and measurements can be attributed to neglecting the semi-rigid coaxial cable in the simulations, to small variations of the material properties of the substrate, to the definition of the port(s), etc. Although these slight discrepancies exist, both simulations and measurement clearly verify the feasibility and usefulness of the proposed common-mode noise reduction schemes for conventional weakly coupled DSDMLs.

Note that, because of practical reasons in our lab, some different geometrical dimensions are used in this section, compared to Section IV. However, the effectiveness of the proposed noise reduction schemes, demonstrated in this section by means of a comparison between measurements and simulation results, shows that the simulation and analysis results for the structures proposed in Section IV, lead to effective performance indices.



(a)



(b)

Fig. 18. Simulated and measured (a) time-domain common-mode noise and (b) frequency-domain differential-to-common mode conversion of conventional and newly proposed DSDMLs.

VI. Conclusions

To reduce the common-mode noise in conventional weakly coupled DSDMLs, this work proposes new noise reduction schemes, leveraging strongly coupled VTCTs and guard traces. The purpose of using strongly coupled VTCTs as a substitute for the conventional VTCTs is to diminish the difference between the delay times introduced by the two traces of the VTCTs, as such reducing the common-mode noise. Adding guard traces reduces the effects of the length of the parallel differential coupled traces and the crosstalk between the pairs of differential traces. The reduction of the peak-to-peak amplitude of common-mode noise, in the time domain, achieved by using only strongly coupled VTCTs, is about 42%. Leveraging both proposed methods, i.e. strongly coupled VTCTs and guard traces, while keeping the differential impedance matched, leads to a noise reduction of about 54%. These values were obtained by means of simulations in HSPICE. Based on frequency-domain simulation by means of HFSS, it is concluded that a considerable reduction of the differential-to-common mode conversion is achieved over a very wide range of frequencies, i.e. 0.3~10GHz, when designing DSDMLs with the two newly proposed noise-reduction methods and while keeping the differential impedance matched. However, careful analysis revealed that the noise reduction obtained by using merely the strongly coupled VTCTs (and no guard traces), was only effective for high frequencies, i.e. in the range of 3GHz~10GHz. Therefore, both time- and frequency- domain results indicate that only by combination of the two proposed schemes, with impedance matching, an optimal noise reduction for a conventional weakly coupled DSDML is achieved. Furthermore, it is important to mention that the differential insertion and the return losses of conventional weakly coupled DSDMLs with

and without the proposed schemes are almost the same. Finally, a favorable comparison between simulated and measured results effectively validates and demonstrates the usefulness of the proposed common-mode noise reduction schemes for conventional weakly coupled DSDMLs.

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REFERENCES

[1] E. Bogatin, *Signal Integrity-simplified*, Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library, 2003.

[2] W. D. Guo, G. H. Shiue, and R. B.Wu, "Comparison between serpentine and flat spiral delay lines on Transient Reflection/Transmission waveforms and eye diagrams", *IEEE Trans. Microwave Theory Tech.*, vol. 54, pp. 1379-1387, April 2006.

[3] C. R. Paul, *Introduction to Electromagnetic Compatibility*, 2nd ed. New York: Wiley, 2006.

[4] G. H. Shiue, J. H. Shiu, Y. C. Tsai and C. M. Hus, "Analysis of common-mode noise for weakly coupled differential serpentine delay microstrip line in high-speed digital circuits," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 3, pp. 655–666, June. 2012.

[5] G. H. Shiue, W. D. Guo, C. M. Lin, and R. B. Wu, "Noise reduction using compensation capacitance for bent discontinuities of differential transmission lines," *IEEE Trans. Adv. Packag.*, vol. 29, pp. 560-569, Aug. 2006.

[6] C. Gazda, D. Vande Ginste, H. Rogier, R. B. Wu, and D. De Zutter, "A wideband common-mode suppression filter for bend discontinuities in differential signlaing using tightly coupled microstrips," *IEEE Trans. Adv. Packag.*, vol. 33, pp. 969-978, Nov. 2010.

[7] F. D. Mbairi, W. P. Siebert, and H. Hesselbom, "On the problem of using guard traces for high frequency differential lines crosstalk reduction," *IEEE Trans. Comp. and Packag. Tech.*, vol. 30, no. 1, pp. 67–74, Apr. 2009.

[8] G. H. Shiue, Y. C. Tsai, C. M. Hsu, and J. H. Shiu, "Common-mode noise reduction schemes for differential serpentine delay microstrip line in high-speed digital circuits," *IEEE 20th Conference on Elect. Performance of Electron. Packag. and Syst.*, San Jose, California , Oct. 2011, pp. 211-214.

[9] "*CST Microwave Studio Manual*" Computer Simulation Technology, Germany, 2003 [Online]. Available: www.cst.com.

[10] W. Fan, A. Lu, L. L. Wai, and B. K. Lok, "Mixed-mode S-parameter characterization of differential structures," in *Proc. IEEE 5th Electron. Packag. Technol. Conf.*, pp. 533–537, Dec. 2003.

[11] High Frequency Structure Simulator. ver. 12, Ansys, Pittsburgh, PA. (2009). [Online]. Available: www.ansys.com.

[12] K. C. Gupta, R. Garg, and I. J. Bahl, *Microstrip Lines and Slotlines*, 2nd ed. Norwood, MA: Artech House, 1996.

[13] C. L. Wang, G. H. Shiue, W. D. Guo, and R. B. Wu, "A systematic design to suppress wideband ground bounce noise in highspeed circuits by electromagnetic-bandgap-enhanced split powers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4209–4217, Dec. 2006

[14] P. Harms and R.Mittra, "Equivalent circuits for multiconductor microstrip bend discontinuities," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 1, pp. 62–69, Jan. 1993.

[15] J.-S. G. Hong and M. J. Lancaster,*Microstrip Filter for RF/Microwave Applications*. New York: Wiley, 2001.

[16] F. D. Mbairi, W. P. Siebert, and H. Hjalmar, "Measurement by vector network analyzer and simulation of crosstalk reduction on printed circuit boards with additional center traces," in *Proc. IEEE Instrument. Measurement Technol.*, Irvine, CA, May 1993, pp. 269–274.

[17] L. Zhi, W. Qiang, and S. Changsheng, "Application of guard traces with vias in the RF PCB layout," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Minnesota, MN, May 2002, pp. 771–774.

[18] G. H. Shiue, C. Y. Chao, W. D. Guo, and R. B. Wu, "Improvement of time-domain transmission waveform in serpentine delay line with guard traces," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, July 2007, pp. 1–5.

[19] Q3D. ver. 10, Ansys, Pittsburgh, PA. (2009). [Online]. Available: www.ansys.com.

[20] C. R. Paul, "Solution of the transmission-line equations under the weak-coupling assumption," *IEEE Trans. Electromagn. Compat.*, vol. 44, no. 3, pp. 413–423, Aug. 2002.

[21] R. B. Wu and F. L. Chao, "Laddering wave in serpentine delay line," *IEEE Trans. Comp., Packag., Manuf. Technol., B*, vol. 18, pp. 644–650, Nov. 1995.