2.5 V passive CMOS mixer with 20 dBm P1 dB compression

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A passive CMOS downconversion mixer with LO buffer is presented in 0.25 μm SiGe BiCMOS using a 2.5 V supply. With a 60 MHz RF signal input, measurements show that the conversion loss is 2.9 dB, the input-referred 1 dB compression point is 20 dBm and the input-referred noise is −146.8 dBm/Hz. Compared to conventional NMOS mixers, the 1 dB compression point is improved by 9.7 dB. The trade-offs and the design of the LO buffer, which has a strong impact on the intermodulation distortion, are also presented.

Introduction: The presented passive CMOS downconversion mixer is part of a broadband power line front-end [1]. This analogue front-end employs a direct conversion receiver (centre frequency 2 MHz up to 60 MHz) with integrated tunable baseband filters (I/Q bandwidth 1, 2, 4 or 8 MHz). In this application, the received spectrum can contain strong interferers (e.g. ham radios) via power lines that act as antennas because most wires are not shielded nor properly twisted. This translates into high linearity requirements and thus a passive mixer is preferred over an active mixer [2].

Mixer design: Passive switching mixers, using NMOS switches only, are widely used. However, the on-resistance of a switch strongly depends on the gate–source voltage and the drain–source voltage. Since the gate–source voltage should be well above the threshold voltage, NMOS switches are used for source/drain voltages down to ground, whereas PMOS switches are used for source/drain voltages up to the supply voltage. Since the mixer should handle strong input signals (almost rail-to-rail), CMOS switches (consisting of NMOS and PMOS transistors in parallel) are proposed. In Fig. 1, the input referred 1 dB compression point (P1 dB) is compared between an NMOS mixer and a CMOS mixer. For the CMOS mixer the simulated P1 dB is 9.72 dB, which is higher than the simulated P1 dB of the NMOS mixer. So consequently the proposed CMOS mixer, shown in Fig. 2, is much more robust against strong interferers than the NMOS mixer.

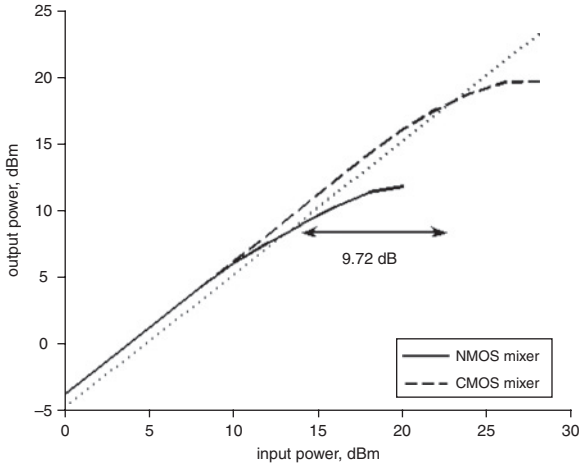

Fig. 1 *Simulated 1 dB compression point: CMOS mixer against NMOS mixer*

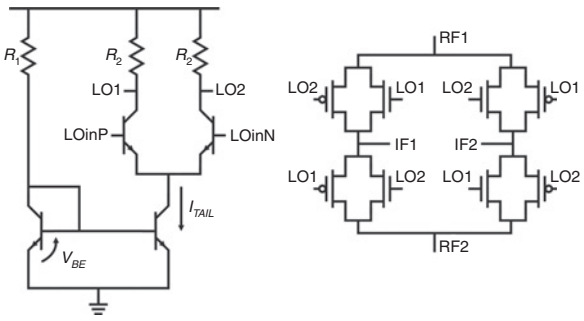

Fig. 2 *Proposed passive CMOS mixer (right) with LO buffer (left)*

The conversion loss of the passive mixer depends on the LO waveform [3]. For a sinusoidal LO the conversion loss is $\pi/4$ (2.1 dB) and for a square wave LO the loss is $2/\pi$ (3.9 dB). Based on the conversion loss one would prefer a sinusoidal LO signal, but the rise and fall times of the LO signal have a strong impact on the intermodulation distortion (IMD) of the mixer [4]. A square wave LO signal is preferred, therefore an LO buffer is required to optimise the switching signal.

LO buffer design: The LO buffer is shown in Fig. 2. The buffer amplifies the LO signal (up to 4 Vpp typically), reduces the rise and fall times (210 ps typically) and applies a stable common-mode voltage (1.5 V). The output common-mode voltage of the LO buffer should be well defined because large variations of the common-mode voltage result in large variations of the IMD for process, temperature and supply variations. For this reason, standard digital CMOS buffers, providing rail-to-rail swings, were avoided. The LO buffer provides a sufficiently stable common-mode voltage without requiring a common-mode feedback loop. With Fig. 2, the dependency on process corners of the common-mode voltage can be determined. The current I_{TAIL} is given by:

$$I_{TAIL} = \frac{V_{DD} - V_{BE}}{R_1}$$

and the differential output voltage V_{DIFF} by:

$$V_{DIFF} = 2R_2 \frac{V_{DD} - V_{BE}}{R_1}$$

The common-mode voltage V_{CM} can be written as:

$$V_{CM} = V_{DD} - \frac{1}{2} V_{DIFF} = V_{DD} - R_2 \frac{V_{DD} - V_{BE}}{R_1}$$

Since V_{CM} does not depend on the absolute value of a resistor, it is less dependent on process corners. The main variation of V_{CM} is caused by the supply voltage V_{DD} and the temperature dependence of V_{BE}. For a ±5% V_{DD} variation, and a junction temperature range from −40 up to 110°C, V_{CM} varies from 1.42 to 1.57 V (or 1.5 V ± 5%) including process corners.

Experimental result: The conversion loss ranges between −2.9 and −4 dB for the whole RF frequency range and for an IF of 2 MHz. The measured P1 dB is 20 dBm (or 6.32 Vpp, exceeding the typical breakdown voltage of I/Os) for an RF frequency of 60 MHz (IF 2 MHz) as shown in Fig. 3. In Table 1, this P1 dB is compared with that of other mixer topologies. Fig. 4 shows the measurement of the third order IMD (IMD3) for a 4 dBm two-tone input signal (±10 kHz spacing) against RF frequency (IF 2 MHz). The IMD3 is below −50 dBc for the RF frequency range of interest (1.6–60 MHz). The measured input referred noise of the mixer is −146.77 dBm/Hz or 10.2 nV/$\sqrt{(Hz)}$.

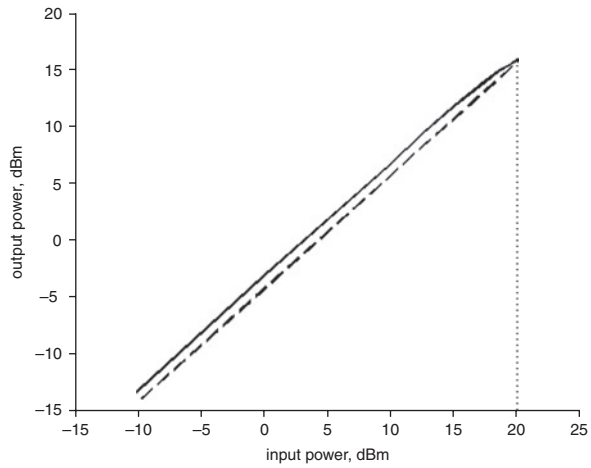

Fig. 3 *Measured 1 dB compression point at RF frequency of 60 MHz (IF 2 MHz)*

Table 1: P1 dB comparison of different mixer topologies

	This work	[5]	[6]	[7]	[8]
Supply voltage (V)	2.5	0.6	1.2	1.2	1.8
Gain (dB)	−2.9	5.4	0	26	16.2
Input referred P1 dB (dBm)	20	−9.2	−1.5	−14	−14
Output referred P1 dB (dBm)	17.2	−3.8	−1.5	12	2.2

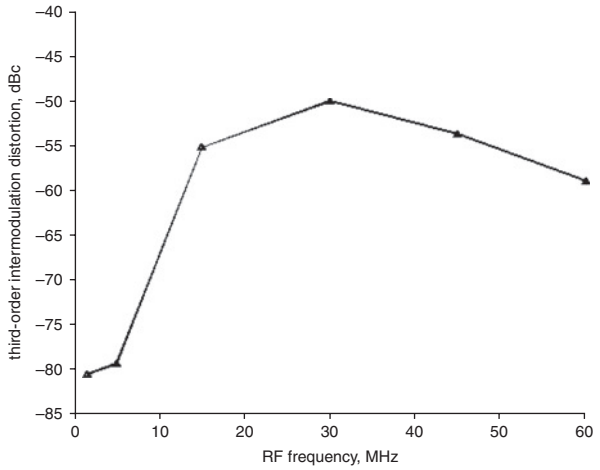

Fig. 4 *Measured third order intermodulation distortion against RF frequency for 4 dBm two-tone input signal (IF 2 MHz)*

Conclusions: A passive CMOS mixer is presented with a P1 dB of 20 dBm and an IM3 below −50 dBc over the RF frequency range (1.6–60 MHz). It is shown that the use of CMOS switches in a passive mixer significantly improves the linearity compared to previously published mixers.

Acknowledgments: This work was supported by the European Commission in the frame of FP6 (POWERNET project). The authors thank the COT Business Unit of Wire line Infrastructure Division of STMicroelectronics for providing technical support, and STMicroelectronics for the chip fabrication.

02 June 2008
Electronics Letters online no: 20081556
doi: 10.1049/el:20081556

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