160 Gb/s Optical Packet Switch Module Employing SOI Integrated Label Extractor

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Abstract

We demonstrate a full functional 1xN optical packet switch employing a Silicon-on-Insulator integrated label extractor combined with a FPGA-based controller. Experimental results show error-free on-the-fly parallel and asynchronous optical label detection, processing and packet switching.

I. Introduction

Several research projects [1] investigated large port-count and low latency optical packet switches (OPS) in order to flatten the inter-cluster data center (DC) network and thus to eliminate the communication bottleneck of current DCs tree topology. However, all the architectures presented employ a centralized controller that leads to port-count dependent reconfiguration time of the switch. Scaling these architectures to thousands ports will result in high switch reconfiguration time and thus high latency. In [2, 3] we numerically and experimentally investigated a novel modular WDM optical packet switch architecture with highly distributed control. Each module includes a label extractor, a switch controller and a 1xN optical switch. The highly distributed control combined with the in-band label processing technique presented in [4] allow for parallel processing operation and thus sub-microsecond inter-cluster communication latency, high throughput and low packet loss. The in-band RF-tone packet labels are extracted from the optical packet by employing an array of fiber Bragg gratings and optical circulators, preventing the integration of the modular switch and making the system bulky and power inefficient. Photonic integration of the label extractor could enable the integration of the OPS module and reduce the overall power consumption.

In this work we experimentally demonstrate the operation of a novel Silicon-on-Insulator (SOI) integrated label extractor based on cascaded microring resonators and evaluate its performance in a 1xN optical packet switch system. We show that the extracted optical label is detected and processed by an FPGA-based switch controller and that the separated packet payload is switched to the appropriate output port of the 1xN optical packet switch. Error-free operation is achieved with 1 dB penalty.

II. Experimental Set-up and System Operation

Fig. 1 shows the experimental set-up. The system operates as follows. The 160 Gb/s packet payload is generated by time multiplexing a 40 Gb/s modulated signal with central wavelength of 1552.5 nm. At the same time three label wavelengths carrying the in-band optical label bits are generated modulating three lasers (LD1=1549.8 nm, LD2=1550.45 nm, LD3=1550.67 nm) by an arbitrary waveform generator according to the RF-tone labeling technique implemented in [4]. In this experiment we considered three RF-tone bits per label wavelength, thus up to 9 bits and 2^9=512 output ports of the 1xN optical switch module can be addressed (N=512). Packet payload with an input power of 2.5 dBm and label with -4.7 dBm of input power (per wavelength) are coupled into the SOI chip using grating couplers.

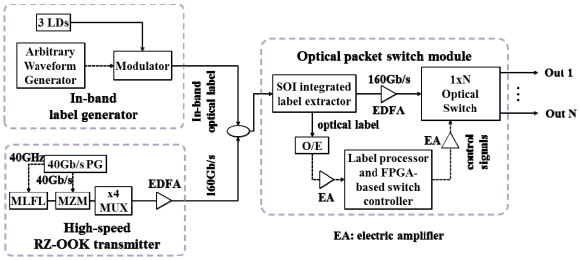

Fig 1: experiment set-up.

This device, shown in Fig. 2(a), consists of four cascaded high-quality factor (Q) add-drop single-ring microring resonators integrated on SOI. The microring is defined as a rib-type waveguide using a partially etch process of 70 nm, and the height and width of the rib are respectively 220 nm and 600 nm [5].

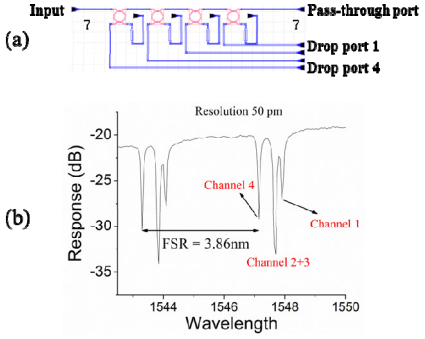

Fig 2: (a) SOI integrated label extractor photograph and (b) wavelength response of the microring resonators array.

The device features 4 drop ports (one for each microring resonator) and 1 pass-through port. Each microring resonator is designed with a radius of 24 µm and a racetrack length of 4 µm in order to obtain a free spectral range of 3.86 nm and low bending losses [5, 6]. This allows extracting efficiently the in-band optical labels (at the drop ports) without distorting the payload (at the pass-through port). Although equally designed, the resonance wavelengths of these adjacent rings may vary up to 1 nm due to local non-uniformities of the etch process. Two of the four resonance frequencies (channels

2 and 3) of the microrings are overlapped as shown in Fig. 2(b), limiting the number of wavelengths of the optical label. Integrated heaters such as in [6] can solve this problem and thus expand the number of useful channels to 4. Once coupled out of the SOI chip, the extracted label is optical-to-electrical converted, while the packet payload is fed into the 1xN broadcast and select optical switch. Label bits are detected and processed by the FPGA-based switch controller that generates the control signals used to set the 1xN optical switch and forward the payload to the appropriate output port. The label generation, the label processor and the FPGA-based switch controller are described in details in [4].

III. RESULTS

The experimental results of the investigated time-slotted system are shown in Fig. 3, 4 and 5.

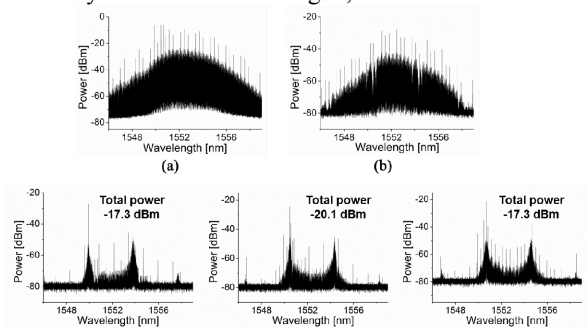

Fig 3: (a, b) optical spectra of 160 Gb/s signal before and after the label extraction; (c-e) optical spectra of the drop ports.

Fig. 3(a-e) show respectively: the optical spectrum of the signal at the input of the SOI integrated label extractor, the spectrum at the pass-through port of the integrated device and the spectra at the drop ports. The power of the payload and labels at the chip output were -11 dBm and -17.5 dBm (per label wavelength), respectively. Thus, the total chip-to-chip losses were around 13.5 dBm including 12 dB of the in/out grating couplers and 1.5 dB chip losses (after crossing 4 rings). Coupling losses could be further reduced to 3.2 dB [7].

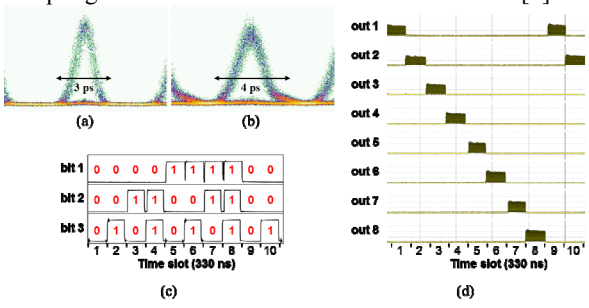

Fig. 4: (a, b) eye diagrams of the 160 Gb/s signal in back-to-back and after the label extraction; (c) recovered label bits; (d) switched packet at the 8 switch output ports.

Fig. 4(a, b) show the eye-diagram of the 160 Gb/s signal before and after the label extractor. Clear open eye is visible after the extractor, although the pulse is slightly broadened, due to the filtering process. Fig. 4(c) shows the time traces of the successfully extracted and detected label bits of one label wavelength. Equivalent results are obtained for the other 6 label bits carried by the two other label wavelengths. In this experiment only 3 label bits have been processed by the FPGA-based switch controller. They are sufficient to address 2^3=8 ports of the employed 1x8 optical switch. Fig. 4(d) shows the dynamic packet switching at the outputs of the 1x8 optical switch according to the label bits encoded destination. Fig. 5 shows the bit-error-rate measurements in back-to-back and after the label wavelength extraction of the four demultiplexed 40 Gb/s signals. It is visible that error free operation is achieved with 1 dB penalty.

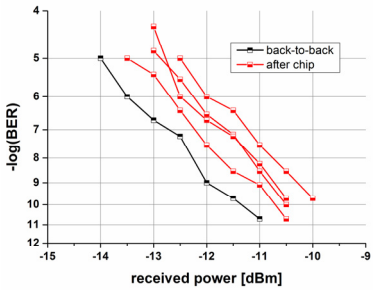

Fig. 5: BER curves in back-to-back (average of the 4x40 Gb/s channels) and after the label extraction of the 4x40 Gb/s channels.

IV. CONCLUSIONS

We investigated a novel SOI integrated label extractor and its operation in a 1xN optical switch module for scalable WDM optical packet switches. We show that the integrated device allows for on-the-fly and asynchronous in-band label extraction without compromising the packet payload. Its CMOS compatibility may allow the integration of the optical label extractor with photo diodes, electronic amplifiers and the switch controller in a single device. As a result, the optical switch module could be improved in terms of dimensions, speed and power consumption.

ACKNOWLEDGMENT

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