# High yield fabrication process for 3D-stacked ultra-thin chip packages using photo-definable polyimide and symmetry in packages

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*Abstract*—Getting output of multiple chips within the volume of a single chip is the driving force behind development of this novel 3D integration technology, which has a broad range of industrial and medical electronic applications. This goal is achieved in a two-step approach: at first thinned dies are embedded in a polyimide interposer with a fine-pitch metal fan-out resulting Ultra-Thin Chip Packages (UTCP), next these UTCPs are stacked by lamination. Step height at the chip edge of these UTCPs is the major reason of die cracking during the lamination. This paper contains an approach to solve this issue by introduction of an additional layer of interposer which makes it flat at the chip edge resulting in Flat-UTCP. In addition to that, randomness in non-functional package positions per panels reduces the overall yield of the whole process up to certain extend. A detailed analysis on these two issues to improve the process yield is given in this paper. 3D-stacked memory module composed of 4 EEPROM dies was processed and tested to demonstrate this new concept of enhanced fabrication yield.

Index Terms— Flat-UTCP, Rotational symmetry, P-o-P alignment, EEPROM memory dies stacking

# I. INTRODUCTION

A reflective approach in miniaturizing the size of electronic packages is to make use of the third dimension by creating vertical interconnections. A tremendous demand for this packaging concept is found in the future generation portable, cheap and smart electronics devices. Hence the large efforts in research are made towards chip embedding and chip stacking using TSV technologies. In the framework of the European Project TIPS, the process for 3D-stacking of Ultra-thin chip packages (UTCP) was developed to provide another way for fabricating devices with a minimal package volume. An overview of this technology resulting in the fabrication of a 300μm thick stack of 4 EEPROM memory dies was previously reported by Priyabadini et al. [1, 9]. This process is based on the first generation of UTCPs which consists of a chip embedding technology within two spin-on polyimide layers [2]. The polyimide membrane of these packages has a total thickness of 40μm, however where the thinned die is embedded a topographical difference of 15 μm to 35 μm exists. Furthermore, the presence of the silicon die results in more and less flexible areas in the interposer. The combination of both mechanical characteristics resulted in an

increased risk of die cracking during the lamination process. This effect has been reported in [9]. In order to control this risk of cracking, the topography can be reduced, thus creating a "Flat-UTCP" (Fig. 1).

According to the stacking concept described in [9], the presence of one non-functional package in the stack makes the whole stack non-functional. To reduce the stacking yield loss due to this effect, a symmetry in package distribution is introduced. In this paper, the development of such Flat-UTCPs with a high stacking yield is discussed.

# II. OVERVIEW: 3D - STACKING OF ULTRA-THIN CHIP PACKAGE PROCESS

The whole process can be divided into two parts.

- UTCP fabrication process
- UTCP stacking process

## A. UTCP fabrication process

In this work, the ICs are thinned down to  $\sim 20\mu$ m and embedded within 3 layers of spin-on photodefinable polyimide(PDPI) thin film. As such, a  $\sim 60\mu$ m thick flexible sheet of Flat-UTCPs is obtained. In order to reduce the costs and achieve a faster production rate, multiple chips are placed on a single processing substrate. An overview of the process flow for multiple Flat-UTCPs is illustrated in Fig. 2. HD Microsystem product PDPI HD4110 [8] is chosen as base material for producing Flat-UTCPs. The basic advantages of this PDPI over other commercially available polyimide precursors are given below which makes it well-suited for this particular application.

- Self-priming property on both glass and Silicon: no adhesion promoter is required before applying it onto the carrier material and/ or silicon chip.
- Thickness range 8-20µm: Easily tunable thickness by selecting appropriate spinning speed to achieve the desired thickness by a single spinning and curing step.
- Negatively photosensitive: advantage in making self-aligned cavities for thin chips in Flat-UTCP fabrication process. Additionally, micro-via realization on the contact pads of many chips well-aligned on the carrier can be done by a single lithography step on the covering polyimide layer.

In a first step, a base polyimide layer is created by spin-coating and curing the HD4110 precursor on the substrate. The substrate is previously coated with a TiW-based alignment layer for precise placement of chips, followed by patterned KCl layer for easy release of packages after fabrication. Next, the thinned dies are placed with an accuracy of less than 10µm using a Tresky fine placer. Their positions are fixed by curing the BCB adhesive layer which is spun prior to the chip placement.

The Flat character of the UTCP packages is created by adding an intermediate layer of polyimide: this layer is spin-coated and patterned by backside illumination through the glass substrate. In this way a self-aligned cavity is created for all the chips at once [6, 10, 15]. After curing, the process continues by applying the top layer and opening the vias to the contact pads, again using photolithography [6-7, 10, 15]. This step can be performed using a single mask for all chips, thanks to the accuracy of the chip placement step. Contact to the external world is made by a fanout metallization on the package which is achieved by deposition and patterning of an 8µm thick copper layer.

Before releasing the sheet of UTCPs from the carrier, the yield per substrate is verified. The overall yield after the full stacking process can be estimated by knowing the position of the non-functional ones per substrate.

However due to high CTE mismatch between this PDPI HD4110 (35 ppm/°C) and the glass carrier (8.7 ppm/°C), shrinkage in the PDPI based package after release from the carrier is un-avoidable. The absolute deformation due to thermal stress increases with an increase in carrier size. This phenomenon makes it difficult to fabricate PDPI based UTCPs with large dimensions: the amount of deformation in the package is too high for the subsequent processes in which mechanical and optical alignment are the most crucial steps.

Considering this issue, fabricating PDPI 4110 based multiple Flat UTCPs in large area is possible, if this shrinkage due to high CTE difference between carrier and PI can be minimized. To achieve a better result, the large area multiple packages can be divided into pseudo-small islands of single packages. This can be achieved during the PI processing phase by introduction of stress-relief grooves in the PDPI layers. These lines are micro-channels which can be patterned with well-defined width, height and length in the PDPI film during flattening layer (2<sup>nd</sup> polyimide) process. Although the effect of this stress-relief grooves is not extensively studied in this paper, a deformation control in polyimide up to a certain extend has been achieved by introducing it in this process. A more detailed explanation of this structure is given in the section III.

#### B. UTCP stacking process

An ideal fabrication process should have the capability to give 100% production yield. However in mass production of the UTCP packages, the yield will be lower. The yield  $\eta$  of the process flow for individual UTCP packages, as described in the above section has been verified to be higher than 85%, based on the measurement of the functionality of several commercially available off-the-shelf ICs (MSP430F1611, nRf24L01, in-house ASIC design, etc) [11]. When *N* UTCP-packages are stacked, one single non-functional UTCP will result in a nonfunctional stack. Therefore the stack yield  $\eta_u$  will drop to  $\eta_u = \eta^N$ . In case of 4 stacked EEPROM dies, the maximum yield will be  $0.85^4$ , or 52%. The effective yield ( $\eta_{eff}$ ) of the whole stacking process will be lower as the above mentioned value needs to be multiplied with the yield  $\eta_S$  of the stacking process itself :

$$\eta_{\rm eff} = \eta_{\rm u} \, {\rm x} \, \eta_{\rm s} \tag{1}$$

Priyabadini *et al* [9] characterized the stacking yield of the non-flat two-layered UTCP to be  $\eta_s \approx 15\%$  only, resulting in an overall yield  $\eta_{eff}$  of 7% following the simple equation on yield calculation (Eq. 1). As discussed in [9], topographical difference in the package (higher package thickness at the chip positions) adds the risk of die cracking during stacking process and this results in a very low  $\eta_s$  value for the conventional 2-PI layered UTCP technology. By adding a third polyimide layer, thus introducing the Flat-UTCP concept, this risk during the lamination process can be reduced and as a consequence the  $\eta_s$  value can be drastically increased.

The above mentioned calculation is based on the process where individual package positions per panel are fixed per substrate. With this type of package distribution, there is no freedom to eliminated the non-functional packages before stacking. However after release of each individual UTCP layer or sheet the functionality of the individual UTCP packages can be checked, and the known-good-packages are allocated. By introducing a new symmetry in package distribution per substrate makes the elimination process easy before lamination. With this symmetry, packages can be selectively aligned on each other after knowing the position of faulty ones. Considering a large scale production process,  $\eta_u$  value can be modified by introduction of this symmetric factor.

On a flat rigid carrier, these multi-UTCP packages can be fabricated with a symmetry in their position. In the previous case[9], packages were arranged in a matrix form with translational symmetry. To eliminate one package, the whole row or column of packages has to be wasted by shifting the position via translation. In the similar situation, a rotational symmetry in the distribution can easily eliminate the non-functional one by selecting the appropriate angle of rotation. As a result, this rotational symmetry in multi-chip packages helps in improving yield in 3D stacking process.

For stacking of packages with different type and dimension of dies, it is more convenient to fabricate them separately on different carriers. Additionally, order of the packages in the stack is an important factor in some critical applications (e.g, inclusion of RF chip package). However, the same concept of rotational principle can be applied in the package orientation. After release from the carrier, a single panel will contain multiple packages with rotational symmetry. By knowing the position of the non-functional ones per panel and number of such positions per batch, they can be easily eliminated from the stack by choosing the proper angle of rotation during package-on-package alignment.

For stacking of 4 packages, they can be fabricated on 4 different carriers where each carrier will contain same packages (chip, and/or metal layout). As demonstrated in Fig. 3, four such panels contain orthogonally rotated packages in a  $2x^2$  matrix form. Each of them has distributed non-functional packages. Taking the advantage of rotational symmetry, the different UTCP sheets are rotated in such a way that the non-functional UTCP's are aligned on top of each other. This results in increasing the number of functional stacks from 1 (stacking in conventional way) to 3 (stacking after selective alignment via rotation).

Following the alignment principle shown in Fig. 3, four of these sheets with two additional flexes on top and bottom are stacked together by vacuum lamination technology[1, 9]. Upilex foil SR 1410 from UBE Inc. of  $25\mu$ m Polyimide/ 9µm Copper and Cu Flex (TW-YE) from Circuit foil of Cu thickness 9µm are used as top and bottom layer, respectively. For package-on-package bonding,  $25\mu$ m thick adhesive films Pyralux LF 100 (from Dupont) is used in between each of these layers during lamination process. The interconnection to each of the embedded packages is made by laser drilling of through hole vias on the external contact pads. This is followed by metallizing the through holes by electroless-galvanic Cu deposition and patterning them using lithography. This results in the production of a ~360 µm thick stacked module with 4 dies embedded inside. The schematic overview of the process flow is illustrated in Fig. 4.

#### III. DESIGN AND FABRICATION PROCESS

This new concept of stacking is demonstrated in lab scale fabrication process by stacking of 4 EEPROM memory die packages. The circuit design of this stacked module is provided by Oticon[14] for the specific purpose of mounting it in a Hearing Aid Device. As per this stack design, package order within the stack is not a factor to be considered. This means packages with four different set of lay-outs can be in any order within the stack. Combining

this with rotation principle during package-on-package alignment, the mask making cost can be reduced by making 4 different layouts on the same mask.

The EEPROM chips are aligned and bonded on the PI substrate in a 2x2 matrix form having a  $90^{\circ}$  rotational symmetry as shown in Fig. 7-a. As a result, this gives rise to 4 EEPROM packages with different metal layouts on the same carrier. After release from the carrier, four of such panels each containing 4 different layouts can be selectively aligned by rotation. This rotation has to be made in such a way that each of the stack will contain 4 packages of different layouts.

The critical factors in making this design and developing this process are to get well-aligned chips placed with proper orientation during chip bonding process and to keep the track of this orientation during whole process. Once the chips are placed precisely on the carrier, the risk factor during the risk of local alignment during via processing and metal patterning on the multiple chips becomes negligible. As a consequence, the multichip UTCP process yield can be increased.

## A. Substrate Preparation:

 $1^{st}$  step of UTCP production process is cleaning of the 2" square glass carriers by conventional process[7]. To align thin-dies on the substrate, a metal pattern is processed by sputter deposition of 50nm thick TiW on the whole surface, followed by patterning it by use of the mask design described in Fig. 5. Together with the alignment marks (Fig. 5-b) for precise placement of chip, some extra lines and alignment structures (Fig. 5-c) are designed on the same mask. A rotational symmetry in the chip alignment mark can be visualized within the 2x2 matrix made by equidistance lines of width 100 $\mu$ m. These lines are designed to transfer it to flattening polyimide layer to create stress-relief pattern. The alignment marks (Fig. 5-c) are used in the next alignment step for making photo-vias on the contact pads of precisely placed chips.

As per the general UTCP process flow, KCl (release layer) is selectively deposited on the substrate by thermal evaporation method. The edges of the carriers are protected from salt by wrapping Aluminum foils which covers 4mm from each side. This prevents direct adhesion of PDPI on the glass edge during base layer spinning due to its self-priming property. A base polyimide layer of film thickness ~18µm 4110 is spin coated with the tunable spinning parameters and fully cured at 375 °C. More details about this process is reported by Wang et. al [7]. Before applying the next thin film on the fully cured base polyimide layer, the PDPI surface is roughened by plasma treatment for a good adhesion.

## B. Multiple Chip placement:

As per the bonding strength experiment[13], benzocyclobutene (BCB) from Dow chemicals is best suited for a void-free Silicon wafer bonding with homogeneous bonding strength. For the thin chip bonding on the polyimide surface, BCB (cyclotene 3022-46) from Dow Chemicals[12] is selected as the bonding material. This BCB is spin-coated on the PDPI surface for getting a uniform thickness. The spinning speed was 500rpm for 10s for uniform spreading, followed by 3000rpm for 30s for thinning down to  $\sim 3\mu$ m. To evaporate some of the solvent content, BCB is pre-baked on the hot plate at 100°C for 1 min in clean room atmosphere.

Some experiments were performed, for placing many thin-chips precisely and void free bonding on the polyimide surface without disturbing chip alignment. Thin chips of different size  $(2.5x2.5mm^2, 2x3.5mm^2, 5x5mm^2)$  and thickness  $(20\mu m, 30\mu m)$  were used for these experiments. The larger the thin chip size (area) is, the stronger is the warpage which is critical to handle ultra-thin chips, intended for flat chip placement. The thin chips are picked faceup by a vacuum tool of Dr. Tresky's fine placer and aligned optically by matching the back side edge of the chip with the alignment mark patterned on the carrier (Fig. 5-b). Although this pattern was covered by the 18µm thick PDPI and 2 µm thick BCB, the visibility was good enough for this alignment. The applied force during placement is 300 g on a 20 µm thick EEPROM die of size  $2x3.5mm^2$  for the duration of 2 min at 150 °C. At this temperature, the underlying pre-baked BCB starts liquefying which is a requirement for pre-bonding of the chip together with BCB on the carrier was allowed to cool down at least for 10 min to avoid thin die shifting. The spacing between chips is maintained at 15mm to eliminate a radial deformation in thickness of BCB which has been noticed due to local heating during chip placement process. If the chips are placed closely enough, the flatness after placement cannot be maintained due to non-uniformity in BCB thickness. After placing 4 chips with a rotational orientation on a single substrate, the BCB is fully cured in 3 steps.

*BCB Pre-curing:* Void-free bonding with BCB is possible if the solvents are sufficiently evaporated during the pre-curing process. This cycle consists of temperature ramping up to  $150 \,^{\circ}$ C with an average heating rate of  $4 \,^{\circ}$ C/min, 30 min holding at  $150 \,^{\circ}$ C, cooling down to room temperature. At this stage, BCB starts flowing and most of the solvent material gets evaporated. There is a chance of chip movement and getting voids under the chip during this phase. This can be controlled by applying a pressure of 1 bar/die on the top of the chip from the beginning till the hot plate cools down to room temperature. For pressure uniformity, the 4 chips on the carrier is covered by a glass carrier with a 20µm thick Teflon layer as an intermediate layer. A load equivalent to the pressure for 4 dies is applied on top of the covering glass. Teflon layer prevents the BCB at the bonding area to come in direct contact with the covering materials. With this combination, a minor shift of thin die has been noticed several times. The reason is thinness of the Teflon sheet and porosity in it, which allows BCB overflow on the entire chip surface. Although a load is applied from top, the movement of this layer together with chip cannot be completely avoided. Therefore, the Teflon sheet is attached to the covering glass by a thermal release tape which can hold it during the complete temperature cycle. The whole stack is well aligned and placed on the hot plate as shown in Fig. 6 before starting the curing process.

*BCB Half-curing:* With the same heating profile, the BCB was half-cured at 210 °C for 30 min with a pressure of 1.7 bar/die. At the end of this process, the BCB changes to semi-solid phase.

*BCB full-curing:* For final bonding of chips onto the PDPI substrate a pressure of 2 bar/die is applied on the top and BCB is cured at 260  $^{\circ}$  for 1 h. This full-curing process is performed in a conventional oven with N<sub>2</sub> ambient.

Fig. 7 shows the final result of the chip placement and bonding experiments implemented in producing 4 wellaligned chips on a single substrate. The reproducibility of the process has been verified by repeating this process in fabrication of 14 of such samples for multi-UTCP fabrication process. As a standard technology, the same surface roughening treatment is repeated before applying next layer for a good adhesion.

# C. Flattening and covering PDPI layer:

The chip thickness together with BCB under it is measured to determine the PDPI thickness required for making the flattening layer. The corresponding spinning speed is determined from the spin curve[8]. The maximum thickness which can be achieved by spinning and curing this PDPI is  $20\mu m$ . Multiple spinning steps are required to cover the chip with thickness more than  $25\mu m$  for complete planarization. In this particular case, the chip + BCB thickness was ranging from 21-22  $\mu m$ . A single PDPI spinning step was enough to make the flattening layer. A mismatch of 1-2  $\mu m$  can be planarized during the final PDPI layer processing. The following sequence of processing steps was executed:

- Spinning PDPI HD 4110 for 10s at 1000rpm for uniform spreading, followed by 1 min at 1500rpm. Pre-baking on hot plate for 4 min at 115 °C. Minimum 5 min cooling time.
- Taking the advantage of negative photosensitivity, backside illumination of UV enables PDPI patterning for self-aligned cavity for chips. In this case, the Si-chip attached to the carrier acts as a mask when the assembly is UV exposed from the back of the carrier (step3, Fig. 2). In addition to that, the equidistant lines with a width of 100 µm, present on the carrier (Fig. 5-c) are patterned on the same layer of polyimide in the same process. The UV exposure time was optimized as 2 min with a light intensity of 10mW/cm<sup>2</sup> for this backside illumination process. The light has to pass through the transparent glass carrier of thickness 0.7mm and a semitransparent full cured thin film of base PDPI layer. After exposure, minimum 10 min holding time before development to stabilize the polymerization process is required.
- PDPI development in dedicated developer PA-400D and PA-400R from HD Microsystems. In this process, the sample is immersed in a beaker containing PA-400D for 1 min with ultrasonic agitation, followed by 30 s in a 1:1 solution of PA-400D and PA-400R, 30s rinsing in PA-400R, finally drying by N<sub>2</sub> blow-off. Post development waiting time minimum 10 min.
- Full curing of polyimide film inside vacuum chamber with same set of parameters as for base PDPI layer.
- PDPI surface roughening by RIE process.

The EEPROM die contains 8 contact pads of size  $103 \times 103 \mu m^2$  with  $90 \times 90 \mu m^2$  pad opening, out of which 7 are used for making interconnection in the 3D-stack of packages. The micro-vias of size  $50 \times 50 \mu m^2$  are opened on the contact pads of the 4 chips by a single lithography step. The cover PDPI layer is spin-coated and developed with the following set of parameters to get a final thickness of  $15 \mu m$  after curing.

- Spinning PDPI HD 4110 for 10 s at the speed 1000 rpm for uniform spreading, followed by 1 min at 2000 rpm.
  Pre-baking on hot plate for 4 min at 115 °C. Minimum 5 min cooling time.
- UV exposure for 38 s with light intensity 4.9mW/cm<sup>2</sup> after alignment of the sample under the via mask. The alignment marks used for this process are illustrated in Fig. 8-a. Minimum 10 min holding time after exposure.
- Same development, full curing and after curing surface roughening step as for previous PDPI layer.

# D. Metallization and Patterning:

Each sample now contains 4 embedded thin dies with micro-vias open on the Ni/Au finished contact pads. For making metal fan-out from the contact pad of the chip to the external surface, the first step is a seed layer deposition

on the entire sample. This is done by loading all the samples together in a sputtering machine for sputter deposition of TiW(50nm)/ Cu(1 $\mu$ m). In the next step, the copper is thickened up to 8 $\mu$ m by a conventional panel plating process. The metal is finally patterned by using a standard lithography and wet chemical etching process. The mask used for the metal patterning contains four metal layouts with orthogonal symmetry as per the chip orientation on the carrier.

The spacing between the center of each Flat-UTCP and the stress-relief groove is maintained at 7.5 mm. The mask used for metal patterning on UTCPs contains the lines of 100 $\mu$ m width which protects the copper deposited inside the grooves. After metal patterning, the profile of this stress-relief groove is studies by optical microscope and wyko profilometer (Fig. 10). The copper width varies from 80 $\mu$ m (top) to 100 $\mu$ m (bottom) in this groove. The polyimide profile and copper profile are created by two different ways of UV exposure and photolithography. The 1<sup>st</sup> one is by backside illumination and 2<sup>nd</sup> one by front side UV exposure. The step height at this region after the 1<sup>st</sup> lithography step is same as the flattening layer thickness, 20 $\mu$ m. After metal patterning, the cavity gets filled with copper up to 8 $\mu$ m. This finally gives a step of height 10-12 $\mu$ m from copper (bottom) to the polyimide (top).

# E. Functional package mapping:

ESD pad on the chips are tested after UTCP fabrication process to map the good ones per sample before going to the stacking process. 8 separate substrates each carrying 4 UTCPs have a random yield which is 75% in 3 panels (3 functional out of 4) and 100% in the rest of the 5 substrates. This in average gives a UTCP yield ( $\eta$ ) of 90%. With the mapping of functional ones and taking the advantage of rotational symmetry in the package distribution, the layer by layer rotation of the released UTCP panel can be easily set to get maximum number of working stacks.

## F. Deformation after UTCP release:

The copper alignment mark positions at the extreme corners of the UTCP panels are checked before its release from the rigid carrier. This helps in keeping the track of deformation in package and stack after complete fabrication process. The PDPI has a good adhesion at the edge of the carrier. For the release of this package, a cutting is made on the polyimide layer covering the release layer. YAG laser is used for the precise release of the package. The back side of the package facing the salt can be rinsed afterwards by DI water.

The shift in alignment mark position(inward) after release from the carrier is the sign of deformation in package. This value has been found the same even after laminating them to stacked packages. In the current process, where stress-relief grooves are introduced in the polyimide film, a linear shrinkage of 0.3% has been observed. This is comparatively less as compared to 1% which was found in larger sample of size 8x8cm<sup>2</sup> fabricated on a 4" square glass substrate[10]. To apply this method in an industrial level fabrication process more investigation should be done on incorporating this stress-relief patterns in large area package production process.

## G. Lamination and Interconnection process:

After release, the UTCP stacks are fabricated as per the alignment concept and following the process flow shown in Fig. 3 and Fig. 4, respectively. The layer by layer flexes are laminated temporarily on hot plate after optically aligning them (Fig. 4, step1). The step by step process for alignment is given below.

• All the UTCP flexes are baked on a hotplate for 2 min at 120℃

- Roll Lamination of 25µm thick LF 100 adhesive glue onto 9µm thick Cu sheet (bottom layer of stack) on a hot plate at 90 °C for 10s.
- Placing the 1<sup>st</sup> layer of multi-UTCP on the adhesive layer and next LF 100 layer and laminating them together at 90 ℃ for 10 s on the hot plate.
- Aligning next UTCP layer wrt to previous layer with necessary angle of rotation which helps in reduction of the non-functional stack count.
- Temporarily fixing the position of the packages by local heating of adhesive at certain points.
- Repeating the adhesive glue lamination and UTCP sheet alignment by rotation process up to the final covering layer Upilex foil of 25µm Polyimide/ 9µm Copper.
- The whole stack is then laminated by vacuum lamination technology as reported by Priyabadini et. al. [9].

The through hole via (THV) drilling at the stacked contact pads is done by YAG Laser. The through holes are plated by electroless and galvanic copper deposition. The top and bottom side Copper patterning is made by dry film resist based lithography and wet chemical etching process. This THV technology for making interconnection is discussed in detail in [9]. The fully fabricated stacked EEPROM UTCPs is shown in Fig. 11. The complete laminate contains 4 stacks in 2x2 matrix form and each stack with having 4 Flat-UTCPs.

# IV. RESULT AND YIELD ANALYSIS:

The cross-section of stacked package (Fig. 12) shows the chip edge region of the 3D-stacked Flat-UTCPs. The 3layered polyimide packages of thickness ~50µm result in an entirely flat package at the chip edge due to inclusion of an extra flattening layer. As a result, this makes the whole stack flat with a total thickness of 360µm. The difference in two versions of stack (as shown in Schematics diagram, Fig.1) can be visualized from the X-ray CT scan pictures (Fig. 13). This analysis gives a clear picture of the metal profile within the stack. A close-up view on the copper routing from the contact pad of the chip to the plated through hole is shown in Fig. 13-b,c. The copper patterned on the packages follows the topography of the underlying layer. This can be verified for the two cases by wavy copper routing at the non-flat chip edge(Fig. 13-b) and straight ones in case of flat chip edge (Fig. 13-c). The micro-via pattern on the contact pads of the chip are different in both the cases. 1<sup>st</sup> one is by laser drilling process where the via is defined on the non-photodefinable PI surface by use of YAG laser [2]. The via size is depended on the beam shaping optics of the laser which is quite smaller and less reproducible as compared to that in case of photo-vias defined on PDPI. The copper track from the photo-via on the contact pad to the chip edge (dotted region in Fig. 13-c) is shown in the cross-section picture (Fig. 13-d).

In the whole process, chip placement is the most critical step which brings down the average yield ( $\eta$ ) of the current UTCP process to 90%. For stack yield( $\eta_u$ ) can be estimated as 0.9<sup>4</sup> or 0.65. Following the rotational symmetry in P-o-P alignment, the  $\eta_u$  value can be calculated as 87.5% (7 working stacks out of 8). The ratio of these two values can be denoted as rotational symmetric factor ( $\eta_r$ ) in the package. For stacking of higher number(N) of packages, this symmetric factor ( $\eta_r$ ) can improve the overall yield ( $\eta_u$ ) by applying rotation law. In that case, the packages has to be arranged in circular pattern on a round carrier which makes the rotation easier. Depending on the

package size, deformation limit and mass production facility, the size of the carrier can be selected. Additionally, use of circular carrier will help in achieving thickness uniformity in the spin-on layers used in package fabrication.

In the current process, the order of packages in the stack was not considered. Therefore the different metal layouts are designed on the same mask and transferred onto the packages. This results in producing UTCPs of different metal layout on the same panel. However this approach adds another risk to the rotation law when a number of packages with same metal layout on different panels becomes non-functional. Although theoretical calculation gives 7 working stacks out of 8, this number drops down to 6 due to this above said risk. To apply this approach in production process, it is recommended to fabricate packages of the same type on a single carrier.

From all the above said calculations, the estimated  $\eta_u$  value was 75% (6 working stacks out of 8). ESD pad test resulted in 5 working out of 8 stacks which gives  $\eta_{eff} = 62.5\%$ . From equation 1, the stacking yield ( $\eta_s$ ) can be calculated as 83% which shows a significantly high impact of the Flat-UTCP in the whole process as compared to 15% in case of conventional UTCP stack.

# V. CONCLUSION:

An improved technology to produce 3D stacks of ultra-thin chip packages with higher yield has been reported in this paper. The most important factors that affect the overall yield in this UTCP stacking process are flatness at the chip edge of the package and symmetry in the package distribution. The Flat-UTCP fabrication process includes the risk of thin chip handling and polyimide deformation due to CTE mismatch. To make this process more fast and accurate, development work still ongoing by using thin chip on carrier and/ or use of photo patterned BCB as glue material. More investigation can be made for deformation control in the package by using different stress-relief patterns which in turn facilitate the large area production of Flat-UTCPs using PDPI. Thermo-mechanical behavior of these thin stacks are going to be studied in near future and will be reported in soon.

#### **References:**

- S. Priyabadini, A Gielen, K. Dhaenens, W. Christiaens, S. Van Put, G. Kunkel, A.E. Petersen and J. Vanfleteren, "3D stacking of ultra-thin chip packages: An innovative packaging and interconnection technology", *Proc.* 44<sup>th</sup> International Symposium on Microelectronics(IMAPS 2011), Long Beach, CA, October 9-13, 2011, pp. 463-468
- 2. W. Christiaens, E. Bosman and J. Vanfleteren, "A Novel Polyimide-Based Ultra-Thin Chip Packaging Technology", *IEEE transactions on components and packaging technologies*, vol. 33, no. 4, 2011, pp. 754-760
- J. Govaerts, E. Bosman, W. Christiaens, and J. Vanfleteren, "Fine-Pitch Capabilities of the Flat Ultra-Thin Chip Packaging (UTCP) Technology", *IEEE\_Transactions on Advanced Packaging*, vol. 33, Issue. 1, Feb 2010, pp. 72-78
- 4. J. Govaerts, W. Christiaens, E. Bosman, and J. Vanfleteren, "Fabrication processes for embedding thin chips in flat flexible substrates," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 1, Feb. 2009, pp. 77–83

- J. Govaerts, W. Christiaens, E. Bosman, and J. Vanfleteren, "Multiple chip integration for flat flexible electronics," *Proc.* 7<sup>th</sup> *IEEE Conf. Polymers Adhesives Microelectron. Photonics (Polytronic 2008)*, Aug. 2008, pp. 1–5
- T. Sterken, M. Op de Beeck, F. Vermeiren, T. Torfs, L. Wang, S. Priyabadini, K. Dhaenens, D. Cuypers and J. Vanfleteren "High Yield Embedding of 30μm Thin Chips in a Flexible PCB using a Photopatternable Polyimide based Ultra-Thin Chip Package (UTCP)", *Proc. 45th International Symposium on Microelectronics* (*IMAPS 2012*), San Diego, CA, September 9-13, 2012, pp. 940-945
- L. Wang, T. Sterken, M. Cauwe, D. Cuypers, and J. Vanfleteren, "Fabrication and Characterization of Flexible Ultrathin Chip Package Using Photosensitive Polyimide", *IEEE Transactions on Components, Packaging and Manufacturing technology*, Vol.2, no. 7, 2012, pp. 1099-1106
- HD 4110, datasheet as provided by HD microsystem (http://hdmicrosystems.com/HDMicroSystems/en\_US/index.html)
- S. Priyabadini, T. Sterken, L. Van Hoorebeke and J. Vanfleteren, "3D stacking of ultra-thin chip packages: An innovative packaging and interconnection technology", IEEE transactions on Components, Packaging and Manufacturing Technology, 2013 (available online, DOI: 10.1109/TCPMT.2012.2234830)
- S. Priyabadini, T. Sterken, L. Wang, K. Dhaenens, B. Vandecasteele, S. Van Put, A.E. Petersen, J. Vanfleteren, "An approach to produce a stack of photo definable polyimide based flat UTCPs", *Proc. 4<sup>th</sup> Electronics Systems and Integration Technology Conference (ESTC 2012)*, Amsterdam RAI, The Netherlands, September 17-20, 2012, pp PA6\_2(1-4)
- T. Sterken, F. Vermeiren, P. Tremlett, W. Christiaens, J. Vanfleteren, "Embedding Thinned chips in Flexible PCBs", *Proc. 4<sup>th</sup> Electronics Systems and Integration Technology Conference (ESTC 2012)*, Amsterdam RAI, The Netherlands, September 17-20, 2012, pp PA10\_4(1-4)
- 12. Cyclotene 3000 Series, datasheet as provided by Dow Chemical (http://microchem.com/PDFs\_Dow/cyclotene\_3000\_dry\_etch.pdf)
- 13. F. Niklaus, P. Enoksson, E. Kaelvesten and G. Stemme, "Low-temperature full wafer adhesive bonding", *Journal of Micromechanics and Micro engineering*, Vol. 11, 2001, pp. 100–107
- 14. Oticon (http://www.oticon.com/)
- S. Priyabadini, T. Sterken, M. Op de Beeck and J. Vanfleteren, "Photo-definable polyimide-based Flat UTCP technology for 3D-stacking application" Smart Systems Integration (SSI 2013), Amsterdam, The Netherlands, March 13-14, 2013, pp. 1-8



Figure 1. Schematic overview of stacking of Flat-UTCP approach



Figure 2. Process flow for multiple Flat-UTCPs



**Figure 3.** An example of rotational symmetry in packages : 3 non-functional UTCPs are aligned on top of each other which gives rise to one non-functional stack in total, instead of 3 non-functional stacks



Step1. Aligning the 4 layers of orthogonally rotated multiple UTCPs and additional Cu flexes on top and bottom with LF 100 as bonding material in between each two layers



Step2. Stacking of all layers by vacuum lamination technology

Step3.Singulated stacks after making through hole via interconnection by Laser drilling, followed by plating and patterning

Figure 4. Schematic overview of stacking of flat UTCPs process flow



**Figure 5.** (a) Design made for precise placement of 4 chips on 1<sup>st</sup> PI layer, stress-relief grooves on 2<sup>nd</sup> PI layer, alignment patterns for photo-via definition on 3<sup>rd</sup> PI layer (b) Chip alignment pattern defined on the carrier by TiW patterning, (c) Pattern on carrier for stress-relief groove on flattening layer of UTCP (left), alignment marks during photo-via definition on the contact pads of multiple chips by photolithography step(right)



**Figure 6.** Schematic cross-sectional view of the stack build up with temporary carrier and release layers over the chip during the bonding process



**Figure 7.** (a) Orthogonally rotated 4 chips placed precisely on semi-transparent PDPI 4110 base layer looking through the alignment pattern on the 2" glass carrier. (b) Back side view of chip edge wrt the TiW-alignment mark in the design file and the corresponding view through the glass carrier; placement accuracy of ~  $10\mu$ m is achieved.



**Figure 8**. Alignment mark (a) designs on the via mask (blue) and on the carrier(black), (b) Defined on the PDPI layer after via processing, (c) and (d) Micro-via of size  $50x50\mu m^2$  opened on the  $90x90\mu m^2$  size contact pads of the multiple chips the placed on the same substrate. Shifting of via position from the center of contact pad is a consequence of chip misalignment.



**Figure 9**. Four different metal layouts (L1-L4) on the same mask with orthogonal orientation to facilitate high yield during stacking process.



Figure 10. Top side view of the stress-relief pattern (a) copper track width measurement by optical microscope, (b) step height measurement by wyko surface profilometer



**Figure 11**. Front side view of 2x2 matrix of 4 stacks of EEPROM UTCPs (16 Flat-UTCPs in total)

		<b>P</b> 4
	Length = 52,30 μm	1 1
1	Length = 51 73 um	P3
Length = 363,82 µm		
	Length = 50,59 µm	<b>P2</b>
	Length = 50,03 µm	<b>P</b> 1
	and the second	Ne sano
*	23	

**Figure 12**. Cross-sectional view of stacked flat UTCP showing uniform package thickness at the chip edge.





**Figure 13:** (a) X-ray CT scan picture of one stacked UTCP showing only conductive lines within the stack, (b, c) close-up view at the Cu routing from the chip contact pads to the TH pads of stack of conventional UTCPs (non-flat) and Stack of Flat-UTCPs, respectively, (d) cross-section view of one the package within the stack at the region marked in (c).