REAL TIME DIGITAL EMULATION OF COPPER ACCESS NETWORKS FOR VDSL APPLICATIONS

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ABSTRACT

The wide scale deployment of fibre optic backbone networks is already a fact, yet, for the last mile(s) up to the subscriber, the reuse of current copper access networks is standard practice. In most cost studies, the so-called 'last mile', connecting individual houses, takes the biggest share, and the reuse of the twisted pair telephony cables, which are already in place, is favored. This explains the success of Digital Subscriber Line technology (xDSL), which can support megabit data rates over the phone-lines connecting nearly every home. Copper pair networks were designed for voice traffic with a limited bandwidth of 3.4 kHz, but HSDL, ADSL, T1, E1 and VDSL may exceed voice bandwidth more then a thousand fold. The efficient exploitation of copper pair access networks at high bandwidth therefore presents a formidable challenge, and the capability of accurately analyzing and emulating specific access line cables and topologies has become quite important.
A reconfigurable digital module for the emulation of the physical layer of communication systems is presented. The feasibility of such a system is demonstrated through the development of a proof-of-concept digital access loop emulator for VDSL applications within the framework of the European MEDEA+ project MIDAS [7]. This prototype instrument can emulate (i.e. imitate in real time) quite complex phone line networks in a lab environment. So, for the first time, cable measurements can be made in the field and later transferred to the emulator, to replicate field installed phone lines precisely.

1. PROBLEM ANALYSIS

1.1. Access loop topologies

The connection between the xDSL subscriber and the local exchange usually consists of a cascade of twisted pair lines, which can vary in type and length. In some cases open ends of unused twisted pair, so-called bridged taps, are connected in parallel somewhere along the loop (Figure 1) .

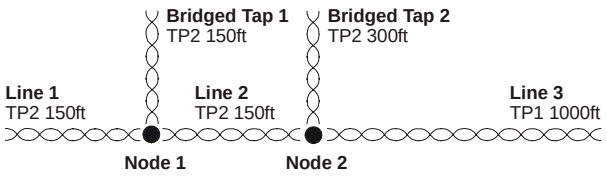

Figure 1 : ANSI VDSL4 Test Loop Topology

A topology of lines and bridged taps gives rise to echoes or reflections, which interfere with the original signal. The insertion loss of a typical line topology is shown in Figure 2. A highly irregular low pass pattern appears, which illustrates the complex task xDSL equipment has to perform to provide reliable, high-speed data transmission over this medium.

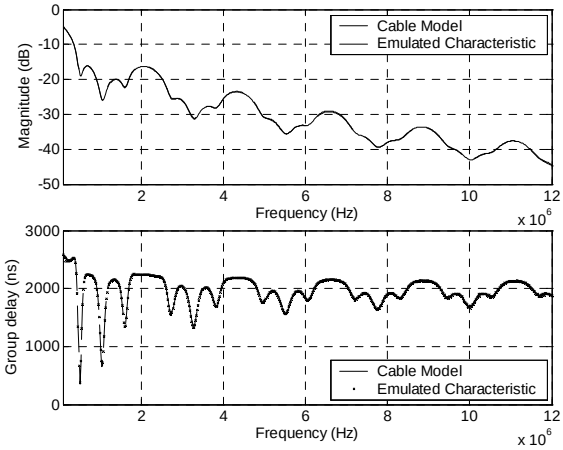

Figure 2 : ANSI VDSL 4 Insertion Loss: Emulation vs model

1.2. Access loop emulator shortcomings

Passive analog line emulators are a valuable asset to xDSL designers as they allow the emulation of transmission line topologies in a lab environment. However, these instruments have limited flexibility, typically only supporting a standardized set of loops ([1],[2],[3]). Analog line emulators are bulky in design and usually require more than one instance of the instrument to emulate a full loop topology. Furthermore, emulators based on lumped elements can exhibit precursor energy, resulting in an incorrect impulse response of the loop.
Passive analog emulators aim to accurately reproduce the primary transmission line parameters (R, L, C and G) of a twisted pair, instead of the secondary parameters (attenuation, group delay, impedance and return loss). Although being products of the primary parameters, the secondary parameters are of importance to the performance of xDSL communication equipment, and a direct emulation of the secondary parameters would be beneficial for the achievable accuracy. Lastly, analog component tolerances, combined with variations caused by environmental conditions and aging, may pose a performance barrier for accurate and consistent channel emulation.

Active analog line emulators address some of the above limitations, notably lack of flexibility and the presence of precursor energy, but others remain unsolved. Active analog emulators are generally limited to the emulation of a single segment, such that to emulate a complex loop topology, several devices may be needed. Due to the use of active components, this type of emulator has a higher noise floor than its passive counterparts.

2. A RECONFIGURABLE HARDWARE PLATFORM FOR DIGITAL EMULATION

2.1. Introduction

An FPGA based digital signal processing module is presented that is capable of emulating the physical layer of communication systems. Depending on the technology for which the emulator is being deployed, different behavioral characteristics and specifications will apply. This myriad of different requirements makes the design of the module more challenging, and illustrates the flexibility of the digital emulator concept. The feasibility of such a system is demonstrated through the development of an access loop emulator for VDSL applications.

2.2. Real-Time digital emulation

A digital approach has a number of advantages over the classical analog designs techniques when considering physical layer emulation:

Reconfigurability— The capability of reconfiguring the platform is an important asset. It allows to change physical layer models to include additional aspects that were not covered in the original models or even add new models without making labor intensive hardware modifications. The applications of the processing core are not only confined to loop emulation. It's reconfigurable nature, combined with a high performance analog front end results in a versatile platform suitable for a wide range of instrumentation applications.
Reproducibility— A digital core produces consistent results over a prolonged time period and is not prone to aging and environmental influences as are analog designs. However, the necessary conversion to and from the analog domain reduces the deterministic character. In-system calibration procedures can compensate for the introduced inaccuracies, without any modification to the actual hardware platform, as the compensation is performed digitally.
Delay emulation— The correct emulation of group delay of the transmission medium is important. Advanced communication systems typically use one or more mechanisms to compensate for the frequency-dependent characteristics of the transmission medium, commonly called equalizers. From a digital perspective, group delay can be emulated efficiently using delay lines, supporting very long delays, whilst maintaining a fine granularity. Analog delay lines, although feasible, cannot achieve the same combination of flexibility and range.

Time-variant, fading channels— An important parameter for evaluating a technology is its stability against channel variations. This impairment is typically observed in wireless communications but also exists in the telephone access network. Temperature variations affect the primary loop characteristics, especially the resistance per unit length [5]. The need for evaluating the capability of the transmission technology to cope with these channel variations has been identified recently in [4]. Although a testing method based on heating or cooling real cable sections is proposed, digital emulation provides a far more accurate and reproducible means to realize the equivalent channel variations.

2.3. Design constraints

Digital emulation has several advantages over the current passive and active analog approaches, yet faces a set of technology-related hurdles, which are discussed below. The combined specifications on linearity, bandwidth, dynamic range, noise floor and accuracy are very high and require state-of-the-art components and novel design approaches, as the emulator needs to outperform the already high performance xDSL equipment in order to successfully validate it.

Hard delay constraints— The correct emulation of the phase response, and of its first derivative, the group delay, is a constraint not often found in the design of a digital (sub)system. Strict end-to-end delay budgets need to be met, resulting from the physical propagation along the emulated line segments. The available computational window, i.e. the time available to perform the necessary calculations, is equal to the delay of the emulated physical medium, minus the time needed for the A-to-D and D-to-A conversions and the delay of the analog low pass filters. This means that for the shortest section in the ETSI and ANSI standards, a 150 ft cable, only 257 ns processing time is available. It is clear that very high performance digital filter structures are needed, especially for the shorter cable lengths. The delay budget needs to be carefully distributed over the building blocks of the system.
Bandwidth— The bandwidth of the system is limited by the throughput rate of the FPGA based signal processing core, through the Nyquist condition. A sample rate of 32 MSPS is necessary to process the full VDSL bandwidth of 12 MHz without too stringent anti-aliasing filter specifications. The samples are then processed at 160 MHz, minimizing the computational latency. These high core speeds can only be reached using custom placement macros in the Xilinx place and route tools. Typical clock rate improvements, such as pipelining the critical paths, cannot be applied here as this increases throughput delay.
Noise floor and dynamic range— The use of active components puts a compromise on the noise floor performance and dynamic range of any device, compared to a completely analog approach. The noise level due to round-off inside the digital core is minimized by using a processing word width of 32 bit. The analog front-end, which takes care of the A/D and D/A conversion will present itself as a limiting factor. In that respect, special care was taken to optimize the design from a system perspective.

2.4. Hardware overview

The hardware consists of two identical interconnected modules each hosting a high performance 14-bit ADC, one 14-bit DAC and a USB 2.0 interface. One module interfaces to a hybrid connected to the subscriber DSL modem and the other module connects through a second hybrid with the central office equipment. As only four extended eurocard sized boards are needed, a complete emulator only takes a volume of only l8 dm^3.

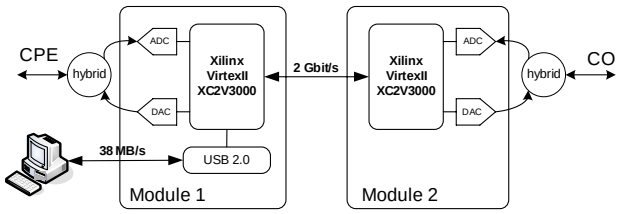

Figure 3 : Dual Module Emulation Setup

The hard real time signal processing is performed in a Xilinx Virtex-II XC2V3000-6 FPGA on each module with a full duplex communication link of 1 Gbit/s each way connecting both modules. In order to address even more complex line topologies, each board can be equipped with a second, identical Xilinx Virtex-II FPGA, doubling the number of available logic gates up to 12 million.

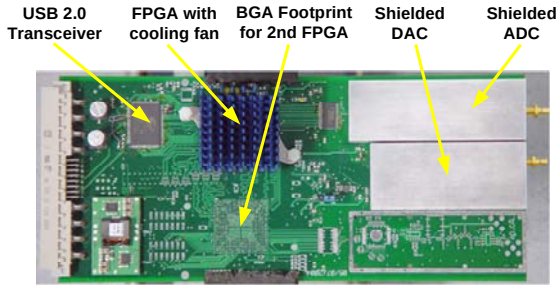

Figure 4 : Single Digital Module

Special care was taken in the design of the analog frond-end. First of all, custom shielding made of a solid metal slab was fabricated in order to achieve an isolation better than 104 dB between the A/D and D/A channel. Secondly, the noise floor of each channel was optimised. This results in a system with a noise floor below -140 dBm/Hz and a dynamic range of 80 dB.

The control platform of the system is an embedded PC running Linux with a custom USB 2.0 kernel module. The USB 2.0 connection is used to configure the FPGAs and to perform settings afterwards. The large interface bandwidth (38MB/s) also permits to stream PC-generated impairment signals to the FPGA and inject them into the signal path.

The FPGA based signal processing core combined with the high performance analog front-end and a fast PC-link makes this module a versatile hardware platform suitable for a broad range of instrumentation applications.

2.5. The digital filter core implementation on FPGA

In literature, a number of attempts to perform physical layer emulation digitally are documented. In most cases, simplifications are made to the original model to reduce complexity or to increase the feasibility of a real-time implementation. This leads to partially inaccurate representations of the physical medium of interest [6].

In order to accurately emulate arbitrary line topologies two types of FPGA building blocks were designed: A 'line' and a 'node'. The former emulates the frequency dependent insertion loss of the cable while the latter is responsible for generating reflections due to characteristic impedance mismatches between cable sections. Both building blocks are devised from several configurable, bi-directional 2^{nd} order IIR filters processing a 32-bit wide input in five clock cycles using only three 32x18 bit multipliers and four adders. In order to process 32 MSPS with minimal latency, an internal clock rate of 160 MHz is needed. If such a design is combined with careful delay distribution over the building blocks, lines as short as 150ft can be accurately emulated.

The FPGA design comprised of the aforementioned configurable building blocks defines the loop topology. The actual frequency dependent characteristics of the lines and nodes are defined by uploading a set of parameters to the modules. Furthermore, each building block is in-system reconfigurable, thus allowing the emulation of time varying parameters such as temperature influences. The generation of these coefficients is outside the scope of this paper. In order to maximize the flexibility of an FPGA design some building blocks can be bypassed and the line propagation time can be adjusted using a configurable delay line. This highly modular and flexible approach allows the accurate emulation of ETSI and ANSI VDSL test loops 0 to 4 as well as custom loop topologies. This is in sheer contrast with commercially available access loop emulators, only supporting ETSI and ANSI loops 0,1 and 2 with limited flexibility.

3. RESULTS

3.1. Introduction

In this section, the performance of the emulator core is evaluated against a simulation model of the test loops. The reference simulation model is generated using a Matlab-based simulation tool, The FTW xDSL simulation tool [8], which contains model data for all standardized DSL test loop sets. All test loops evaluated here are extracted from the standardized reference test loops mentioned in [2],[3] and are based on the models provided in [1], to provide a basis for objective reference. The measurements shown in the following paragraphs are obtained without the reflection modules in place, to evaluate the performance of the digital core.

The specifications adhered to are those listed in [3]: a maximum magnitude deviation of 3 % on a dB scale and a group delay error of less then 3 % on a linear scale. A schematic view of the topologies covered in the different test cases is shown in Figure 5.

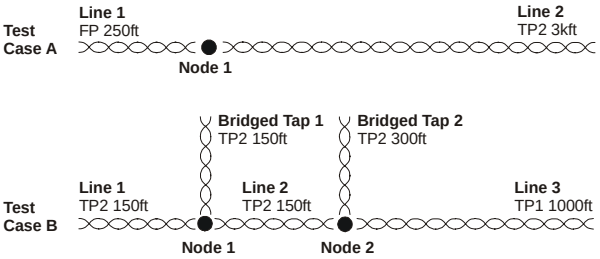

Figure 5: Test Loop Topologies Case A & B

3.2. Test Case A

The ANSI VDSL test loop 2 consists of a cascade of two transmission line sections, with a relatively long second section representing street cabling, and a first, shorter section, which may represent cabling at the subscriber's premises. Figure 6 indicates the accuracy with which the loop is emulated. The rather long TP2 section already introduces considerable attenuation at higher frequencies, yet the measured frequency response remains closely matched to the expected model, to within 0.5 dB. The emulated loop topology exceeds ETSI requirements: the group delay always remains within the 3% allowed margin of error, with an average deviation of less than 20 ns.

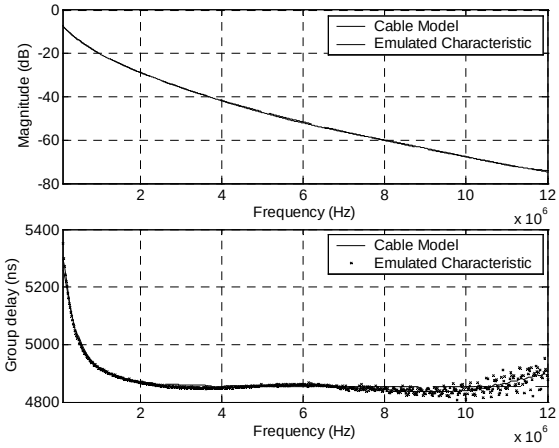

Figure 6 : Results Test Case A

3.3. Test Case B

An example of a complex loop topology is the ANSI VDSL4 test loop. Its topology and resulting characteristic was already shown in Figure 1 and Figure 2. This topology is an excellent example of delay limited design and the careful distribution of the delay over the building blocks. The first node, where signal reflections occur, is encountered after only 150 ft, this corresponds to a round-trip delay of 457 ns. This figure includes the propagation delay across the propagation modules and the signal conversion circuits, which amounts to approximately 200 ns, leaving only 257 ns to digitally process the incoming signals. The capability to digitally emulate short line sections is clearly demonstrated. Figure 2 shows the close correspondence between the model of the emulated topology and the measurements. The location of the notches, and their depth, is clearly defined indicating correct emulation of both group delay and amplitude response of the two bridged taps. The group delay remains within the allowed margin of error, except for the lowest frequency notches, where the margin is exceptionally tight. However, the severity of this deviation is debatable, considering the fact that xDSL equipment will generally avoid transmission in these notches. With exception of these notches, group delay emulation is accurate to within a 50 ns margin. The digital emulation core on the first module consumes 70% of the available FPGA slices and uses 80 out of 96 embedded multipliers, resulting in a processing power of 8.3 GMAC/s. The 'Line 3' section from the topology is implemented on module 2.

4. CONCLUSION

In this paper, a reconfigurable platform for the emulation of access networks is presented. The multi-million gate FPGA design is capable of emulating both amplitude and absolute phase of a complex line topology, even for very short line sections, and reproducibly achieves a substantially better accuracy than current, commercially available emulators. The building block concept and the easy reconfiguration open a whole new range of applications.

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