Java-enabled Low Cost RF Vector Network Analyzer

Bert De Mulder, Koen Van Renterghem, Els De Backer, Pieter Suanet, Jan Vandewege
Ghent University, IMEC/Intec
Sint Pietersnieuwstraat 41, B-9000 Ghent, Belgium
E-mail: bert.demulder@intec.ugent.be

***Abstract*-This paper describes a compact, low cost, low power vector network analyzer. The instrument's measurement range spans from 300 kHz up to 1500 MHz. The design was conceived to make the instrument generic and suited for many application areas. The instrument runs a local web server, hosting a java applet that contains application specific data processing software. We present the system architecture, discuss sub-block performance and propose some possible applications.**

I. INTRODUCTION

Nowadays, a complete range of RF spectrum analyzers and time domain analyzers exist that differ in terms of frequency range, dynamic range, sensitivity and processing capabilities. Because different applications require different instrument specifications, both low-end and high-end solutions have market potential.

The concept of a vector network analyzer (VNA) has since long been proven. Continued research on network analysis mainly focused on the design of professional instrumentation with ever-superior performance [1]. Numerous features make these instruments ideal for lab environments, but in cost sensitive applications such as continuous monitoring or in manufacturing and control processes, other approaches and priorities may yield better results.

We present a low cost high performance network analyzer, designed to be a flexible, cost-effective measuring platform suitable for a wide range of applications. After a summary of VNA basics, the system architecture and performance of the instrument are discussed in detail.

A next paragraph illustrates how processing of the measurement data, or *S* parameters, can generate more relevant information, reduce the information stream to be sent over the data network, and even hide the real VNA function behind an application specific interface. Finally, some application areas for continuous monitoring of electrical parameters are shortly described in this paper.

This work is a follow-up project of an earlier developed VNA [2] with frequency range from 50 kHz to 200 MHz.

II. SYSTEM ARCHITECTURE

Fig. 1 gives an overview of the VNA hardware, which consists of four major building blocks, arranged in a classical build-up to measure the *S* parameters of a two port. The transmitter block synthesizes a high purity sine wave with varying frequency. It forms an incident wave at port P_1 of the linear device under test (DUT), called the stimulus signal a_1.

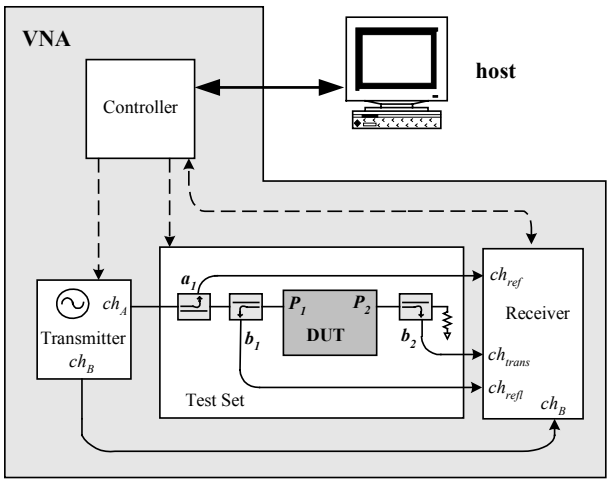

Fig. 1. System overview of the VNA. The device under test (DUT) is excited by a sine wave; both reflected and transmitted waves are measured in magnitude and phase.

Part of this incident wave is reflected at port P_1 causing b_1, while the remaining wave power enters the DUT which causes a wave b_2 to leave port P_2. The receiver consists of a reference channel that samples a_1, a transmission channel measuring b_2 and a reflection channel sampling b_1. Each single measurement is taken coherently, defining the relative magnitude and phase of b_1 and b_2 with respect to the reference a_1. This information is subsequently transformed into the *S* parameters S_{11} and S_{21}.

The test set splits off a small fraction of the incident and reflected waves at port P_1 and P_2 by means of wideband directional couplers, and feeds this fraction to the receiver. It can also simultaneously switch the excitation source to port P_2 and the transmission port to port P_1 without disconnecting the DUT, so that also S_{22} and S_{12} can be measured.

A low-cost embedded microcontroller performs less time-critical signal processing, and acts as the VNA system controller. It performs the transmitter and receiver setup and stimulates the frequency stepping, processes the measurement data and provides a LAN interface to a remote PC or workstation.

Of course the setup is non-deterministic and the instrument specifications may vary with temperature and time. Therefore a calibration cycle removes systematic errors from the measurement data, and every measurement point needs to be processed to retrieve the calibrated data. This process requires a lot of processing power, and hence runs on the logging host.

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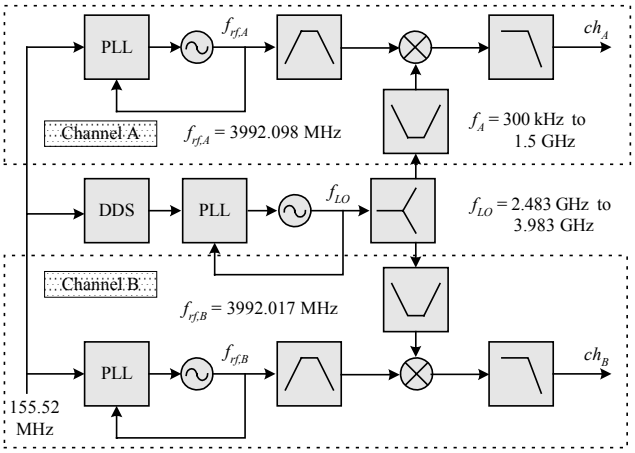

Fig. 2. Simplified transmitter architecture. It consists of two channels; one chain contains output-leveling circuitry. The synthesized frequency ranges from 300 kHz to 1.5 GHz.

A. Transmitter

The transmitter contains two channels. Channel A synthesizes a signal with frequency f_A, which can vary between 300 kHz and 1.5 GHz. Channel B synthesizes a signal with frequency f_B, having a fixed offset f_{if} from f_A.

The transmitter architecture is shown in detail in Fig. 2. Both channels contain a fixed-frequency PLL, synthesizing the RF frequencies $f_{rf,A}$ and $f_{rf,B}$ with a relative offset that equals f_{if}. After harmonic filtering, both signals are mixed with the same swept frequency local oscillator signal using passive double-balanced diode mixers.

The local oscillator (LO) signal synthesizer has a hybrid PLL/DDS architecture. This DDS driven PLL combines the advantages of a high frequency resolution with short frequency locking times [3], as required for fast and accurate sweeping. The output frequency can be switched in maximally 80 µs, a necessity for obtaining high measurement refresh rates. Other architectures could yield better phase noise performance, but at the expense of much higher transmitter complexity, power dissipation and cost. Furthermore, phase noise is a statistical process, and it's influence on measurement accuracy can be reduced by averaging consecutive measurements or reducing the receiver IF bandwidth.

Channel A contains a variable attenuator and amplifier to counteract the high-frequency roll-off of the channel, and to maximize the system dynamic range. Table I summarizes the transmitter specifications.

TABLE I
TRANSMITTER SPECIFICATIONS

	spec
Frequency range	300 kHz-1.5 GHz
Frequency Resolution	< 5 Hz
In band harmonic spurs	< -30 dBc
In band non-harmonics spurs	< -30 dBc
Phase noise @ 10 kHz	< -78 dBc
Phase noise @ 100 kHz	< -100 dBc
Channel A output power	> 12 dBm
Major close-in spur (@ f_{if} offset)	< -36 dBc

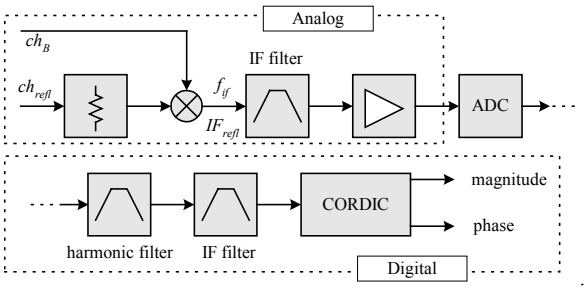

Fig. 3. Architecture of one narrowband IF mixed signal processing chain. Note that the complete receiver contains four channels.

B. Receiver

Fig. 3 shows the architecture of one single receiver input channel. Three similar receiver channels are used to process the reflection, transmission and reference signal (Fig. 1).

The transmitter B channel output provides the receiver LO input, having a fixed f_{if} frequency offset from the A channel stimulus signal. Each RF input signal is downconverted to f_{if} with a wide range RF mixer. No single passive diode mixer was found that has adequate bandwidth and performance to downconvert the full frequency span, so the receiver should be equipped with two different mixers.

After filtering and amplifying all IF signals, these are digitized by two dual channel 16-bit A/D converters at a fixed $6 \cdot f_{if}$ conversion rate. The conversion starts when all the PLL's are locked and the receiver input signals have stabilized.

Next, digital signal processing is performed by an FPGA. The digital signal is filtered with a fixed 12-tap FIR filter that suppresses all harmonics that are not at distance $N \cdot 6 \cdot f_{if}$ with N a natural number higher than zero. This filter optionally can be cascaded with a narrowband IIR filter to suppress non-harmonic spurs and phase noise, at the expense of slower measurements. The filtered IF signal is further processed by a CORDIC [4] core. CORDIC is a successive approximation algorithm that calculates magnitude and phase of the IF signal. It can be implemented very efficiently in programmable logic, justifying the selection of CORDIC above competitors. After algorithm completion, an interrupt notifies the controller that new measurement data is available for readout.

When the instrument is performing a frequency sweep, the procedure for every frequency point consists of setting the transmitter output frequency, waiting until the DUT is in steady state regime and defining magnitude and phase of all receiver input channels.

The key receiver specs are summarized in Table II. The limited inter channel isolation is caused by the ch_a distribution network. The standalone IF receiver has a SNR of 83 dB and it's interchannel isolation is better than 79 dB.

TABLE II
RECEIVER SPECIFICATIONS

	min	max
Frequency range (mixer 1)	5 MHz	1.5 GHz
Frequency range (mixer 2)	50 kHz	200 MHz
Input power		0 dBm
Inter channel isolation (full range)	48dB	

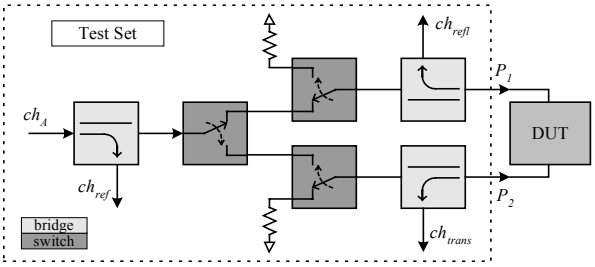

Fig. 4. Test set architecture. Two discrete load resistors provide in good return loss at the transmission port. By changing the state of all switches, port 2 becomes the excitation port.

C. S parameter Test Set

The test set architecture is shown in Fig 4. It contains three broadband directional bridges to sample both incident and reflected waves, next to three low cost solid-state switches. Using a bridge instead of a coupler increases the forward insertion loss, but this drawback is compensated by a more than two octave wide operating bandwidth.

The test set has frequency dependant loss and phase shift, so a 12-term short/open/load/through (SOLT) calibration [5] is performed to compensate for all systematic errors. Calibration improves the effective directivity, and compensates partially for finite channel isolation within the test set.

Some key specifications of the uncalibrated test set are summed in Table III. Note that in frequency range 1, directivity is still good, but increased losses in the directional bridge result in a reduced instrument dynamic range. Generating a higher transmitter power can counteract this.

D. Controller

The instrument controller consists of a microprocessor module that interfaces to an Ethernet controller providing a LAN connection to the user.

The microprocessor control task involves initializing the PLL and DDS components of the transmitter to the appropriate states. During a continuous frequency sweep this must be done on a regular basis. When the frequency sweep is completed, the microprocessor transfers frequency-stamped data from the FPGA platform and forwards these to the connecting workstation.

E. User Interface

The controller runs a small embedded web server. Any workstation that is web-wired to the instrument and authorized to do so can load the local web page.

TABLE III
TEST SET SPECIFICATIONS

	Range 1	Range 2
Frequency range	300 kHz-5 MHz	5 MHz-1.5 GHz
ch_A-P_1 insertion loss	< 26 dB	< 16.5 dB
ch_A-ch_{ref} insertion loss	< 30 dB	< 10.5 dB
P_1-ch_{refl} / P_2-ch_{tran} insertion loss	< 30 dB	< 10.5 dB
Isolation ch_A-ch_{tran} max	78 dB	61 dB
Isolation ch_A-ch_{tran} min	61 dB	56 dB
ch_A-ch_{ret}-P_1 Directivity	> 20 dB	> 24 dB

The web page contains a platform independent java applet. When loaded, both a control (tcp) and data (udp) connection are instantiated between host and controller. The tcp connection arranges the instrument setup. The data connection transfers uncalibrated measurement data to the host, which removes systematic errors from the measurement and converts the data to an appropriate format. A general purpose user interface is currently under development.

F. Prototype

The VNA prototype was built on three europrint size boards (160 mm x 100 mm), making the instrument very compact with respect to current professional analyzers. Fig. 6 gives an overview of the prototype. The left board is a two-layer FR4 PCB that has 4 IF input channels, and contains 4 A/D converters and the FPGA. A plug-on module contains the microprocessor and provides a LAN interface. The middle board contains the test set and three RF to IF downconversion channels for ch_{trans}, ch_{refl}, and ch_{ref}. This two-layer board was milled out of a high frequency laminate. The right board is the transmitter board, and has a hybrid layer stack. A high frequency laminate layer is used to implement microstrip transmission lines and filters. The other layers consist of low-cost epoxy material. In the test setup all boards are interconnected with coax and flatcable.

One should note the compactness compared to professional analysers. The system power consumption is a humble 11.5 W.

III. MEASUREMENTS

To check the accuracy of this low cost VNA, measurements made with our equipment were compared to HP8753D network analyzer measurements. SOLT standards from a HP85033D calibration kit were used to calibrate both instruments. The receiver was equipped with mixer type 1, and measurement range started from 10 MHz up to 1.5 GHz. All measurements were made without digital IF filter or averaging, as this design is still under development.

After performing a 12-term SOLT calibration cycle on our VNA, we reconnected the load at both ports and then measured the *S* parameter responses, as shown in Fig. 7. Reflection measurements have more than 50dB overall dynamic range. Inter-channel isolation between port 1 and 2 is found better than 68 dB below 1 GHz and better than 55 dB above. Professional instruments have lower crosstalk, as this limitation stems from a tradeoff with instrument compactness,

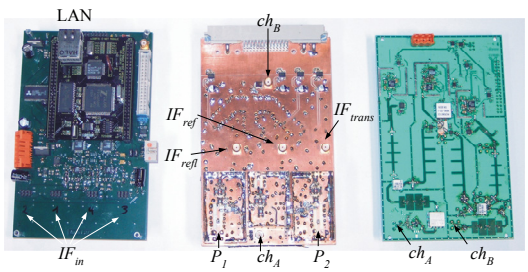

Fig. 6. VNA prototype. From left to right we distinguish the digital board, test set and downconversion board and transmitter board.

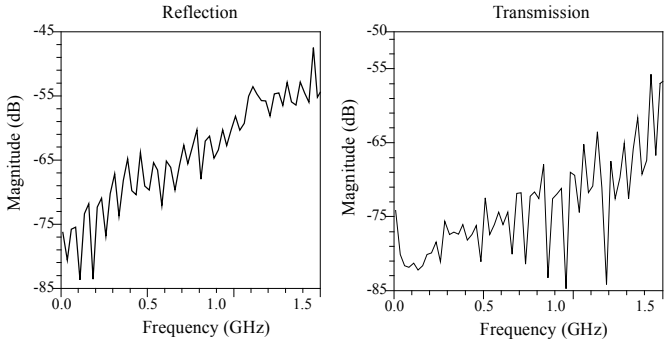

Fig. 7. VNA S_{11} and S_{21} measurement after calibration has been performed, with a load attached to both port P_1 and P_2.

weight and cost.

A 500 MHz low-pass filter was measured with both instruments. Fig. 8 and Fig. 9 compare the results to HP8753D measurements made on the same DUT. When measuring transmission responses, magnitude accuracy was better than ±1.2 dB and phase deviation lower than ±1 degree. Reflections could be measured with accuracy better than ±0.3 dB, and ±0.8 degree. These specifications are quite impressive, considering a total electronic component budget that is estimated at 600 USD, a fraction of the cost of professional analyzers.

These measurements prove the concept and illustrate the promising capabilities of low budget network analysis.

IV. APPLICATION DOMAINS

The most common application of the VNA is measuring *S* parameters of RF cabling, components, or (sub-) systems. Measured *S* parameters are easily entered into RF design software to model and optimize reflection, gain, group delay, VSWR, matching, tuning and even time-domain response.

Another application is frequency domain reflectometry. Using an inverse Fourier transform, a complex frequency-domain reflection measurement can be converted to time-domain information, which might reveal more relevant information. The highest measurable frequency of 1.5 GHz suggests a minimum resolution of 0.66 ns (or 0.2 m of cabling), but this can be improved by proper signal processing. A low cost VNA can be very effective for continuously monitoring electrical cable plants (RF and data networks,

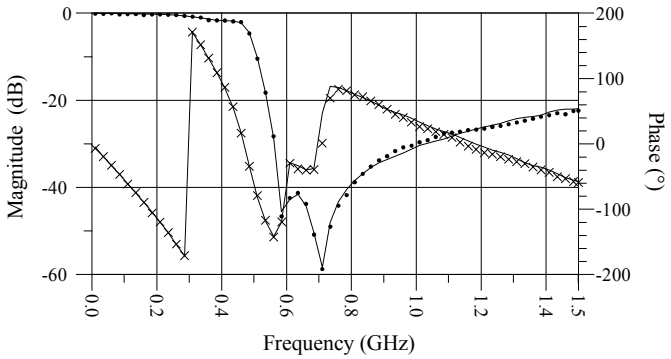

Fig. 8. Transmission (S_{21}) measurement made on a prototype low-pass filter. The dots and crosses indicate VNA measurement points for magnitude and phase respectively, the solid lines denote the HP8753D reference curves.

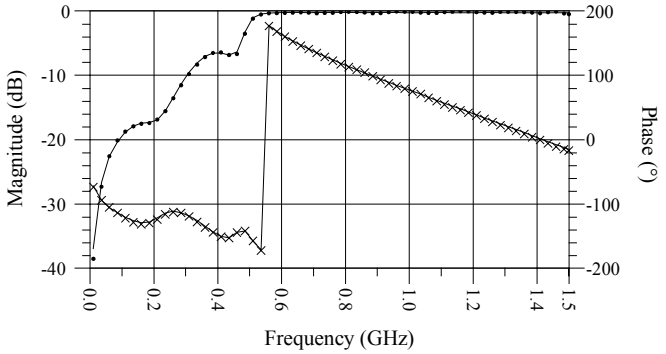

Fig 9. Reflection (S_{11}) measurement made on a prototype low-pass filter. The dots and crosses indicate VNA measurement points for magnitude and phase respectively, the solid lines denote the HP8753D reference curves.

power lines or even optical fiber cabling), enabling real-time network monitoring. By continuously scanning the reflection response of the network, fault prediction and fast error diagnosis is possible without interfering with the network operation.

The generic approach allows the development of a wide range of application specific software, hiding the unnecessary details and offering the user a familiar interface. So a "place and forget" scenario is possible, where the user does not even need to know what network analysis is all about.

V. CONCLUSION

This research has revealed a wide range of cost-sensitive applications that can hardly be covered with existing, lab-type VNA equipment. A web-based vector network analyzer was designed based on state-of-the-art RF hardware, and efficient digital signal processing. The VNA prototype covers a 300 kHz to 1.5 GHz frequency range. It is very compact, low weight, and consumes a humble 11.5 W, making it suitable for embedded applications. Measurement results were verified against professional lab equipment, and show good accuracy.

This system considerably lowers the threshold for tackling real life instrumentation and monitoring tasks with frequency domain VNA techniques.

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