# **Driving electronics for OLED lighting**

# Ann Monté\*, Jan Doutreloigne\*, Jindrich Windels\*, Pieter Bauwens\*

\*University of Ghent, Belgium

#### **ABSTRACT**

This paper proposes the concept of integrating an OLED (foil) and its driving electronics into one module. A complete light system consisting of these modules is the ultimate goal of this work. The main focus in this article is on the design of the driver chip and the circuit implementation. The measurement results confirm that it is possible to control the light output of the different modules.

#### 1. INTRODUCTION

Current OLED technology developments are mostly concentrating on material research, higher efficiency, low-cost production, etc. But for fully exploiting the potential of OLED (foils) in a lighting system, more developments are needed concerning driving electronics, power distribution, integration and miniaturization.

These last challenges are tackled within the IMOLA project. IMOLA stands for "Intelligent light Management for OLed on foil Applications". The main concept of the project is the realization of an interactive, modular, flexible, large area, OLED-based lighting system on low-cost foil with built-in intelligent light management. In this system the light intensity can be adjusted uniformly on the whole OLED panel or locally at module-level. Innovative developments in the IMOLA system are situated in the OLED driver concept, the optical feedback mechanism and the technology integration challenges, resulting in a lightweight and very flat tiled lighting system.

To drive the OLED, a chip was designed in the I3T80 technology of ON Semiconductor. It contains an OLED driver prototype consisting of High-Voltage switching transistors, being part of a DC-DC buck converter, and a feedback loop.

# 2. A TILED LIGHTING SYSTEM 2.1 The IMOLA concept

A 3D impression of the end product targeted in the IMOLA project is shown in Figure 1. The right image shows how the tiled OLED lighting system will be assembled. The OLED front panel is laminated and connected to the driver back panel, forming a complete segmented lighting foil. On the left a detailed view of a single OLED – Driver element is shown.

The front side of the system consists of OLED tiles, the backplane foil contains the driver electronics for the brightness control of the individual OLED tiles. In order to make a flexible lighting system, the OLED driver circuit is integrated on chip as much as possible. One can imagine that building the driver circuit with discrete components limits the flexibility of the system.

Yet, a relatively large inductor (up to  $10\mu H$ ) is needed. As it is impossible to integrate an inductor of such a value that still has a reasonable series resistance on chip, the use of an external inductor is mandatory. In order to maintain the flexibility of the system, this component is embedded into the backplane foil as a spiral inductor.

More information on the IMOLA concept, the driver electronics and the design of the inductor can be found in [1], [2] and [3].

# 2.2 OLED driver design

The driver electronics consists of a DC-DC buck converter and a feedback loop [1]. The High-Voltage switching transistors and the feedback loop are integrated on chip. In the final product, the goal is to have an optical feedback loop based on the light measurement done with a photodiode. However, this

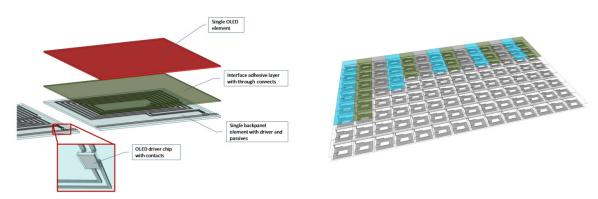


Fig. 1 3D impression of the IMOLA project

intelligence is not integrated yet in the first chip which is discussed in this article.

The block diagram of the chip is shown in Figure 2. On the right, there is the High-Voltage part converting the 40V supply voltage into a controllable DC current for each OLED based on the Low-Voltage Pulse Width Modulated (PWM) input signal. The converter consists of a pDMOS preceded by a buffer and a lever shifter as well as an nDMOS transistor acting as a freewheeling diode. A 36.7V linear regulator needed for the buffer is also integrated. A schematic of the complete buck converter is shown in Figure 3.

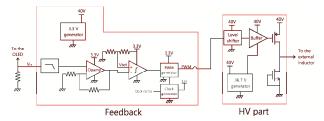


Fig. 2 Block diagram

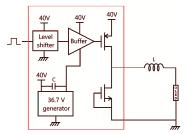


Fig. 3 Buck converter

The PWM input signal is generated by the feedback loop and is based on both the actual current through the OLED and the desired current. The actual OLED current is known by measuring the voltage over a low value sense resistor in series with the OLED. Since the OLED current varies periodically with the switching frequency, a  $2^{nd}$  order low-pass filter is added to get an average of the OLED current. After being amplified, the filtered voltage is compared with an externally applied signal ( $V_{set}$ ) by means of a differential integrator.

The output of the integrator is a measure for the accumulated difference between the actual OLED current and the desired OLED current. This voltage is then used by the PWM generator to decide the duty cycle of the PWM signal. This PWM generator circuit is based on digital logic with a controllable delay line.

The frequency of the PWM generator is determined by the output signal of the clock generator. Depending on the exact value of the externally applied voltage clock\_control, the frequency can be set between 1 MHz and 10 MHz.

#### 3. MEASUREMENT RESULTS

A first test of the chip was done on breadboard. It was immediately clear that all the capacitance added on chip was not enough to buffer the peak current sunk at the switching moments. Moreover, a switching circuit needs a well-considered layout. Therefore, a double-sided PCB was designed with the appropriate decoupling capacitance and an efficient layout of the tracks. The chip was wire-bonded onto the PCB instead of packaged in a DIL package.

At first, the chip is evaluated without any load connected to check the basic functionality. Afterwards, an inductive load in series with a load resistor is added.

#### 3.1 Evaluation of the chip - no load connected

Both the feedback loop and the HV part are tested. To check the HV part, a PWM input signal is applied with a function generator and the voltage at the drain of the switching transistor is measured. When the input PWM voltage is high, the output voltage is 40V to fall slowly when the input PWM voltage is 0V. So we can conclude that the functional behavior of the chip is correct when no load is connected.

To test the feedback loop, the PWM input signal of the HV part is connected to ground. First, the internally generated clock signal is verified. When no voltage is applied to the clock\_control pin, the frequency is set at 5MHz. One can see in Figure 4 that the period of the internally generated clock signal is indeed about 200ns. However, some additional capacitance on the clock\_control pin is required to achieve a 50% duty cycle for the clock.

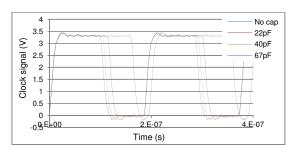


Fig. 4 Internal clock signal

A sine wave of 10Hz with 40mV amplitude and a varying DC voltage is applied to the feedback pin to test the combination of the filter, amplifier and integrator. Figure 5 shows the applied sine wave at the feedback pin and the output signal of the integrator for different values of  $V_{\rm set}$ . One can see that for lower values of  $V_{\rm set}$ , the integrator output switches from high to low at lower FB voltages as expected. However, for values of  $V_{\rm set}$  higher than 2V, the integrator output doesn't differ a lot as a function of  $V_{\rm set}$ . This is due to the design of the integrator, more specific, the input of the integrator is a p-type differential pair with a dc shifter. This choice was made to allow for values of  $V_{\rm set}$  below the threshold

voltage of the alternative (n-type) input stage. According to the IMOLA project specifications,  $V_{\text{set}}$  should be able to vary over a factor 10.

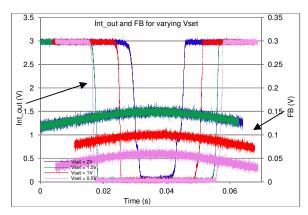


Fig. 5 Integrator output when a 40mV sine wave is applied at the feedback pin

The last block of the feedback loop, besides the 3.3V linear regulator, is the PWM generator. Figure 6 shows the generated PWM output signals for different values of the integrator output. The clock period is set at 200ns.

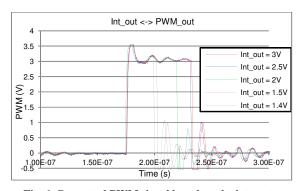


Fig. 6 Generated PWM signal based on the integrator output signal

One can see that the duty cycle of the PWM signal varies with the integrator output value. Once that value is above 2.5V, the pulse width of the PWM no longer significantly increases. This is a design choice based on the requirement of achieving a minimum pulse width of 25ns for a 3V Int\_out voltage over all process and temperature corners.

Up to now, we can conclude that if no load is connected, only minor adaptations are needed to make all the different building blocks of the chip work as expected.

#### 3.2 Evaluation of the chip - inductive load

For evaluating the complete chip, two different chips are used. One on the PCB on which only the feedback loop is enabled and one on breadboard of which only the HV part is used. The reason we do this is that all of the chips on PCB but one were destroyed in testing (and I would like to save the remaining one). The load connected

to the switching node is a  $400\mu H$  inductor in series with a  $400\Omega$  resistor and a  $3\Omega$  feedback resistor.

As a first test,  $V_{\text{set}}$  was varied and the switch pulse at the drain of the switching transistor was measured. The result is shown in Figure 7.

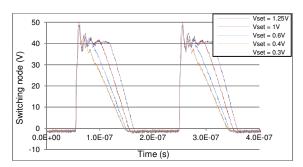


Figure 7 HV pulses generated at the switching node for different values of  $V_{\text{set}}$ 

One can see that it is possible to tune the duty cycle of the pulses at the switching node within a certain range. However, the system is very sensitive. Figure 8 shows the measured signal on the  $V_{\text{set}}$  pin when the HV chip was switched off and on respectively. It is clear that switching on the buck converter introduces a lot of noise, which makes it difficult to build a sensitive system.

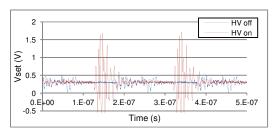


Fig. 8 Difference in the  $V_{\text{set}}$  voltage for the buck converter switched on and off

Even though both chips were at a distance of about 15cm, noise is still coupled between both chips. Moreover, it is difficult to know exactly what is measured. For example, when adding a second probe to measure the value of Vset at the same time the signal at the switching node is measured, the signal at the switching node changes.

# 4. DISCUSSION

Based on the previous results we can conclude that the functional behavior of the chip is as expected, but that due to both the steep OLED I-V characteristic and the slow falling edge of the switching pulse it will be very difficult to tune the current through an OLED with small steps.

#### 5. CONCLUSION

The IMOLA project offers a solution for integrating the OLED driving electronics and the OLED front panel in one flexible system. It is possible to tune the current

through an OLED by means of a switching DC-DC converter. The resolution of the system is not yet as we desire, but a first big step is made towards the integration of an OLED lighting system.

## **ACKNOWLEDGEMENT**

This work was funded under the Seventh Framework Programme for ICT of the European Union through the IMOLA project (GA 288377).

## **REFERENCES**

[1] J. Doutreloigne, A. Monté, J. Windels, "Design of an

- Integrated OLED Driver for a Modular Large-Area Lighting System", CSS2013, January 2013.
- [2] J. Kundrata, A. Baric, "Design of a Planar Inductor for DC-DC Converter on Flexible Foil Applications", Proc. of the 35<sup>th</sup> International Convention MIPRO2012, pp. 54-59, May 2012.
- [3] J. Kundrata, A. Baric, "Electrical and Thermal Analysis of an OLED Module", *Comsol Conference*, Milan, Oct 2012.