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Voltage dip immunity test set-up for induction motor drives

Kurt Stockman, Frederik D'hulster, Kevin Verhaege, Jan Desmet*, Ronnie Belmans**
* Hogeschool West-Vlaanderen, dept. P.I.H., Graaf Karel de Goedelaan 5, B-8500 Kortrijk, Belgium
** K.U.Leuven, dept. ESAT/ELEN, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

Abstract: *A growing number of industrial facilities is using adjustable speed induction motor drives in order to increase the quality of their products and the flexibility in the production process. The reliability of the production plant decreases with the number of installed drives due to their sensitivity towards voltage dips. This paper presents a test set-up to determine the immunity of standard induction motor drives against supply voltage dips under various load conditions. Furthermore, the measurements are compared to simulation results.*
Key Words: ***Adjustable speed drives, voltage dips, dip immunity, ride through***

1. INTRODUCTION

A voltage dip is a momentary reduction of the rms voltage at a customer position. Bollen [1] characterises a voltage dip by a magnitude and a duration (0.5 – 30 cycles). The voltage dips are caused by faults in the utility distribution system and transported to all facilities on the same distribution network.

Voltage dips are widely recognised as the main cause of disturbances in production plants, equipped with adjustable speed drives (ASD). McGranaghan et al. [2] show that the economic impact of the possible loss of production due to voltage dips can be very high. In order to prevent tripping of an ASD during a dip, the immunity of drives should be taken into account during the design stage of production plants. This paper gives the design engineers a helpful insight in the possible ride-through ability of standard drives for induction machines under typical load conditions.

2. ENERGY CONSIDERATIONS

Fig. 1 shows the topology of an AC adjustable speed drive. It consists of three major parts: a diode rectifier, a DC buffer link and a controlled inverter.

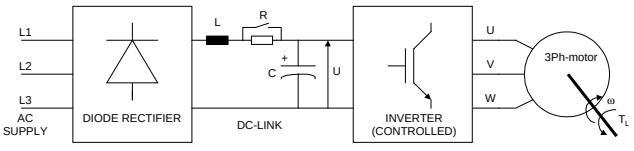

Fig. 1 *Typical AC adjustable speed drive topology*

The behaviour of the ASD, during a supply voltage dip, can be represented by an energy balance .

$$E_C + E_{kin} = E_L \tag{1a}$$

$$\frac{C}{2}\left(U_C^2(t_2) - U_C^2(t_1)\right) + \frac{J_L}{2}\left(\omega^2(t_2) - \omega^2(t_1)\right) = \int_{t_1}^{t_2} T_L.\omega.dt \tag{1b}$$

Note that, if the symmetrical voltage dip is below the DC-link voltage U_C, no energy is fed from the AC-supply into the DC-link because of the reverse biased diodes in the rectifier.

When analysing the energy balance, we can determine three main parameters influencing the behaviour of an ASD during a supply voltage dip of duration $(t_2 - t_1)$:

- The DC-link capacitor C: determines the electric energy E_C stored in the DC-link;
- The load inertia J_L: determines the mechanical energy E_{kin} stored in the rotating parts;
- The motor load profile $T_L(\omega)$: the energy consumer.

In low-inertia systems, the discharge-rate of the capacitor determines the survival-duration of the loaded drive. Typical values for the DC-link capacitor are between 75 and 360 µF/kW [1]. Fig.2 shows the decay of the DC-link voltage with such capacitor size under constant power demand P as expressed in

$$U(t) = \sqrt{U_0^2 - \frac{2P}{C}.t} \tag{2}$$

The energy-amount in a loaded capacitor is not enough to drive the load longer than 1.5 periods, with a DC-link undervoltage protection of 65% U_0 $(= U_{DC\ nom})$. If the DC-link voltage drops below the minimum voltage protection level $U_{DC\ min}$, the inverter is inhibited and the charging resistor R (Fig. 1) is activated, limiting the charging current at return of the supply voltage. If the voltage is restored, before reaching the DC-link

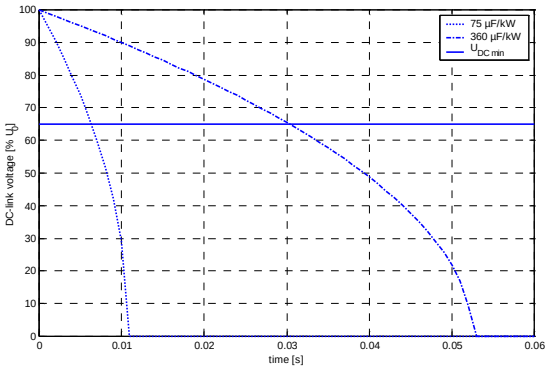

Fig. 2 *Influence of capacitor size on DC-link voltage*

undervoltage protection, the transient behaviour is mainly determined by the R-L-C combination in the supply and DC-link. Poor damping of this electrical second order system results in a DC-overvoltage and a peak supply current, at the re-entry of the supply voltage after a dip. This peak current can cause severe stress on the drive rectifier unit.

3. SIMULATION MODEL

Fig.3 represents a Matlab® / Simulink® discrete model of an ASD with PWM-pulse control. The dipgenerator feeds the rectifier with a three-phase controllable power source. A PWM-pulse generator controls the switching pattern of the IGBT's in the inverter. The slip-speed controller generates the required frequency and amplitude for the sine reference generator. The U/f-ratio is kept constant over the overal speed range. In order to simulate the behaviour of standard induction motor drives under various load conditions, one can select whether the load is function of time or speed. Different voltage dip ride-through techniques, e.g. kinetic buffering can be implemented in the model. Fig. 4 shows the RMS supply line voltage, the DC-link voltage, the rotor speed, the load torque, the motor

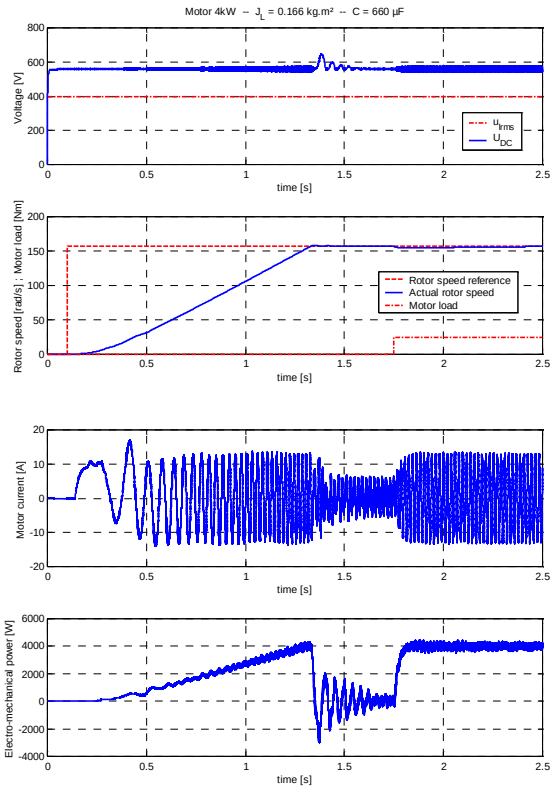

Fig. 4 *Simulation results of the behaviour of a PWM-pulse controlled 4kW induction motor*

current and the electromechanical power delivered by the motor. This model is used to analyse the behaviour of a standard induction motor drive under different voltage dips and load conditions.

4. TEST SET-UP

An experimental test set-up is build to measure the immunity of variable speed drives towards voltage dips under different load profiles. Fig. 5 shows the experimental set-up. It consists of four major parts: a

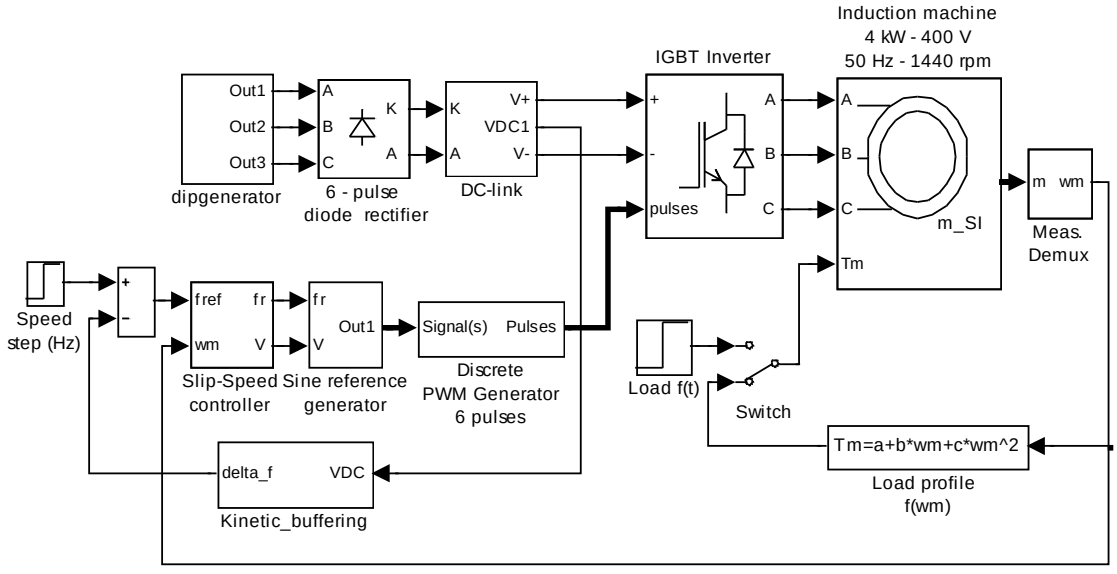

Fig.3 *Simulation model of an ASD with PWM-pulse control*

programmable power source, the adjustable speed drive, the load machine and the load controller. A programmable power source (3x5kVA) is used to generate both balanced and unbalanced voltage dips according to the IEC 61000-4-11 standard [3]. The EUT, consisting of an adjustable speed drive with induction motor (up to 11kW) is loaded by a torque controlled DC-machine. Using a dSpace® DS1103 PPC controller-board, a Matlab® / Simulink® program is run to control the test set-up in real-time. Speed and load torque are measured to generate the necessary corrections, according to the selected loading profile. With the real-time user-interface ControlDesk®, different load profiles can be programmed in the controller. All signals are isolated in order to protect the controller-card against EMC, ground loops and overvoltages.

5. MEASUREMENT RESULTS

Several standard induction motor drives have been subjected to balanced and unbalanced voltage dips. The measurement results are compared to the simulation results in order to prove the validity of the model. Fig. 6 shows a voltage dip measurement of the transient behaviour of a 4kW ASD under full load condition.

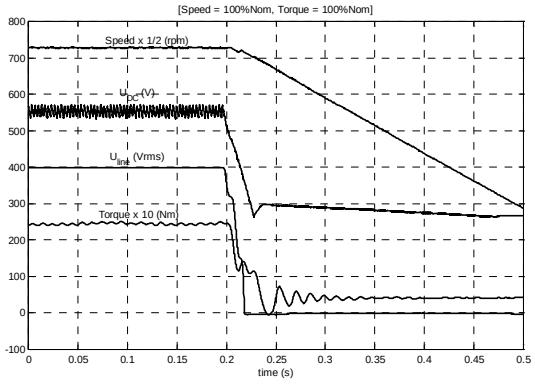

Fig. 6 *Voltage tolerance measurement (4kW ;T_{rated}; n_{rated})*

The transition in slew rate of the DC-link voltage marks the drive tripping point.

To represent the behaviour of drives under dip conditions, voltage tolerance curves are used. A voltage tolerance curve divides the dip magnitude - duration plane in a ride-through (pass) and a trip (fail) area. The only standard that currently describes how to measure the voltage tolerance of three-phase equipment is IEC 61000-4-11. However, this standard does not mention anything about voltage tolerance curves. Only some discrete dips (depth and duration) should be measured to define the voltage tolerance. Using these predefined measurements, the voltage tolerance curve cannot be constructed as not all measurements are pass-fail transition points. On the test set-up, the depth and duration of voltage dips were continuously changed in order to define the limits of ride-through (voltage tolerance).

Fig. 7 compares the simulated and measured voltage tolerance curve for a 4kW ASD at full load (T = 25Nm). If the remaining voltage during the dip is below the undervoltage limit of the ASD, the drive will always trip. The rectifier stops conducting and all energy has to be taken from the capacitors. As seen from Fig. 7, the drive trips after 17 ms.

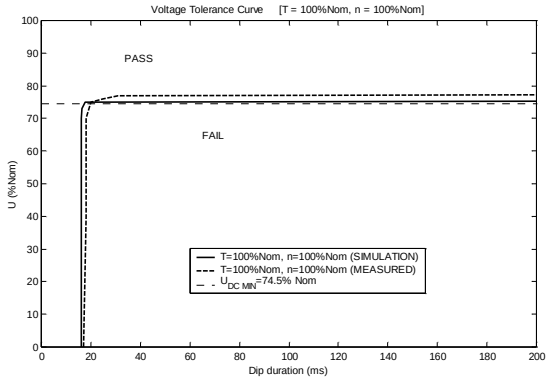

Fig. 7 *Voltage tolerance curve (4kW ;T_{rated}; n_{rated})*

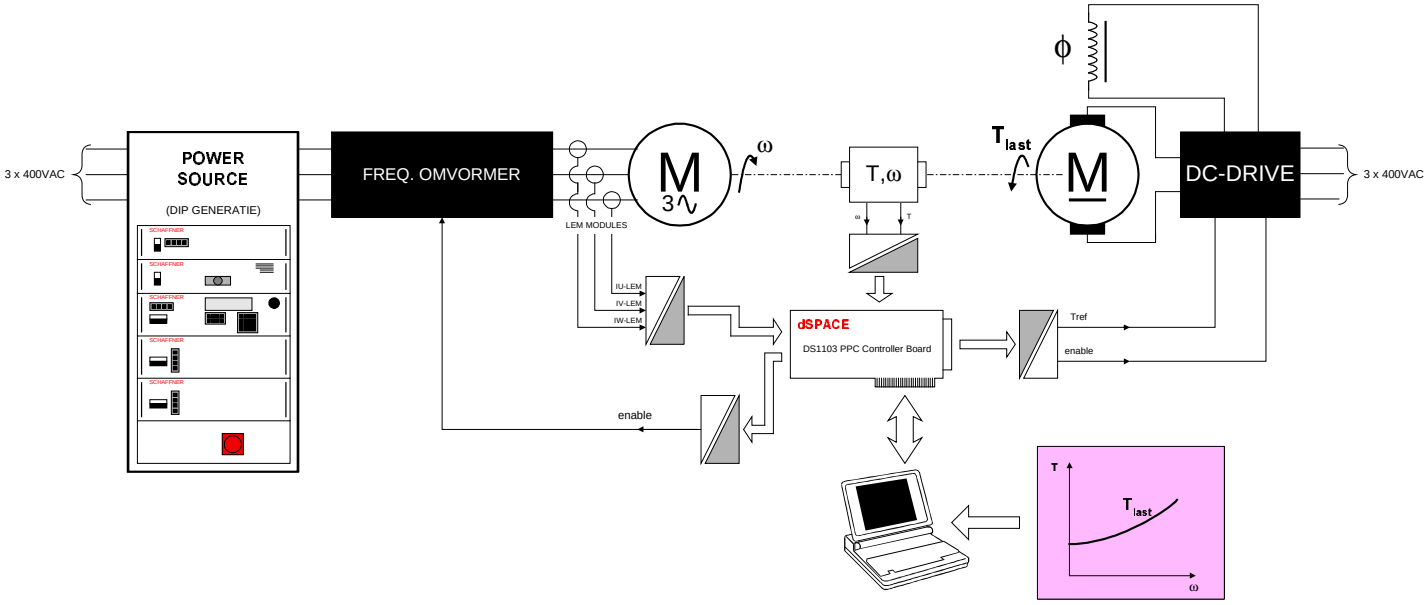

Fig. 5 *Experimental set-up*

By reducing the depth of the dip, one can find a supply line voltage for which the drive does no longer trip. Depending on the torque and speed conditions of the machine, this value differs from the undervoltage treshold level due to the ripple on the DC-bus voltage. Fig. 8 represents the influence of the motor load on the voltage tolerance curve.

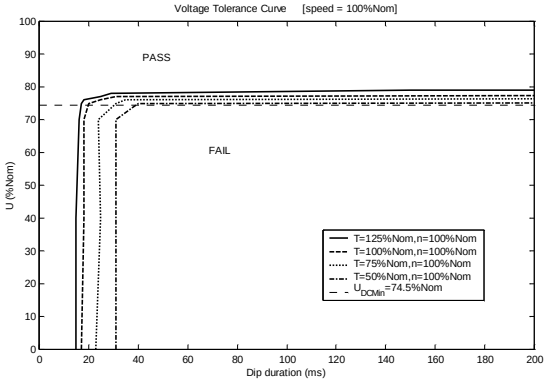

Fig. 8 *Influence of motor load on voltage tolerance curve (measurement)*

Considering a constant torque and reducing the speed of the machine results in a decreasing power demand. The ripple on the DC-bus voltage thus becomes smaller. Fig. 9 shows that the operation at reduced speed improves the immunity against voltage dips.

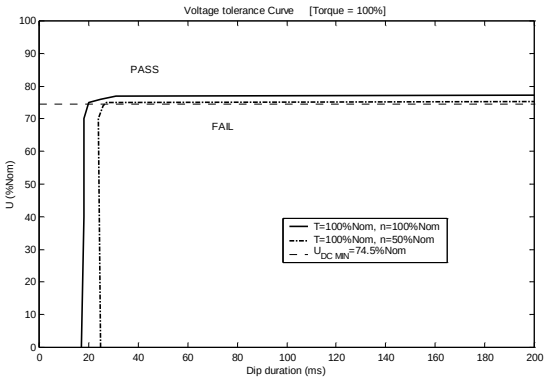

Fig. 9 *Influence of motor speed on voltage tolerance curve (measurement)*

The point on wave at which the voltage dip occurs, also has an influence on the possible ride-through time. Fig. 10 shows the influence of the dip start-time for a three-phase balanced dip. For the same dip-duration, the dash-dotted voltage curve trips and the solid curve survives, due to a higher energy level in the DC-link at dip-initiation.

Up to now, only balanced dips have been discussed. In practice, however, unbalanced dips occur more frequently. Single-phase-to-ground (SPTG) faults do not strongly affect the behaviour of an ASD (Fig. 11). The three-phase rectifier acts as a single-phase rectifier. In this case the DC-link can recharge every 10 ms from the two remaining supply lines. Fig. 5 shows a simulation of the DC-link with a SLTG fault (40ms) in the power

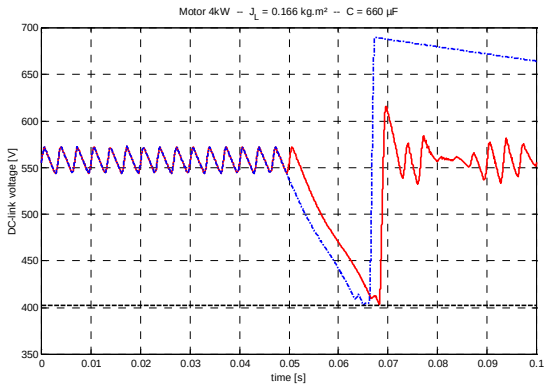

Fig. 10 *Influence of the voltage dip-initiation time (simulation)*

supply. At full motor load (4 kW), the DC-link voltage never reaches the undervoltage protection level ($U_{DC\ min}$ = 74.5%).

For a two-phase-to-ground (TPTG) fault, the remaining line voltage at the rectifier equals the system phase voltage. The maximum available DC-link voltage is:

$$U = \frac{U_0}{\sqrt{3}} \qquad (3)$$

If the undervoltage limit cannot be reduced under this voltage level, the behaviour can be compared to a balanced voltage dip. Fig. 11 shows a simulation of a SPTG fault versus a TPTG fault.

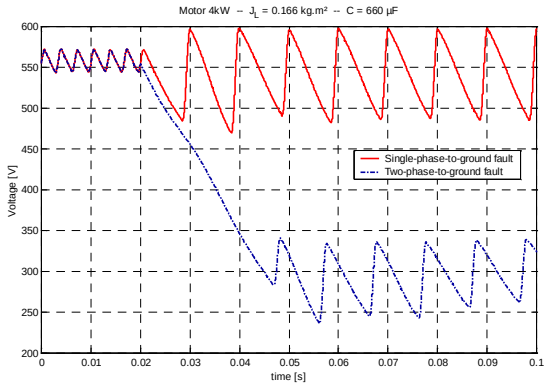

Fig. 11 *SPTG versus TPTG fault (full load) (simulation)*

6. CONCLUSIONS

This paper introduces a test setup to obtain voltage tolerance curves for ASD under different load conditions. Furthermore the measurement results are verified with the simulation model. Standard ASD are very sensitive to voltage dips. The main restriction is the DC-link undervoltage protection level, defined by the manufacturer. It can be seen from Fig. 2 that increasing the capacitor value is not a very effective way to improve the ride-through time.

Further research and measurements will concentrate on the improvement of the immunity of the ASD. New tolerance curves for ASD with kinetic buffering, boost modules and other ride-through equipment will help the design engineer to choose the correct mitigation equipment to reach the desired level of ride-through.

7. ACKNOWLEDGEMENT

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