An Equivalent Circuit Model of the Traveling Wave Electrode for Carrier-depletion-based Silicon Optical Modulators

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***Abstract*—We propose an equivalent circuit model for the coplanar waveguide (CPW) which serves as the traveling wave electrode to drive carrier-depletion-based silicon modulators. Conformal mapping and partial capacitance techniques are employed to calculate each element of the circuit. The validity of the model is confirmed by the comparison with both finite-element simulation and experimental result. With the model we calculate the modulation bandwidth for different CPW dimensions and termination impedances. A 3 dB modulation bandwidth of 15 GHz is demonstrated with a traveling wave electrode of 3 mm. The calculation indicates that by utilizing a traveling wave electrode of 2 mm we can obtain a 3 dB modulation bandwidth of 28 GHz.**

***Index Terms*—Equivalent circuits, microwave propagation, optical modulation, p-n junctions, transmission lines.**

I. Introduction

Silicon optical modulators have clearly gone through a period of rapid progress during the past several years [1], as waveguide-based silicon modulators are successfully demonstrated with different modulation mechanisms, such as: the Franz-Keldysh effect of SiGe [2], [3], the plasma dispersion effect of silicon itself [1], the electro-optical (EO) effect of strained silicon [4] and polymer-clad silicon slots [5], [6], the carrier depletion effect of the multiple quantum wells wafer-bonded on silicon [7], etc.. The most common method among these silicon modulation solutions is to exploit the plasma dispersion effect of silicon, since it doesn't need integrations of any other materials like germanium or polymer, and thus is intrinsically compatible with CMOS technology. To implement optical modulation by the plasma dispersion effect, the charge density inside an optical waveguide has to be manipulated by an electrical signal. This can be achieved by three techniques: carrier injection, accumulation and depletion [1]. Since the carrier-depletion-based modulator offers merits of processing simplicity and high operation speed, a lot of efforts are devoted to improve its performance [8]-[11]. A carrier-depletion-based modulator is implemented by incorporating a PN junction inside the core of an optical waveguide. The optical modulation is achieved by reverse-biasing the junction and extracting the carriers. Its intrinsic response speed is limited by the time required for carriers to be swept out from and to return to the PN junction. This process only takes a few picoseconds since carriers drift at their saturation velocity under a large electrical field, so the potential bandwidth of such a device can reach 50 GHz [12]. However, the final operation speed is limited by particular driving schemes. Basically an optical modulator can be driven by a lumped electrode or a traveling wave electrode provided that a Mach-Zehnder (MZ) interferometer structure is employed. The lumped electrode is straightforward but it cannot fully exploit the advantage of high operation speed of the carrier-depletion-based modulator due to the RC time constant, so a traveling wave electrode is strongly desired [8], [9], [13], [14].

The operation speed of a modulator driven by a traveling wave electrode is determined by 3 factors: the velocity matching between the microwave and the optical carrier, the impedance matching and the microwave attenuation. A specific transmission line calculation is essential to achieve high speed modulation. This can be carried out by numerical field simulations employing the method of lines (MoL) [15], [16] or the finite-element method (FEM) [17]-[20]. Another technique to analyze the transmission line is to develop its equivalent circuit model under the quasi-TEM approximation [21]-[24]. Such an equivalent model is always preferable not only because it requires much less computing resource than the numerical simulation, but more importantly, because it gives a clear physical insight into the transmission line. The equivalent circuit model is used quite common for $LiNbO_3$ modulators [21], [22]. However, to develop this model for carrier-depletion-based optical modulators turns out to be tricky, since a carrier-depletion-based modulator is not a regular laminated structure consisting of homogeneous dielectric layers with the electrode on top. A typical CMOS compatible carrier-depletion-based modulator has vias through the pre-metal dielectric layer (PMD); meanwhile the conductivity of its waveguide layer is not uniform due to different local doping levels in order to form the PN junction and the contact. These features make it a challenge to deduce an equivalent circuit model for carrier-depletion-based modulators, so in [14]

Manuscript received Aug 3, 2011.

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an approximate method is used for the RF design. The distributed parameters of an unloaded coplanar waveguide without the phase shifter is calculated at first, then the theoretical capacitance of the diode is added into the capacitance of the unloaded coplanar waveguide so as to estimate the overall effect. In other reported equivalent circuit models the distributed parameters are actually extracted from the FEM simulation [24] or the experimental data [23].

In this paper we deduce an analytical equivalent circuit model for the traveling wave electrode which drives carrier-depletion-based silicon modulators. It agrees quite well with the FEM simulation and the measurement result. Based on the model we design the traveling wave electrode and discuss the influence of different termination impedances. A 3 dB modulation bandwidth of 15 GHz is demonstrated with a 3 mm electrode.

II. Transmission Line Equivalent Circuit

A carrier-depletion-based silicon modulator with the traveling wave electrode is a Mach-Zehnder interferometer in silicon-on-insulator (SOI). At least one of its two arms contains a PN junction so as to shift the optical phase. The cross section of a typical phase shifter is shown in Fig. 1, where a coplanar waveguide (CPW) acts as the traveling wave electrode [14], [19], [25]. Free carriers are extracted from the p^+ and n^+ doped regions by a reverse bias, thus a carrier depletion region is left inside the rib as outlined by the dotted line in Fig. 1(a). According to the optical waveguide theory, the modulation efficiency of this structure is proportional to the square root of the doping concentration in the carrier depletion region, so both p^+ and n^+ areas have a relatively high doping concentration of $10^{18}/cm^3$ [11]. The *p* and *n* type silicon in Fig. 1 is lightly doped in order to reduce the optical loss. However, a low doping concentration would lead to a high series resistance and thus limit the bandwidth. A typical value based on a trade-off between the operation speed and the optical loss can be $2\times 10^{17}/cm^3$. Two contact areas far away from the optical mode center are heavily doped to $10^{20}/cm^3$. They are connected to copper electrodes by silicided regions and tungsten vias, matching a standard CMOS contacting process. Our simulation indicates that the figure of merit $V_\pi L_\pi$ of this doping scheme is 1.92 V·cm [11]. In order to achieve enough modulation depth with a small driven signal, the phase shifter is chosen to be 2 mm. Its DC modulation characteristic is shown in the inset of Fig. 1(a). The insertion loss due to doping is 3.25 dB. Provided that the modulator is biased at 6 V where the light is sensitive to the voltage variation, a 1 V sinusoidal signal is able to extinct the beam by 5.2 dB (modulation depth of 67.7%), which is sufficient for most applications [1]. Meanwhile the width of the carrier depletion region varies within 8% of its value at the DC bias point. The traveling wave electrode in Fig. 1 is actually a nonlinear transmission line since the PN junction capacitance is voltage-dependent. However, because of the 2 mm electrode we can drive the modulator in the small signal regime. Under the small signal approximation the carrier depletion region can be

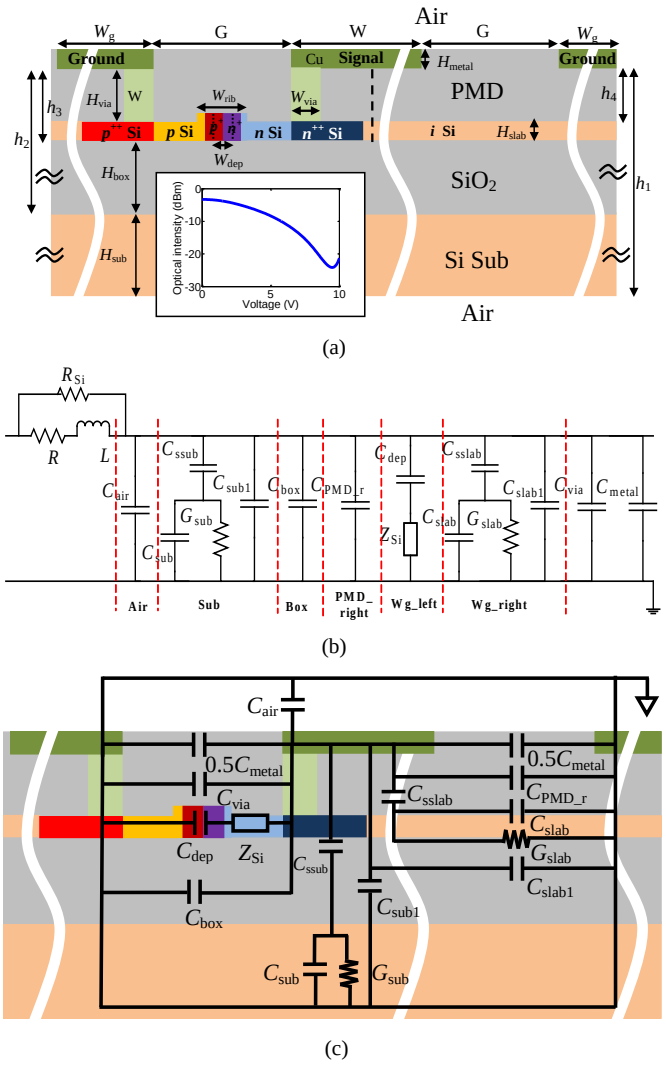


Fig. 1. (a) The cross section and the DC modulation characteristic (inset) of a typical carrier-depletion-based optical modulator in SOI with a coplanar waveguide of 2 mm as the electrode. (b) The transmission line equivalent circuit model of the traveling wave electrode shown in Fig. 1(a). (c) Relation between the circuit and the physical device.

treated as an insulator with constant width according to [26].

Relying on the specific RF frequency, silicon resistivity and device dimension, the transmission line in Fig. 1(a) supports 3 microwave propagation mechanisms which have been widely investigated: the skin effect mode, the slow wave mode and the dielectric quasi-TEM mode [27]-[29]. Here we give a brief overview about them in terms of the particular structure in Fig.1 (a):

- If the *p* and *n* regions in Fig. 1(a) which sandwich the space charge region are lightly doped, they exhibit a small dielectric loss tangent at the operation frequency. Therefore, silicon in the *p* and *n* regions acts like a dielectric. Both the transverse electric and the transverse magnetic fields can freely penetrate into the *p* and *n* doped silicon. The propagation mode is so-called “dielectric quasi-TEM mode”.
- If the *p* and *n* regions are moderately doped, the dielectric relaxation frequency of the two areas can be higher than the operation frequency. This implies the free carriers outside the space charge region respond rapidly enough to shield the

interior part of the p^+ and n^+ doped regions from the external AC field. Therefore, the electrical field of the microwave is constrained inside the space charge region. In the meanwhile if the widths of the *p* and *n* regions are less than a skin depth, the magnetic field will penetrate through the *p* and *n* regions while the electrical field does not. Such a spatial separation between electric and magnetic energies leads to the propagation of the so-called "slow-wave mode". Its effective dielectric constant is bigger than the permittivity of any medium that comprise the transmission line [27], [28].

- If the *p* and *n* regions are heavily doped to an extremely high conductivity, their width will be bigger than the skin depth. The *p* and *n* regions behavior like two lossy conductor walls, since neither the electric nor magnetic fields can penetrate them. The mode then is called the "skin-effect mode" [27], [28].

Since the skin effect mode requires a very high doping concentration which is impractical for the optical modulator, only the slow wave and the dielectric quasi-TEM modes are relevant. Y. R. Kwon has corroborated that a quasi-TEM analysis technique is valid for the slow wave mode guided by a micron-size CPW, as the very small cross-section of the transmission line ensures that transverse fields are essentially quasi-static [30]. Above arguments manifest that a quasi-TEM analysis applies to the CPW in Fig. 1(a), so this structure can be described by an equivalent circuit effectively.

The partial-capacitance technique is employed to deduce the equivalent circuit from the structure in Fig. 1(a) [31], [32]. This method is based on the assumption that all dielectric/dielectric interfaces are along electric field lines, thus magnetic walls can be placed at these interfaces. Under this assumption a CPW on a multilayered substrate can be split into several CPWs on different single-layer substrates with modified dielectric constants. The capacitance per unit length of each partial CPW component can be calculated by conformal mapping. The capacitance of the practical CPW then is the sum of all partial capacitances. Although the partial-capacitance technique is an approximation, it is proved to be effective for the CPW on regular multilayered substrate [31]. We believe that this method also applies to the irregular structure in Fig. 1(a), since the electrical field inside the carrier depletion region is definitely parallel with the interface between the Si waveguide layer and the buried SiO_2 layer.

Using the conformal mapping and partial capacitance techniques, we get the equivalent circuit model shown in Fig. 1(b). We mark physical origins for all elements in Fig. 1(c). For the air space above the electrode and beneath the Si substrate, its capacitance can be written as [31], [32]

$$C_{\text{air}} = 4\varepsilon_0 \frac{\mathrm{K}(k_0')}{\mathrm{K}(k_0)} - 2\varepsilon_0 \frac{\mathrm{K}(k_1')}{\mathrm{K}(k_1)} \tag{1}$$

where $\mathrm{K}(k_i)$ is the complete elliptic integrals of the first kind. Its modulus k_i is given by

$$k_0 = \frac{x_c}{x_b}\sqrt{\frac{x_b^2 - x_a^2}{x_c^2 - x_a^2}} \tag{2}$$

$$k_i = \frac{\sinh(\frac{\pi x_c}{2h_i})}{\sinh(\frac{\pi x_b}{2h_i})}\sqrt{\frac{\sinh^2(\frac{\pi x_b}{2h_i}) - \sinh^2(\frac{\pi x_a}{2h_i})}{\sinh^2(\frac{\pi x_c}{2h_i}) - \sinh^2(\frac{\pi x_a}{2h_i})}} \tag{3}$$

with $k_i' = (1 - k_i^2)^{1/2}$, $x_a = W/2$, $x_b = x_a + G$, $x_c = x_b + W_g$ and $i = 1,2,3,4$. The structural parameters *W*, *G*, W_g, and h_i are denoted in Fig. 1(a). Analogically the capacitance of the buried SiO_2 (BOX) layer is

$$C_{\text{box}} = 2\varepsilon_0\varepsilon_{\text{SiO}_2} \frac{\mathrm{K}(k_2')}{\mathrm{K}(k_2)} - 2\varepsilon_0\varepsilon_{\text{SiO}_2} \frac{\mathrm{K}(k_3')}{\mathrm{K}(k_3)} \tag{4}$$

Unlike the BOX layer, the Silicon substrate is a semiconducting layer with non-zero conductivity, thus 4 elements are required to describe its behavior as shown in Fig. 1(b) [33]. According to [33] and [34], the transverse conductive and displacement currents in the Si substrate are represented by a conductor G_{sub} and a capacitor C_{sub} respectively

$$C_{\text{sub}} = 2\varepsilon_0\varepsilon_{\text{Si}} \frac{\mathrm{K}(k_1')}{\mathrm{K}(k_1)} - 2\varepsilon_0\varepsilon_{\text{Si}} \frac{\mathrm{K}(k_2')}{\mathrm{K}(k_2)} \tag{5}$$

$$G_{\text{sub}} = \frac{2}{\rho_{\text{sub}}}\left[\frac{\mathrm{K}(k_1')}{\mathrm{K}(k_1)} - \frac{\mathrm{K}(k_2')}{\mathrm{K}(k_2)}\right] \tag{6}$$

where ρ_{sub} is the resistivity of the silicon substrate. The capacitor C_{ssub} which is connected in series to G_{sub} and C_{sub} represents the capacitance between the signal metal and the Si substrate. It can be written as

$$C_{\text{ssub}} = \varepsilon_0\varepsilon_{\text{SiO}_2} \frac{W}{h_2} \tag{7}$$

Here we neglect the Si waveguide layer since it is very thin (0.22 um), and assume the medium for the PMD layer is also SiO_2. The capacitor C_{sub1} does not represent any substantial part in Fig. 1(a). However, it is indispensable to make the model stand up at the high frequency limit [33]. If the frequency is high enough, the conductive current is negligible compared with the displacement current, i.e. the capacitor C_{sub} effectively shunts the conductor G_{sub}. Therefore, the Si substrate can be regarded as a dielectric. According to the partial-capacitance technique, this dielectric layer should be described by the single capacitor C_{sub} in (5), so a parallel capacitor C_{sub1} is added to make sure that the total capacitance converges at C_{sub} at the high speed limit [33]

$$C_{\text{sub}} = \frac{C_{\text{sub}}C_{\text{ssub}}}{C_{\text{sub}} + C_{\text{ssub}}} + C_{\text{sub1}} \tag{8}$$

The capacitance C_{sub1} then is determined by (8).

The Si waveguide and PMD layers are calculated by first dividing each layer into two parts along the midline of the signal metal which is shown in Fig. 1(a) by the dash line [35]. The right side can be regarded as one half of a regular CPW, so the PMD layer can be represented by a capacitor ($C_{\text{PMD\_r}}$) while the Si waveguide layer (the Si slab after waveguide etching) is described by 3 capacitors and 1 conductor (C_{slab}, G_{slab} C_{sslab} and C_{slab1}). The procedure to calculate these elements is the same as that to calculation C_{sub}, C_{ssub}, C_{sub1}, and C_{box}, except that

corresponding expressions should be divided by a factor of two. On the other hand, in order to characterize the waveguide and the PMD layers on the left side, we take the impedance of the doped silicon, the capacitance of the PN junction, and the capacitance between two vias into account. Due to the small thickness of the optical waveguide, the fringe field should not be neglected when we calculate the PN junction capacitance. If the influence of rib is neglected, the doped silicon sandwiching the carrier depletion region can be regarded as two plates of finite thickness, therefore the reverse biased PN junction can be treated as a parallel-plate capacitor. W. H. Chang gave a formula to calculate the capacitance between two finite thickness plates which takes the fringing field in to account [36]. However, in his calculation the medium outside the capacitor where the fringing field exists is the same as that between the plates. In contrast the PN junction in Fig. 1(a) is between the PMD and the BOX layers, so W. H. Chang's formula should be modified

$$C_{\text{dep}} = (C_1 - \varepsilon_0\varepsilon_{\text{Si}}\frac{H_{\text{rib}}}{W_{\text{dep}}})\frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{Si}}} + \varepsilon_0\varepsilon_{\text{Si}}\frac{H_{\text{rib}}}{W_{\text{dep}}} \qquad (9)$$

where H_{rib} and W_{dep} are the height of the rib and the width of the carrier depletion region as shown in Fig. 1(a). C_1 is W. H. Chang's capacitance formula, which is not listed here for brevity. The first term in (9) represents the fringing field in the PMD and BOX layers, while the second represents the field inside the depleted Si. The impedance of the doped silicon between the contacts and the carrier depletion region is given by

$$Z_{\text{Si}} = \frac{\rho_{\text{Si}}}{1 + \text{j}\omega_{\text{m}}\rho_{\text{Si}}\varepsilon_0\varepsilon_{\text{Si}}}\left(\frac{W_{\text{rib}} - W_{\text{dep}}}{H_{\text{rib}}} + \frac{G - W_{\text{rib}}}{H_{\text{slab}}}\right) \qquad (10)$$

where ρ_{Si} is the resistivity of the p and n doped silicon, ω_{m} is the microwave frequency. Here we assume both p^+ and n^+ doped regions are fully depleted. The impedance of the heavily doped silicon (the p^{++} and n^{++} regions) within the transfer length from the silicon to the silicide is neglected due to its high conductivity. The capacitance between two vias can simply be deduced from the PMD permittivity, the distance between the two vias and the via height: $C_{\text{via}} = \varepsilon_0\varepsilon_{\text{Si}}H_{\text{via}}/G$. Similarly the capacitance between side walls of the signal and the two ground electrodes is $C_{\text{metal}} = 2\varepsilon_0\varepsilon_{\text{Si}}H_{\text{metal}}/G$. For simplicity we assume the medium above the CPW is air in Fig. 1(a). There may be other inter metal dielectric (IMD) layers covering the CPW in practical CMOS technology. If so, the partial-capacitance technique allows us to add corresponding capacitors into the circuit so as to represent these IMD layers [31].

The last three elements to complete the equivalent circuit model are the line resistance R and the line inductance L which represent the longitudinal current flow in the electrode, and the resistance R_{Si} which represents the longitudinal current in the substrate and the Si waveguide layer. At low frequency limit, the line resistance can be calculated directly by Ohm's law, while the line conductance can be derived from common magneto-static theory. Both of them are constants in this

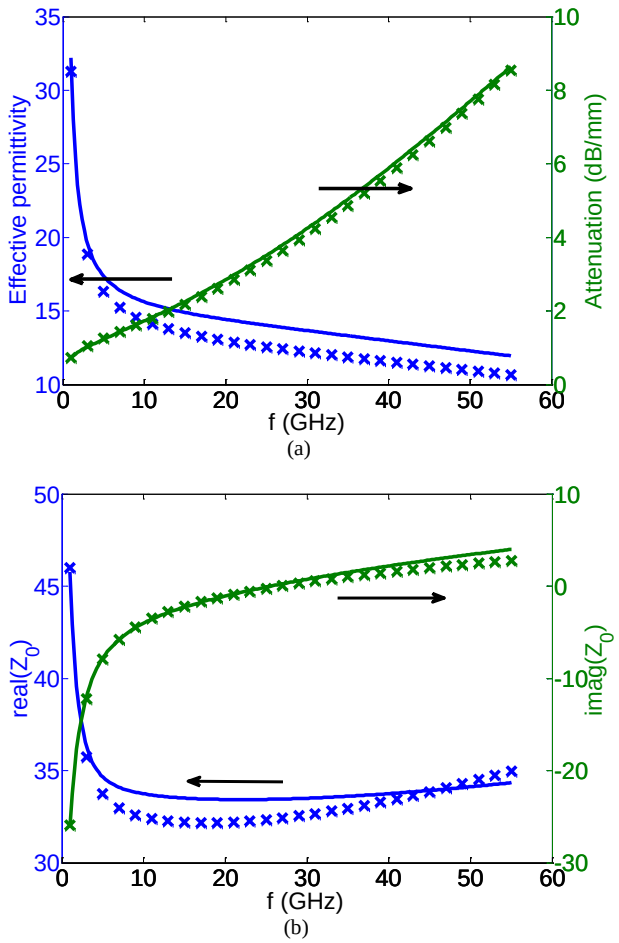


Fig. 2. A comparion between the equivalent circuit calculation and the HFSS simulation. Values of the parameters used in the comparion are: W=5 μm, H_{metal}=0.5 μm, G=2.5 μm, σ_{Si}=1/ ρ_{Si} =2500 S/m, W_{dep}=0.133 μm, H_{via}=1 μm, W_{via}=1 μm, W_{rib}=0.5 μm, H_{rib}=0.22 μm, H_{slab}=0.15 μm, H_{box}=2 μm, H_{sub}=500 μm, and ρ_{sub}=0.1 Ω·m.

frequency range. However, as the frequency increases they become frequency dependent due to the skin-effect of the imperfect metal. In the skin-effect region, the inductance can be divided into an internal and an external part. The external inductance is frequency independent, which can be obtained from the capacitance of an air-filled CPW of the same dimension. The internal inductance can be calculated by Wheeler's incremental inductance rule [35]. The same technique is also used to calculate the line resistance in the skin-effect regime. W. Heinrich has given closed-form formulas to calculate R and L of CPWs which are accurate over a large frequency range from DC to RF [35], his result is employed in our model. Because of the interaction between the magnetic field and the Si, there is a longitudinal current inside the substrate and the Si waveguide layer. This current which parallels the current inside the metal also contributes to the loss. Y. R. Kwon points out that it can be represented by a resistance R_{Si} which is connected to R and L in parallel as shown in Fig. 1 (b) [30]. Due to the small dimension of the waveguide layer and the high resistivity substrate of the practical SOI wafer, R_{Si} is far more than the impedance given by R and L, so it can be ignored.

With the equivalent circuit in Fig. 1(b), we can get the total

shunt admittance Y and the total series impedance Z per unit length. The propagation constant γ and the characteristic impedance Z_0 are determined by Y and Z as $\gamma = \sqrt{ZY}$ and $Z_0 = \sqrt{Z/Y}$. The effective permittivity ε_{eff} and the attenuation α of the transmission line are deduced from the real and the imaginary parts of γ respectively. To validate the equivalent circuit, we calculate ε_{eff}, α and Z_0, and then compare them with the simulation result of a commercial software package HFSS which uses the FEM method to solve Maxwell's equations in RF domain. The comparison result is shown in Fig. 2. We can see the equivalent circuit agrees well with the simulation in a frequency range from 1 GHz to 55 GHz. The relative errors between calculation and simulation are equal or less than 10.9%, 4.3%, and 3.9% for ε_{eff}, α, and $|Z_0|$ respectively. The small discrepancy convinces us that the equivalent circuit model is effective for designing the traveling wave electrode. In section IV the validity of the model will be further confirmed by a comparison with the experimental measurement. At low frequency ε_{eff} is higher than the permittivity of every medium in Fig. 2(a), which is a clear sign of the slow wave propagation. As the operation frequency exceeds the dielectric relaxation frequency of the p and n doped silicon, the slow wave mode evolves to the dielectric quasi-TEM mode.

III. Traveling Wave Electrode Design

In this section we calculate the frequency response of a carrier-depletion-based modulator with the equivalent circuit model we proposed in section 2. Supposing the voltage amplitude and the frequency of the driving signal are V_g and ω_m respectively, the average voltage between the signal and the ground electrodes experienced by a photon as it travels through the phase shifter is [37]

$$V_{\text{avg}}(\omega_m) = \frac{V_g(1+\rho_1)\exp(i\beta_o l)}{2\left[\exp(\gamma l) + \rho_1\rho_2\exp(-\gamma l)\right]}(V_+ + \rho_2 V_-) \quad (11)$$

$$V_\pm = \exp(\pm i\phi_\pm)\frac{\sin\phi_\pm}{\phi_\pm} \quad (12)$$

$$\phi_\pm = \frac{(-i\gamma \mp \beta_o)l}{2} \quad (13)$$

$$\rho_1 = \frac{Z_0 - Z_s}{Z_0 + Z_s} \quad (14)$$

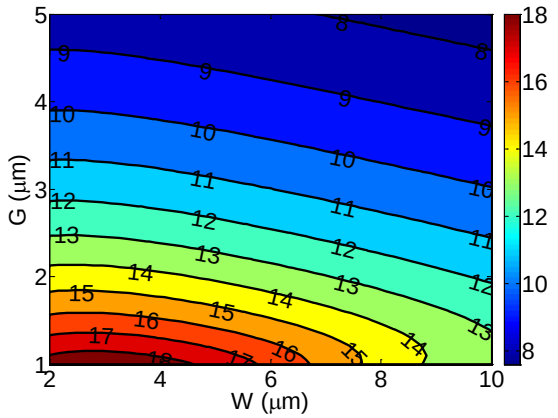
$$\rho_2 = \frac{Z_t - Z_0}{Z_0 + Z_t} \quad (15)$$

$$\beta_o = \frac{\omega_m}{c} n_o \quad (16)$$

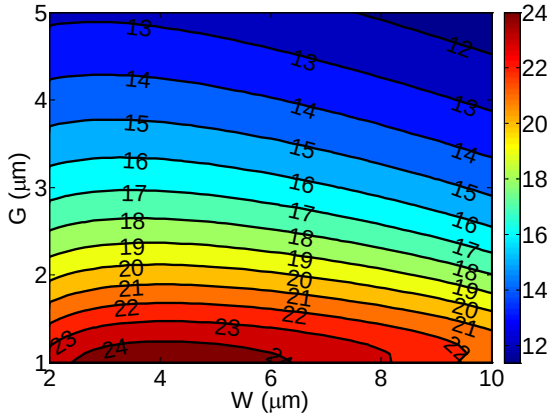
where Z_s and Z_t are the impedance of the microwave source and the terminator, respectively, l is the length of the electrode, and n_o is the group refractive index of the optical mode [38], [39]. Under a small driving voltage, the modulation depth is proportional to the average RF voltage V_{dep} that drops cross the carrier depletion region, which is the product of $V_{\text{avg}}(\omega_m)$ and the voltage division factor of the PN junction capacitor. By normalizing the modulation depth by its low frequency reference value, we get the frequency response of the modulator

$$m(\omega_m) = \left|\frac{V_{\text{dep}}(\omega_m)}{V_{\text{dep}}(\omega_0)}\right| = \left|\frac{(1+j\omega_0 C_{\text{dep}} Z_{\text{Si}})V_{\text{avg}}(\omega_m)}{(1+j\omega_m C_{\text{dep}} Z_{\text{Si}})V_{\text{avg}}(\omega_0)}\right| \quad (17)$$

where ω_0 is the lowest output frequency of the microwave source. It is 10 MHz in our calculation. It is necessary here to note that (17) has already taken the velocity match, impedance match, and the microwave loss into account [37]. The 3 dB



(a)



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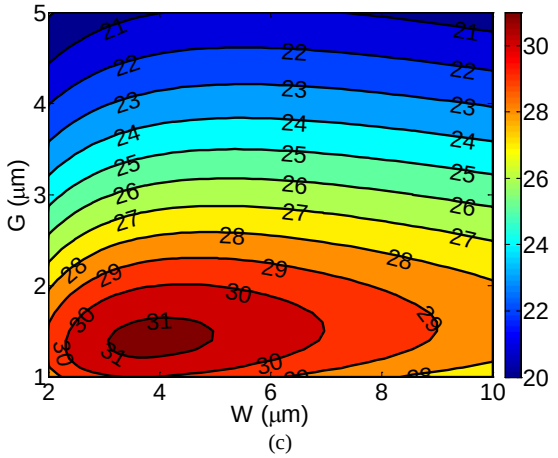

(c)

Fig. 3. 3 dB modulation bandwidth $f_{3\text{dB}}$ vs the size of CPW for different silicon conductivities. (a) σ_{si}=500 S/m. (b) σ_{si}=1000 S/m. (c) σ_{si}=2500 S/m. Parameters take the following values in the calculation: Z_s=Z_t=50 Ω, l=2 mm, n_o=3.59, H_{metal} =0.5 μm , and W_{dep}=0.133 μm, other parameters are the same as those in Fig. 2.

optical modulation bandwidth f_{3dB} is the frequency where $m(\omega_m)$ falls by 50%.

Based on above discussion, we can design the CPW in terms of increasing its modulation bandwidth. As mentioned in section 2, the electrode in our bandwidth calculation is chosen to be 2 mm, while the DC bias voltage is 6 V. Of course cutting the electrode length scales up the bandwidth but with the expense of a weakened modulation depth. The width of the carrier depletion region is 133 nm according to the specific doping concentration and the bias voltage. Figure 3 presents contour maps of the 3 dB modulation bandwidth as a function of the size of CPW for different silicon conductivities σ_{si}. In Fig. 3(c) the modulator exhibits the largest bandwidth when the signal electrode width is between 3 μm and 6 μm. On the other hand, we can improve the modulation bandwidth by increasing the silicon conductivity σ_{si}, or by shrinking the gap G between the signal and the ground electrodes. This can be explained by reducing the series impedance between the carrier depletion region and the two contacts. However, the side-effect is an increased optical loss. A trade-off then depends on the particular requirement about the bandwidth and the optical loss. A typical gap G is 2.5 μm so as to isolate the optical mode from contact areas, thus from Fig. 3(c) a conductivity of σ_{si}= 2500 S/m is enough to support a 28 GHz bandwidth. The doping level of this conductivity is less than 1e18/cm^2, so the resultant optical loss is inside the safe region.

In Fig. 3 we calculate the 3 dB modulation bandwidth which is dominated by three factors: the velocity mismatching, the impedance mismatching and the RF loss. It is necessary to single out the effect of each factor and find out which one is the major factor that limits the bandwidth. For a lossless modulator with impedance-matched load and generator (Z_s=Z_t=Z_0), its 3 dB modulation bandwidth which is determined only by the velocity mismatching between the RF and optical signals can be calculated as [38]

$$f_{3dB} = \frac{0.18}{l(n_m - n_o)}\text{GHz} \qquad (18)$$

where l is the electrode length, n_m is the microwave refractive index, and n_o is the group refractive index of optical mode rather than the effective refractive index [39]. The microwave refractive index of the coplanar waveguide calculated in Fig. 2(a) is $n_m = \sqrt{\varepsilon_{eff}} = 3.71$ at 28 GHz. On the other hand the group refractive index of the optical mode is n_o=3.59 at 1.55 μm for our waveguide. If we ignore the microwave loss and the impedance mismatching, a modulator bandwidth of 750 GHz is expected for an electrode of 2 mm according to (18). This is far beyond the final bandwidth of 28 GHz shown in Fig. 3(c). Therefore, as a result of the short electrode the bandwidth is not limited by the velocity mismatching but by the impedance mismatching together with the microwave loss.

Since the output impedance of microwave sources is always 50 Ω, here we only analyze the impact of the termination impedance. The frequency responses of a MZ modulator with different terminators are displayed in Fig. 4(a). We find that a small resistor is beneficial for increasing the bandwidth. L. Liao found the similar phenomenon in their experiment [40], he attributes the reason to the reflections resulting from the impedance mismatching which then pre-emphasizes the RF signal. Actually this phenomenon can be understood by examining the modulation depth, which can be characterized by the voltage V_{dep} as we have indicated. The evolution of V_{dep} with the frequency is presented in Fig. 4 (b), where V_{dep} is already normalized by the amplitude of the driving voltage V_g. We find that decreasing the resistance of terminator doesn't really enhance the modulation depth at high frequency. Instead, the operation bandwidth is improved by suppressing the modulation depth at low frequency [37]. At the DC limit the voltage on the transmission line is $V_g Z_t /(Z_s + Z_t)$ due to the fact that the DC resistance of the CPW is negligible, so the static modulation depth degrades with reducing the termination resistance.

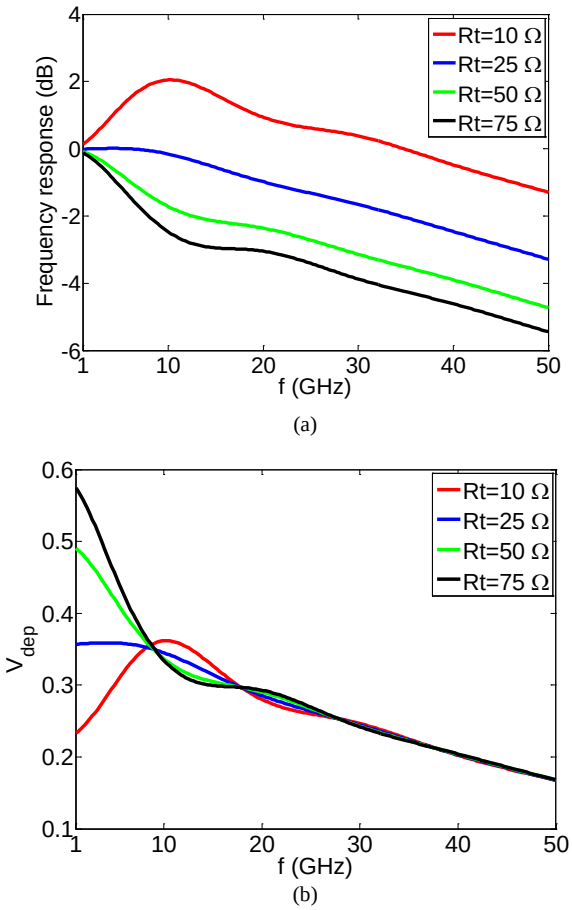

Fig. 4. Frequency response (a) and modulation depth (b) of a modulator with different termination resistors. Parameters in the calculation are: W =5 μm , G=2.5 μm and σ_{si}=2500 S/m. Other parameters are the same as those in Fig. 3.

IV. EXPERIMENTAL RESULT

In order to fully prove its validity, we compare the equivalent circuit model with the measurement result of a practical modulator in Fig. 5. The nominal doping concentration in the p^+ and the n^+ doped regions is 2×10^{18}/cm^3 for the practical device, while that in the p and the n doped regions is 0.6×10^{18}/cm^3. The width of the central signal metal is 6 μm. The gap between the

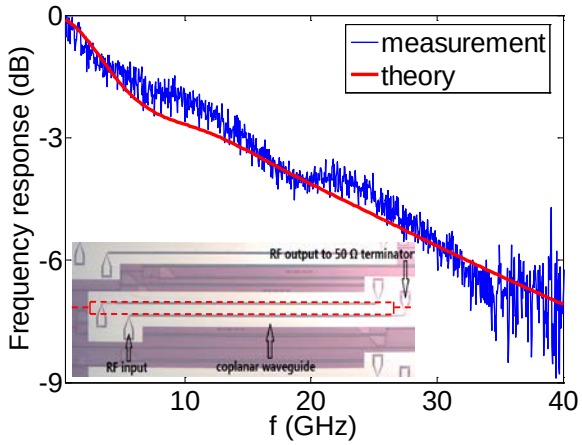

Fig. 5. Comparison between the theoretical calculation and the measurement result. The inset shows a microscope image of the practical device.

central metal and two grounds is 3.5 μm. The length of phase shifter is 3 mm. A description about the device fabrication and characterization is in [41]. The inset within Fig. 5 shows a microscope image of the device.

Since silicon in the *p* and the *n* doped regions exhibits different conductivities because of the mobility difference between electrons and holes, for simplicity we can take their mean value of σ_{si}= 1300 S/m in the calculation. In Fig. 5 the DC reverse bias applied is -4 V. Taking the practical doping profile of gradient PN junction into account [11], we estimate the width of carrier depletion region is 0.11 μm. Substituting these parameters into our equivalent circuit model, we calculate the frequency response with (17). In Fig. 5 there is a good agreement between the calculation and the measurement result, which confirms the validity of our model. With this device, we are able to obtain an error free modulation at 35 Gbit/s [41].

V. Conclusion

In this paper we propose an equivalent circuit model for the traveling wave electrode which drives carrier-depletion-based optical modulators. Closed form expressions are deduced for every element in the circuit. Based on the model, we design the CPW for high speed modulation, and calculate the frequency response of a practical device. The calculation agrees well the final measurement result. Our calculation manifests that with a conservative doping concentration which would not cause too much optical loss and a phase shifter as long as 2 mm, a well designed CPW is able to support a 3 dB bandwidth of 28 GHz as well as a high modulation depth. This point is also confirmed by recent published results of 40 Gbit/s and 50 Gbit/s modulators which are based on similar structures [14], [42].

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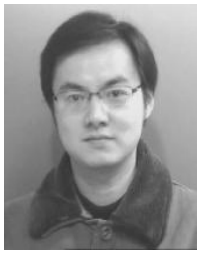

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