Sampling Algorithm for Small Input Current Distortion in Digitally Controlled Boost PFC Converters

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Abstract

After a short introduction to the digital control of boost power factor correction converters, the principle of operation of the alternating-edge-sampling algorithm is reviewed. The main features of this sampling algorithm are: switching noise immunity, straightforwardness, the need for only few extra processor cycles and accurate measurement of the averaged input current. However, to accomplish this last feature the timing of the sampling instants has to be tuned manually. Moreover, the "ideal" timing instants may slowly vary because of temperature effects and during the life-time of the converter. To annihilate these effects and to avoid manual tuning, the alternating-edge-sampling algorithm is extended with an auto-tuning feature for the timing of the sampling instants. The distortion caused by the sampling algorithm due to an inaccurate timing of the sampling instants is quantified to obtain an estimate for the timing error. This timing error is continuously monitored and intermittently used to adjust the timing of the sampling instants. As a result, the proposed sampling algorithm provides accurate measurements of the averaged inductor current without manual tuning, over a wide temperature range and during the operating life-time of the converter. Experimental verification using a digitally controlled boost converter demonstrates the feasibility of the proposed sampling algorithm and demonstrates that a small input current distortion can be achieved.

I. Introduction

During the last decade, there has been a large interest in power factor correction (PFC) [1]–[8]. For price reasons, the control algorithms for single-phase PFC converters are in most cases implemented as analogue circuits. With the advent of fast digital signal processors (DSP), embedding control peripherals such as pulse-width-modulation (PWM) units, analogue-to-digital converters (ADC), etc., new and more complicated control algorithms become feasible. For the near future, as the ratio price/performance of DSPs is expected to decrease further, there is a fair chance that the analogue control circuits will be abandoned in favour of digital implementations. This tendency can be illustrated by the recent interest in digital control of PFC converters [2]–[8].

In [8], a sampling algorithm intended for symmetric or centre-based PWM was proposed. The main features of the sampling algorithm are: switching noise immunity, straightforwardness, need for only few extra processor cycles and accurate measurement of the averaged input current. However, this last feature involves a manual tuning of the timing of the sampling instants (see section II.). As manual tuning is time-consuming and prone to human error, in this paper the algorithm of [8] is extended with an auto-tuning feature for the timing of the sampling instants. Hence, accuracy of the measurement

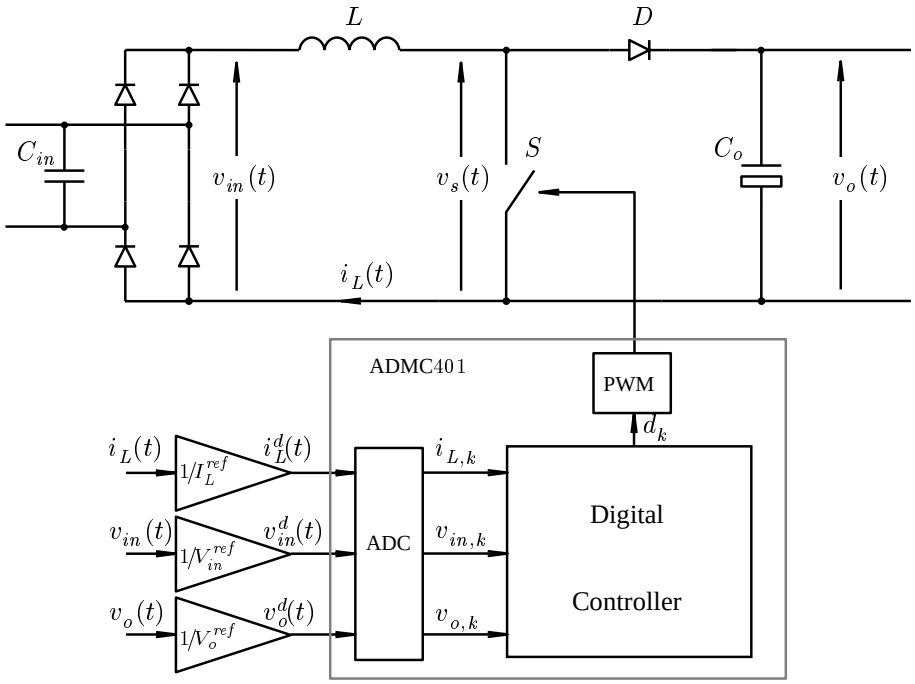

Fig. 1. A digitally controlled boost PFC converter.

of the averaged input current doesn't require human intervention and can be guaranteed over a wide temperature range and during longer periods of time. The theoretical results obtained are validated using an experimental setup of a digitally controlled boost PFC converter.

The general scheme of a digitally controlled boost PFC converter is depicted in Fig. 1. For the purpose of digital control the control variables (inductor current i_L, input voltage v_{in}, and the output voltage v_o) are sensed, processed by analogue amplifiers and sampled by the ADC. The obtained digital quantities are then used by the control algorithm to calculate the duty-ratio d_k for the switch S. The main target of the control algorithm is to maintain a virtually constant output voltage and to force the inductor current to accurately track the wave shape of the input voltage.

As the output of the ADC is always in fixed point n-bit notation, the largest positive number that can be represented is either $(011...11)_{\mathrm{B}}$ for a signed format or $(111...11)_{\mathrm{B}}$ for an unsigned format. This largest positive quantity corresponds in $(1.n-1)$-complement notation and unsigned $(0.n)$-format respectively with

$$\begin{aligned}(011...11)_{\mathrm{B}} &= 1-2^{-(n-1)}\\ (111...11)_{\mathrm{B}} &= 1-2^{-n},\end{aligned}$$

or, when a sufficiently high number of bits is used, with approximately 1. This corresponds also with the largest value of a sensed control variable that can be represented digitally. If each control variable is divided by its maximum value that can be represented digitally (I_L^{ref}, V_{in}^{ref}, and V_o^{ref}) some sort of per unit system is obtained in which the per unit value (i_L^d, v_{in}^d, and v_o^d) is directly related to the digital representation obtained after the ADC.

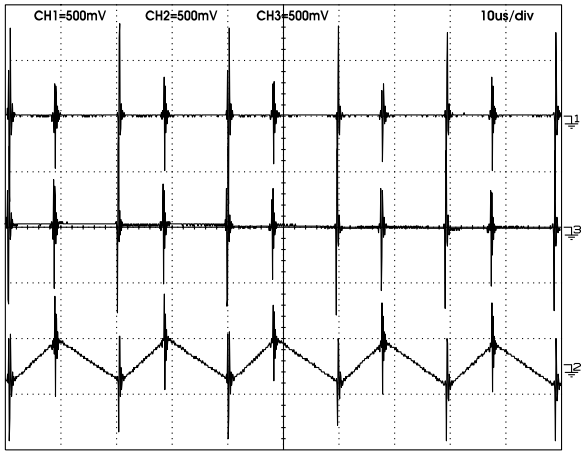

Fig. 2. The three control variables before the ADC. Signals from top to bottom: the output voltage, the input voltage, the input current.

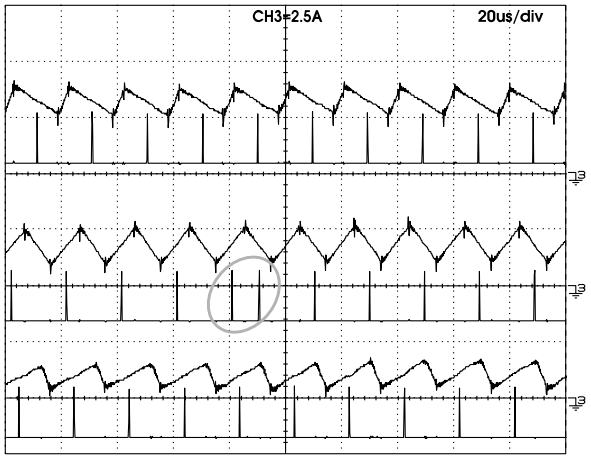

Fig. 3. The sampling instants for the AES algorithm. *Upper traces:* small d_k. *Centre traces:* transition. *Lower traces:* large d_k.

II. Review of the Alternating-Edge-Sampling Algorithm

A. The Principle of Operation

The alternating-edge-sampling algorithm was presented in [8]. As in the current paper the alternating-edge-sampling algorithm is extended with an auto-tuning feature guaranteeing an accurate measurement of the averaged input current, the operating principle of the alternating-edge-sampling algorithm is reviewed briefly in this section.

The switching of the boost converter causes a switching ripple with large magnitude on the input current (Fig. 2, lower trace). To avoid aliasing of the switching ripple, the sampling frequency should be chosen at least ten times higher than the switching frequency. As a very high sampling frequency would pose a heavy burden to the processor, the sampling is synchronized with the switching of the converter. Because of this, the switching ripple on the input current becomes a hidden oscillation, not appearing in the reconstructed signal. Moreover, for continuous conduction mode, if the samples are taken in the middle of the rising edge or in the middle of the falling edge of the measured inductor current, the obtained samples are a direct measure for the averaged inductor current $\langle i_L \rangle$ (averaged over one switching cycle).

Due to switching noise coupled to the sensors and to the signal chain during switching transitions, high peaks (ringing) appear on all control variables offered to the ADC (Fig. 2). As the sampling of a real ADC lasts a finite time, the accuracy of the sampled output is affected by sudden changes of the sampled input during the sampling. Consequently, the occurrence of high frequency switching noise during the sampling process will result in improper system behaviour due to large errors on the value of the obtained samples. Hence, a careful selection of the sampling instants is necessary.

This may be accomplished by using alternately the middle of the rising edge or the middle of the falling edge of the measured (by the ADC) inductor current as sampling instant. When the duty-ratio is large (Fig. 3 lower traces), the sampling occurs in the middle of the rising edge of the measured inductor current, when the duty-ratio is small (Fig. 3 upper traces) the sampling instant is moved to the middle of the falling edge. To decide upon the sampling edge for the next PWM-cycle the duty-ratio is compared to a cross-over duty-ratio δ_c (Fig. 3 centre traces). If the cross-over duty-ratio δ_c is set to $1/2$ and the duration of the ringing on the measured signals caused by the switching transitions is less than $T_s/4$ (which is the case in a properly designed system), this ringing will not coincide with the sampling, guaranteeing proper measurements. The resulting sampling algorithm is called alternating-edge-sampling.

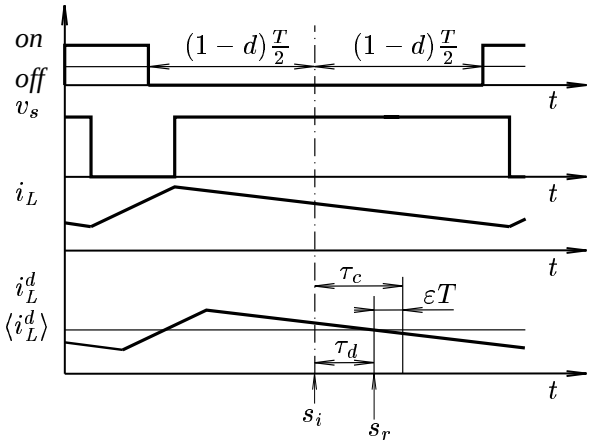

Fig. 4. The delay between the centre of the PWM commands and the middle of the rising edge of the measured inductor current.

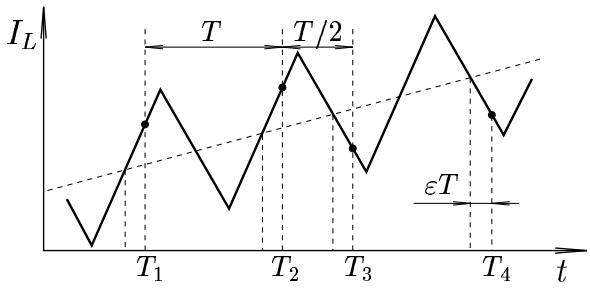

Fig. 5. Measurement error on inductor current due to sampling-instant inaccuracy.

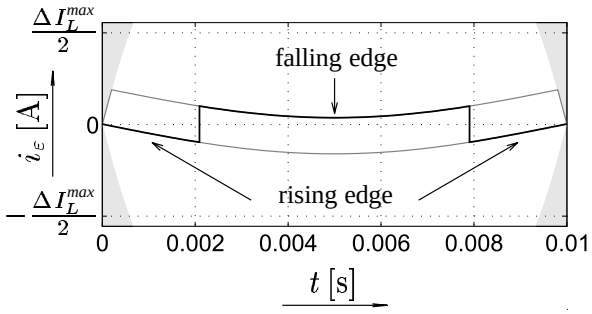

Fig. 6. Input current error caused by incorrect timing of the sampling instants for $\varepsilon = 2\%$ (during half a mains period, 50Hz).

B. Input Current Distortion Induced by the Sampling Algorithm

To obtain accurate samples of the averaged inductor current $\langle i_L \rangle$, the sampling instants must be exactly in the middle of the rising or the falling edge of the measured inductor current. From the processor point of view the centre of the PWM commands can be accurately determined. However, the centre of the rising or falling edge of the measured inductor current differs from the centre of the PWM commands because of the phase-lag induced by the low-pass filters in the signal chain and because of the delay between the switching commands of the processor and the actual switching of the switch S (Fig. 4); the total delay is represented by τ_d. This delay can be compensated for by postponing the sampling instants by a time τ_c with respect to the centre of the PWM commands. However, this compensation by a manually derived delay τ_c is never perfect due to measurement errors. Moreover, the delay τ_d depends on the switch-temperature and may vary over time. As a result there is always a small difference between the delay τ_d and its compensation τ_c: the timing error εT ($\varepsilon > 0$ in Fig. 4). Due to this timing error the obtained samples are different from the averaged inductor current (Fig. 5). As the current-loop controller treats the retrieved samples as if they were samples of the averaged inductor current, distortion is induced in the inductor current waveform.

For alternating-edge-sampling the inductor current distortion can be understood intuitively. When the input voltage is low, the duty-ratio is high and the sampling instant appears during the rising edge of the inductor current. Assuming that the sampling instants appear a time εT late ($\varepsilon > 0$), the measured value of the inductor current is higher than the averaged value (samples T_1 and T_2 in Fig. 5). As the current compensator will force the obtained samples to track the desired inductor current, the averaged inductor current will be too low. While the input voltage rises, the duty-ratio sets until it becomes smaller than $1/2$.

When this occurs the sampling edge is moved from the rising edge to the falling edge and the measured values of the inductor current suddenly become underestimates for the averaged inductor current (T_3 and T_4 in Fig. 5). The current compensator reacts to this jump in the measured inductor current and tries to increase the inductor current and the averaged inductor current becomes too high. Hence, each time the sampling instant is swapped from the rising edge to the falling edge or vice-versa, a transient in the inductor current is visible that is inverse to the jump in the measured inductor current. The input current error i_ε caused by a positive relative timing error ε is shown in Fig. 6 ($\Delta I_L^{max} = \frac{V_o T}{8L}$ with V_o the output voltage, or ΔI_L^{max} is the maximum input current ripple).

III. Alternating-Edge-Sampling with Timing Error Compensation

Instead of manually deriving the value for the compensation time delay τ_c, the processing power of the digital controller can be applied to continuously monitor the timing error εT and correct the compensation delay τ_c accordingly. This also allows to compensate for the time effects and temperature effects on the delay τ_d. To derive an expression for the timing error, the jump in the measured inductor current caused by a transition in sampling edge from rising to falling is analysed using Fig. 5.

As the digital controller is a causal system, it will not respond to the change in measured inductor current before it has occurred. Hence, the sample retrieved at T_3 doesn't contain the response of the controller and is only due to the change in sampling slope. From T_4 onwards the current controller reacts to the alleged jump in the inductor current and forces the measured inductor current back to its original track. As a consequence, the difference between the samples of the inductor current at T_2 and T_3 is a function of only the timing error εT and not of the controller parameters. The change of the measured input current during the transition can be expressed as

$$\begin{aligned} i_L(T_3) - i_L(T_2) &= [i_L(T_3) - i_L(T_3 - \varepsilon T)] - [i_L(T_2) - i_L(T_2 - \varepsilon T))] + \\ & \quad i_L(T_3 - \varepsilon T) - i_L(T_2 - \varepsilon T). \end{aligned} \tag{1}$$

This can be written as

$$i_L(T_3) - i_L(T_2) \approx \varepsilon T \left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\substack{\text{falling}\\ \text{edge}\\ t = T_3}} - \varepsilon T \left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\substack{\text{rising}\\ \text{edge}\\ t = T_2}} + i_L(T_3 - \varepsilon T) - i_L(T_2 - \varepsilon T). \tag{2}$$

By substituting the expressions for the slopes of the inductor current of the boost converter for the rising and falling edges

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\substack{\text{falling}\\ \text{edge}\\ t = T_3}} = \frac{v_{in}(T_3) - v_o(T_3)}{L} \tag{3}$$

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\substack{\text{rising}\\ \text{edge}\\ t = T_2}} = \frac{v_{in}(T_2)}{L} \tag{4}$$

in (2), this equation can be written as

$$i_L(T_3) - i_L(T_2) = \frac{\varepsilon T}{L}\left[\Big(v_{in}(T_3) - v_{in}(T_2)\Big) - v_o(T_3)\right] + i_L(T_3 - \varepsilon T) - i_L(T_2 - \varepsilon T). \tag{5}$$

TABLE I

Annihilation of the timing error after successive iterations of the timing error compensation algorithm with large error on the calculation: (a) $\frac{\widehat{\varepsilon T}}{\varepsilon T} = 0.6$, and (b) $\frac{\widehat{\varepsilon T}}{\varepsilon T} = 1.4$.

(a)

$\frac{\varepsilon T}{T_p}$	$\widehat{\frac{\varepsilon T}{T_p}}$	round($\widehat{\frac{\varepsilon T}{T_p}}$)
10	6.0	6
4	2.4	2
2	1.2	1
1	0.6	1
0	0.0	0

(b)

$\frac{\varepsilon T}{T_p}$	$\widehat{\frac{\varepsilon T}{T_p}}$	round($\widehat{\frac{\varepsilon T}{T_p}}$)
10	14.0	14
-4	-5.6	-6
2	2.8	3
-1	-1.4	-1
0	0.0	0

Taking into account that the change of the input voltage in half a switching period $[v_{in}(T_3) - v_{in}(T_2)]$ is very small compared to the value of the output voltage $v_o(T_3)$ and that the rise of the input current over half a switching period $[i_L(T_3 - \varepsilon T) - i_L(T_2 - \varepsilon T)]$ that is not caused by the sampling algorithm, can be estimated from the previous samples, (5) becomes

$$i_L(T_3) - i_L(T_2) \approx -\frac{\varepsilon T}{L} v_o(T_3) + \frac{i_L(T_2) - i_L(T_1)}{2}. \tag{6}$$

This finally yields an expression for the timing error for a transition of sampling edge from rising edge to falling edge

$$\varepsilon T = \frac{L}{2v_o(T_3)} \left(-i_L(T_1) + 3i_L(T_2) - 2i_L(T_3)\right). \tag{7}$$

In a similar manner, an expression for the timing error calculated from a transition of sampling edge from falling to rising edge can be derived

$$\varepsilon T = -\frac{L}{2v_o(T_3)} \left(-i_L(T_1) + 3i_L(T_2) - 2i_L(T_3)\right). \tag{8}$$

Again T_3 corresponds with the sample right after the transition while T_1 and T_2 are the timing instants of the two previous samples.

As the inductance L is known and the output voltage $v_o(T_3)$ is measured for the output voltage control loop, the processor has all the required data to calculate the timing error εT in (7) and (8). This value of the timing error allows the processor to adapt its sampling instants, resulting in an accurate measurement of the inductor current. By monitoring the value of the timing error εT at every transition from rising-edge to falling-edge and vice-versa (4 times in a grid-period), the measurement of the averaged inductor current maintains its accuracy over a wide range of switch-temperatures and during a long period of time.

IV. Implementation Issues for the Timing Error Compensation Algorithm

Equations (7) and (8) allow to theoretically calculate the value of the timing error. However, the processor requires a value of the timing error relative to the processor cycle time T_p. Moreover, the per unit system introduced in Fig. 1 alters the constants of (7) and (8). If the processor employs a fixed point

n-bit representation, the timing error relative to the processor cycle time can be expressed by using a $1.(n-1)$-complement representation as

$$(\varepsilon T)^d = \frac{\varepsilon T}{T_p\, 2^{n-1}}. \tag{9}$$

If the expressions for the per unit system are applied, the processor representation of the timing error (7) can be rewritten (a similar procedure can be used to rewrite (8))

$$(\varepsilon T)^d = \frac{L I_L^{ref}}{2^n\, T_p V_o^{ref} v_o^d(T_3)} \left(-i_L^d(T_1) + 3 i_L^d(T_2) - 2 i_L^d(T_3) \right). \tag{10}$$

To avoid nervous reactions of the timing adjustment algorithm to small measurement errors in the successive values of the measured inductor current, the dimensionless timing error $(\varepsilon T)^d$ is passed on to a low-pass filter.

The procedure used to correct the sampling error calculates four times every grid period the value for the dimensionless timing error by using (10) and a similar expression derived from (8). These values are continuously sent to the low-pass filter. Every few seconds the timing for the sampling instants is adjusted according to the value at the output of the low-pass filter, directly followed by a reset of the output of the low-pass filter. As a consequence, the timing of the sampling instants is continuously monitored and adjusted to annihilate temperature effects and other slow variations in the delay τ_d.

Another positive effect of this repetitive correction algorithm is that there is no need to accurately calculate the value of the fraction in (10). After all, if the value for the fraction of (10) contains significant errors, the timing error is nevertheless reduced to nil after several passes of the algorithm. This is demonstrated in Tables I(a) and I(b) for a fraction that is too low (60%) or too high (140%), respectively. Therefore it is assumed that the initial relative timing error $\varepsilon T/T_p$ is 10 and that the value estimated by the processor is $\widehat{\varepsilon T}/T_p$ (estimated values are indicated as $\widehat{\cdot}$). As the processor is only capable of adjusting its timing instants in multiples of its cycle time T_p, the calculated value for the relative timing error is rounded to the nearest value before the timing correction is executed.

Since in a production environment the accuracy of inductor values is in many cases not better than 20%, the successive corrections of the timing error compensation algorithm avoid that a precise measurement of this inductor value is required. Moreover, it is no longer necessary to perform the time-consuming division by $v_o^d(T_3)$. Instead, the nominal value of the output voltage V_o^{nom} can be used in (10)

$$(\varepsilon T)^d = \frac{L I_L^{ref}}{2^n\, T_p V_o^{nom}} \left(-i_L^d(T_1) + 3 i_L^d(T_2) - 2 i_L^d(T_3) \right). \tag{11}$$

Hence, the calculation of the timing error only requires additions and multiplication, operations a modern processor can perform in only a few processor cycles.

V. Experimental Results

The sampling algorithm was tested by using an experimental test setup. The entire control for the boost PFC converter was implemented on the ADMC401 of Analog Devices. The S and D switches of the boost rectifier are MOSFET SPP20N60S5 and diode RURP3060 respectively. The passive components used have $L = 1$mH and $C = 470\mu$F. The converter switches at 50kHz, supplies 400V DC at the output and is rated at 1kW for an input voltage range of 190V–264V AC.

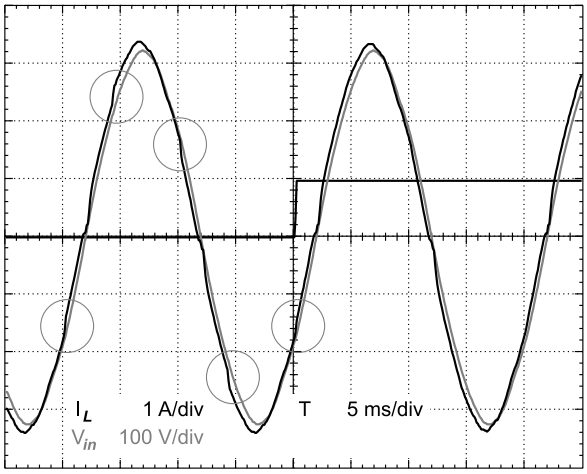

Fig. 7. Operation of the timing compensation algorithm for an initial timing error of $\varepsilon T \approx 400$ns.

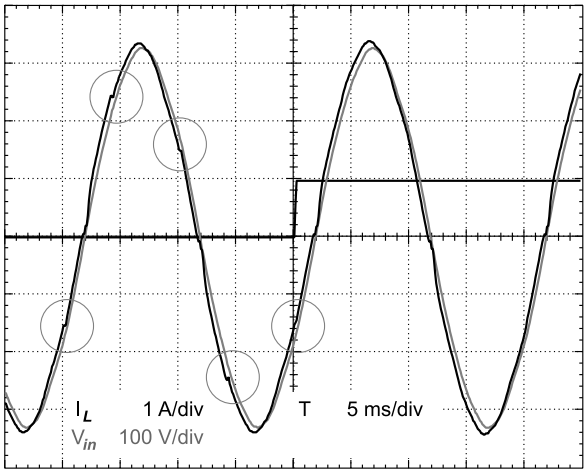

Fig. 8. Operation of the timing compensation algorithm for an initial timing error of $\varepsilon T \approx -400$ns.

The operation of the timing error compensation algorithm is demonstrated in Figs. 7 and 8. For this purpose two different initial timing errors were introduced: $\varepsilon T = 400$ns and $\varepsilon T = -400$ns respectively. On the left side of both figures the timing error compensation algorithm has not yet compensated for the timing error but is continuously calculating its value and forwarding it to the digital low-pass filter. As a result, on the left side an important timing error is present yielding important input current distortion due to jumps in the input current (encircled) where the sampling edge is moved form rising to falling and vice-versa (compare Figs. 7 and 6). On the right side of Figs. 7 and 8, the timing error compensation algorithm has corrected the timing of the sampling instants for the first time. As in our case the parameter values in the circuit (such as the inductance L) are well known, the first estimate of the timing error is very accurate and removes virtually all the distortion due to sampling-instant inaccuracy of the input current. The only input current distortion left is mainly caused by the imperfectness of the inductor current compensator.

VI. Conclusion

When the alternating-edge-sampling algorithm is used, the timing of the sampling instants is very important. After all, timing instant inaccuracy results in important input current distortion. The input current distortion is used to quantify the timing error. This results in a new sampling algorithm in which the position of the sampling instants is intermittently corrected based on the continuous measurement of the timing error. The most important features of this sampling algorithm are: switching noise immunity, straightforwardness, the need for only few extra processor cycles, accurate measurement of the averaged input current over a wide temperature range, during the life-time of the converter and without the need for manual tuning. The experimental tests on a digitally controlled boost PFC converter demonstrate the feasibility of the proposed algorithm and show that a small input current distortion is achievable with digital control.

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