Modeling and Optimal Design of Shorting Vias to Suppress Radiated Emission in High-Speed Alternating PCB Planes

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Abstract [1] **—An analytical mode analysis of vias in the multi-layered printed-circuit-board periphery is developed to suppress the electromagnetic radiation induced by ground bounce. After separating the even and odd modes in alternating planes, the far-field radiation of parallel plates is derived using Huygens' principle. It is mainly contributed by the odd mode excitation, while the even mode sets a lower bound on the radiation level from the system when shorting vias are inserted between alternating ground plates. For the odd-mode radiation, a canonical problem is then constructed and analytically solved by applying image theory. Based on that, a systematic approach to achieve the optimum suppression design is developed for the various geometry parameters of the shorting vias, including the pitch, radius, and distance to the board edge. Full-wave simulation and measurement are also presented and the good agreement with the theoretical prediction validates the correctness and efficiency of the present analysis and design.**

***Index Terms* — ground bounce noise, electromagnetic interference (EMI), radiation, shorting via, canonical problem, Green's function, mode theory, duality.**

I. Introduction

In the recent decades, continuous advances in semiconductor technology increase data rate and edge rates in high-speed digital systems. Thus, there have always been concerns about the ability of components to operate safely in an increasingly disruptive electromagnetic environment. Electromagnetic emission from other devices will result in some unpredicted effects such as signal-noise fluctuation, even leading to a system crash. A typical example is that interference stripes appear on the screen of some older televisions when a mobile device approaches. Hence, reduction of electro- magnetic emission from integrated circuits [1] to meet the EMI requirement such as the IEC or FCC standard becomes a crucial procedure in whole design

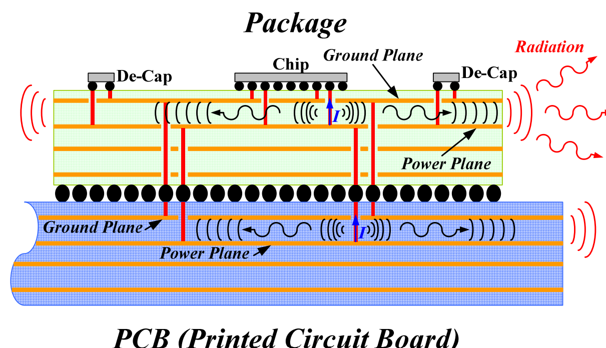

Fig. 1. Fringing radiation from package and PCB due to simultaneous switching current.

flow. On the other hand, the first priority of EMC engineers is to mitigate or block the severe radiated noise before these electronic products enter the markets.

In multilayer printed circuit boards (PCB), ground bounce will be excited when a sudden change of current passes through a through-hole via [2], as shown in Fig. 1. Significant fringing electric fields on the board edges cause radiation to the surrounding space and results in EMI concerns. Considerable efforts have been presented in the literature to mitigate this problem. The spread spectrum clock (SSC) generation [3] is a popular circuit technique spreading the operation frequency of the clock over a narrow band around the clock frequency, thereby avoiding the radiation concentrating at a single frequency. Another circuit technique such as the use of asynchronous circuits [4], with similar mechanism to SSC but in time-domain, shapes the current in order to alleviate the radiated emission from simultaneous switching.

Reducing the package inductance [5] is a commonly employed technique in high-speed digital circuits; the use of absorbent materials [6] has been proposed to reduce the radiated emission; in addition, electromagnetic bandgap structures [7] developed in recent years are also applied to suppress the propagation of ground bounce. However, these techniques call for additional structures and are not common in modern industrial practice. On the contrary, the most popular approach is using decoupling capacitors to suppress not only the ground bounce but also the radiated emission [8], [9], but the applicable range is limited to about 1GHz due to the significant ESR and ESL at higher frequencies.

Connecting the ground planes by shorting vias located on

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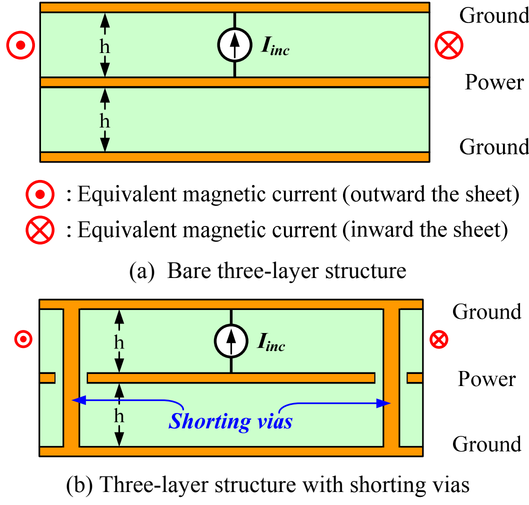


(a) Bare three-layer structure

(b) Three-layer structure with shorting vias

Fig. 2. Three-layer power/ground planes with/without shorting vias.

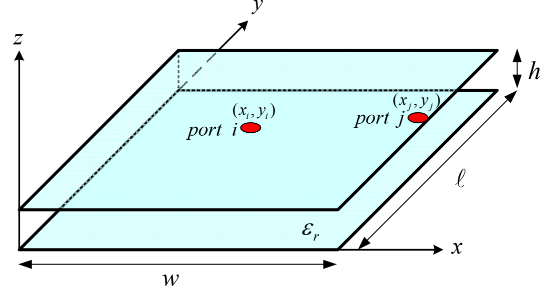
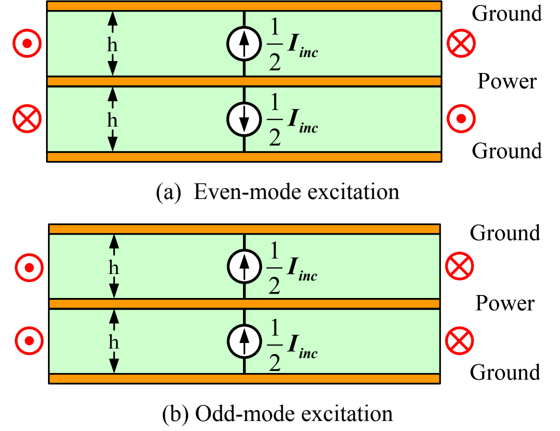


Fig. 3. Rectangular power-ground planes with two ports



(a) Even-mode excitation

(b) Odd-mode excitation

Fig. 4. Three-layer power/ground planes with even- and odd-mode current sources.

different layers was a powerful approach [10] due to low cost and high flexibility. The structures of stacked power/ground planes with vias stitching the reference planes was originally presented to reduce the fringing electric field in [11], but the analysis relies on FDTD and the design was mostly based on case studies. Hence, in this paper, a three-layer structure with ground-power-ground (GPG) stack-up is chosen as an example for a systematic design. This stack-up always exhibits serious ground bounce and radiation. For the purpose of blocking the emission, shorting vias are planted at the periphery and the major goal is to achieve maximum EMI suppression below a certain maximum frequency with the lowest number of vias. Hence, the density of the shorting vias will be chosen in an adaptive way depending on the via radius, thickness between power and ground planes, distance from the center of via to the edge of board, and the frequency of interest. This paper is organized as follows. After a brief statement of problem in Section I, two radiation modes are identified and their excitation and suppression mechanisms are separately investigated. Then, the analytical expressions based on the Huygens' principle [12] and Poynting vector are derived to predict the far-end radiation and dominant mode in bare power/ ground planes in Section II, including a canonical problem and closed-form solution for the multi-layer structure with shorting vias along the periphery. In Section III, a systematic design procedure for the geometric parameters of the vias to achieve the maximum EMI suppression is exemplified. Experimental validation is presented in Section IV and the conclusions are addressed in Section V.

II. Theory and Design of Shorting Vias

A. Statement of the Problem

Consider a current source excitation between the power and ground planes in three-layer GPG stack-up structures without and with shorting vias shown in Figs. 2(a) and (b), respectively. The current source stands for current drawing from the voltage regulator module (VRM) while the logic circuit suddenly changes, and the radiation is generated from the fringing electric field along the periphery. Shorting vias are commonly used to block the radiation since they form a virtual PEC wall if dense enough.

First, in order to estimate the far-field radiation, Fig. 3 shows a pair of close-spaced power-ground planes separated by a dielectric substrate with two source ports, port i and port j; the length, width, height, and dielectric constant are l, w, h, and ε_r, respectively. After the transfer impedance is obtained [13], [14], the fringing electric field is expressed using the transfer impedance as expressed in (1) with a current source I_{inc} fed at port i (assume the port j is at periphery).

$$E_z(x_j, y_j) = \frac{1}{h} V\left(x_j, y_j\right) = \frac{1}{h} Z_{ij} \times I_{inc}(x_i, y_i) \tag{1}$$

Then, the radiated emission of the parallel plates can be attributed to the radiation from the equivalent magnetic surface current $\vec{M}_s = -\hat{n} \times \vec{E}$ due to the fringing electric filed E_z along the board edges.

B. Mode Mechanism in EMI Suppression

By superposition, the GPG stack-up with one source between the 1st layer and 2nd layer as shown in Fig. 2(a) can be decomposed into two structures of even- and odd-mode excitations as depicted in Figs. 4(a) and (b), respectively. Note that the two equivalent magnetic current sources corresponding to the even-mode excitation in Fig. 4(a) are of

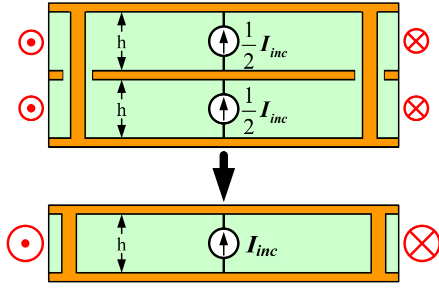


Fig. 5. Simplification for GPG stack-up structure with shorting vias and odd-mode excitation.

opposite polarity, while those for odd- mode excitation in Fig. 4(d) are in phase.

Next, the closed-form expressions from a magnetic source and electric source are dual [15]. Hence, the vector electric potential resulting from the equivalent magnetic surface current $\vec{M}_s$ can be written as

$$\vec{F}(\vec{r}) = \frac{\mu}{4\pi}\int_V \frac{e^{-jk_0|\vec{r}-\vec{r}'|}}{|\vec{r}-\vec{r}'|}\vec{M}_s dv' = \frac{\mu h}{4\pi}\int_C \frac{\vec{M}_s(x',y')\cdot e^{-jk_0 R}}{R} ds' \quad (2)$$

where k_0 is the propagation constant in free space, μ is the permeability, R is the distance from source $\vec{r}' = \hat{x}x' + \hat{y}y'$ to the observation point $\vec{r}$, and the integration is taken over the periphery of the PCB. The radiated field $\vec{E}_{rad}$ and $\vec{H}_{rad}$ of the equivalent magnetic surface current are then described by

$$\vec{E}_{rad} = -\frac{1}{\varepsilon}\nabla\times\vec{F},\ \ \vec{H}_{rad} = -\frac{1}{j\omega\mu}\nabla\times\vec{E}_{rad} \quad (3)$$

Note that the closed-form expression in (2) is of single magnetic surface current. Consider the even- or odd-mode excitation with two cavities. In the far-field, the two sources act as an the antenna array with separation h; hence the vector electric potential can be expressed in single excitation problem with a proper array factor

$$\begin{aligned}\vec{F}(\vec{r}) &= \frac{\mu h}{4\pi}\cdot\int_C \vec{M}_s(x',y')\left[\frac{e^{-jk_0R}}{R} \pm \frac{e^{-jk_0R_{lower}}}{R_{lower}}\right]ds' \\ &\approx \frac{\mu h}{4\pi}\cdot\int_C \vec{M}_s(x',y')\frac{e^{-jk_0R}}{R}ds'\cdot AF\end{aligned} \quad (4)$$

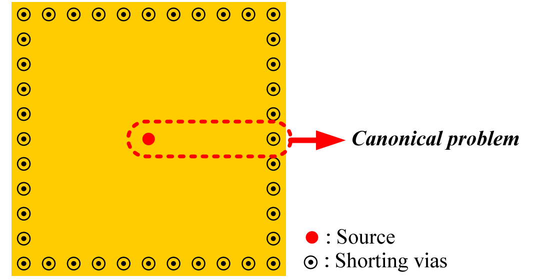
in which

$$R_{lower} \approx R + h\cos\theta$$

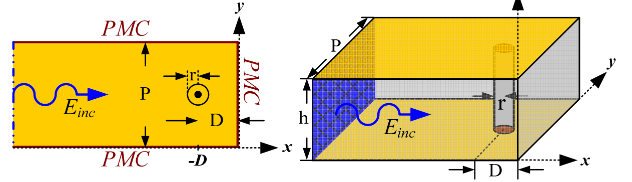
is the distance from the lower cavity to the observation point, θ is the zenith angle of the observation point, and the array factor

$$AF = \begin{cases} jk_0 h\cos\theta, & \text{for even mode} \\ 2, & \text{for odd mode}\end{cases}$$

As a result, the ratio of the even- to odd-mode radiation is given by an attenuation factor:



(a) Top View of GPG stack-up with shorting vias



(b) Top-view (c) Side-view

Fig. 6. Geometric structure of canonical problem.

$$A = \frac{|E_{\text{rad, even}}|}{|E_{\text{rad, odd}}|} = A_{\text{ideal}}\cos\theta;\quad A_{\text{ideal}} = \tfrac{1}{2}k_0 h \quad (5)$$

Without the shorting vias, the radiation due to the odd-mode excitation is similar to that in the original problem Fig. 1(a), while the even-mode radiation is much smaller. With shorting vias to connect the upper and lower planes, the even-mode excitation in Fig. 4(a) is hardly affected because the electric potential between 2nd-to-1st layer and 2nd-to-3rd layer are identical under even-mode excitation, *i.e.*, there is an infinite amount of virtual shorting vias between the 1st layer and the 3rd layer. However, provided that the shorting vias are sufficiently closely spaced, the fringing electric field on the board edges due to the odd-mode excitation in Fig. 4(b) is strongly reduced and the even-mode radiation becomes the dominant term. Hence, A_{ideal} in (5) becomes a good approximate to the theoretical limit of the EMI suppression by the present technique of stacked planes with vias stitching. For example, if an EMI suppression of 20dB from dc up to 3GHz is desired, one can easily choose layer height h < 3.1mm so that A < 0.1 for all θ.

Finally, the total radiated power can be obtained by the integral over a spherical surface in the far field

$$P_{\text{total}} = \oint_S \vec{P}_{\text{avg}}\cdot d\vec{s} \quad (6)$$

where the Poynting vector

$$\vec{P}_{\text{avg}} = \frac{1}{2}\text{Re}\left[\vec{P}\right] = \frac{1}{2}\text{Re}\left[\vec{E}_{\text{rad}}\times\vec{H}^{*}_{\text{rad}}\right]$$

C. Canonical Problem

The above reasoning relies on neglecting the odd-mode radiation, which can be justified only if the vias are spaced densely enough so that the fringing electric field on the board edge is very small. More vias can yield better shielding but imply larger manufacturing costs and less freedom for the routing near the board edges. An optimal design of the vias is that the electric field on the board edges can be reduced by an attenuation factor given by (5), thereby assuring that the odd-mode radiation remains smaller than that of the even-mode excitation.

Consider a three-layer GPG stack-up structure with shorting vias near the periphery as depicted in Fig. 2(b), but the excitation is the odd-mode one. The power plane is virtually connected to the shorting via since the potential between power/ground planes must be zero at the center of the shorting via to fit the odd- mode excitation. Consequently, the problem can be simplified to a two-layer structure with shorting vias as depicted in Fig. 5.

The major design parameters are the pitch P between two adjacent vias, distance D from via center to board edge, and via radius r. Without loss of generality for the design of these parameters, consider a rectangular two-layer structure with shorting vias at all the four sides as shown in Fig. 6(a). Furthermore, provided that the size of the plane is large as compared with a wavelength, the field distribution in the region near the vias and board edge can be approximated as the canonical problem shown in Fig. 6(b). It is a wave scattering problem in a waveguide with two perfectly magnetic conductors (PMC) as the side walls while the bottom and upper walls are metal planes as shown in Fig. 6(c).

D. Closed-form Solution

To solve the problem, first consider an incident field E_{inc} impinging from the left side of Fig. 6(c). It will induce a current I_{via} on the shorting via, such that the resultant electric field along the via surface is zero. To determine the electric field due to the induced current, the canonical problem can be extended into infinite space by image theory as depicted in Fig. 7. Here, the board edge is chosen at $x = 0$ and assumed to be a PML, while the two PML walls of the waveguide are located at $y = 0$ and P. In infinite space, there are two infinite arrays of image shorting vias and induced currents, which are in phase to satisfy the PMC boundary conditions, *i.e.*, $I_{via} = I'_{via}$.

The wave propagating outward from a cylindrical via can be written as [15]:

$$E_z^+ = -j\omega\mu I_{via} \cdot \frac{1}{4j} H_0^{(2)}(k\rho) \qquad (7)$$

where $H_0^{(2)}$ is the Hankel function of the second kind of zeroth order, k is the propagation constant in the material, and ρ is the distance from the center of the via to the observation point (x, y). Since the shorting via is placed at $(x', y') = (-D, \frac{P}{2})$, the electric field due to the two current arrays can be expressed by

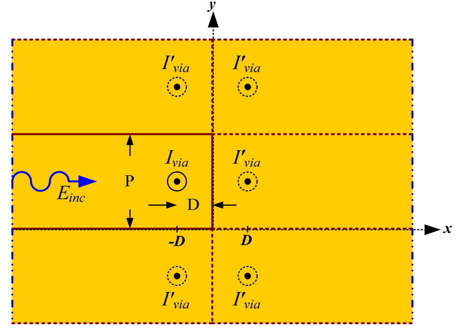


Fig. 7. Infinite current array by image theory

$$E_z^s(x,y) = -j\omega\mu I_{via} \cdot \left[g(x+D, y) + g(x-D, y) \right] \qquad (8)$$

where the Green's function is

$$g(X,y) = \sum_{n=-\infty}^{\infty} \frac{1}{4j} \left[H_0^{(2)}\left(k\sqrt{X^2 + (y - \tfrac{P}{2} - nP)^2} \right) \right]; \qquad (9)$$

Next, the incident field E_{inc} is taken into consideration to derive the total electric field on the board edge. In Fig. 7, the total electric field involves two directions of incident field E_{inc}, toward positive and negative x-axes, contributed from the true and image fields, and can be written by

$$\begin{aligned} E_z^{tot}(x,y) &= E_{inc}e^{-jkx} + E_{inc}e^{jkx} + E_z^s(x,y) \\ &= 2E_{inc}\cos kx - j\omega\mu I_{via} \cdot \left[g(x+D,y) + g(x-D,y) \right] \end{aligned} \qquad (10)$$

Since the total electric field in (10) should be zero at the via boundary, say $x = -(D-r)$ and $y = P/2$, I_{via} can be solved as

$$I_{via} = \frac{2\cos(kD - kr)}{j\omega\mu \cdot \left[g(r, \frac{P}{2}) + g(2D - r, \frac{P}{2}) \right]} \cdot E_{inc} \qquad (11)$$

The above derivation is only valid under the assumption that the via radius is small compared to D and P as is the case in any practical situation.

With the thus solved I_{via}, the total electric field is obtained by substituting (11) into (10), which is independent on the board thickness h. From (10), it can be found that the maximum and minimum electric field on the board edge are at $y = 0$ (or $y = P$) and $y = 0.5P$, respectively, if D is smaller than a wavelength in the material. The results are physically reasonable since the via fence can prevent the propagating wave from reaching the board edge; hence, the point directly behind the shorting via can be protected well and the point between adjacent vias has the worst protection. The odd-mode suppression factor can be defined as the ratio between the maximal edge electric field and E_{inc}, *i.e.*,

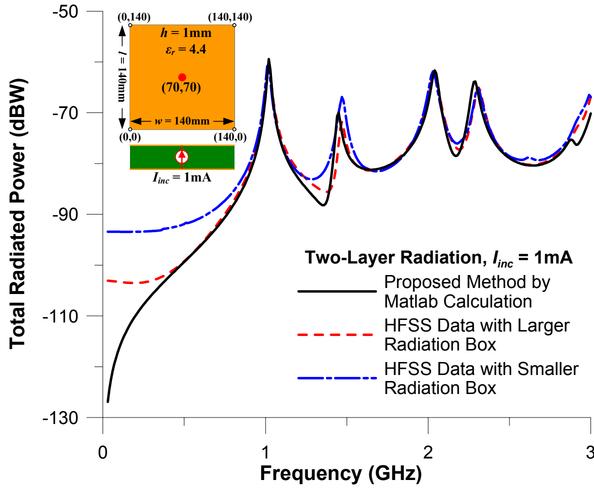


Fig. 8. Comparison between proposed approach and simulation results for the total radiated power of power/ground planes

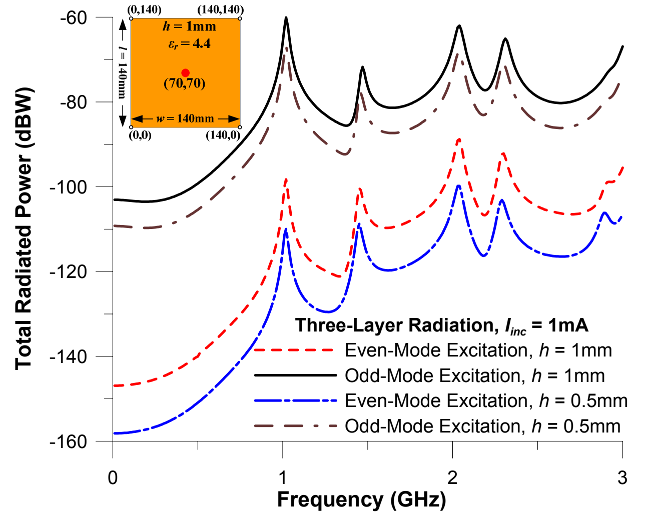


Fig. 9. Comparison of different thicknesses for the three-layer structure

$$A_{\rm odd} \equiv \frac{E_{z,\max}^{total}(0,y)}{E_{inc}} = \frac{E_{z}^{total}(0,0)}{E_{inc}}$$
$$= 2 - 2\cos(kD - kr)\cdot\left(\frac{2g(D,0)}{g(r,\frac{P}{2}) + g(2D - r,\frac{P}{2})}\right) \qquad (12)$$

It is worth noting that the infinite series in (9) is very slowly convergent. For numerical computation, the summation can be significantly facilitated by employing the Poisson summation formula [16], *i.e.*,

$$g(X,y) = \frac{e^{-jk|X|}}{2jkP} + \sum_{m=1}^{\infty}\frac{(-1)^m e^{-k_m|X|}}{k_m P}\cos\left(\frac{2m\pi y}{P}\right) \qquad (13)$$

in which

$$k_m = \sqrt{\left(\frac{2m\pi}{P}\right)^2 - k^2}$$

In practical cases, r is always much smaller than the two other major parameters D and P. The odd-mode suppression factor may be larger than 1 when kD is close to 0.5π. From the view of wave propagation, the field in the concerned region becomes complicated while D is larger than one eighth wavelength. It implies the effect of suppression will be worse at higher frequency. Fortunately, present PCB manufacturing allows a minimal value of D = 0.46mm (~18mil), so the effective frequency is as high as to 40GHz.

E. Shorting Vias Design Procedure

With the use of the above presented canonical structure simplified from the conventional GPG stack-up, analytical results in terms of the relevant parameters r, D, P, f, ε_r, have been presented. Given the desired specification of the EMI suppression in the frequency range of interest, the following design procedure is suggested:

1) Estimate the maximum thickness h by $A_{\rm ideal}$ from (5) to ensure sufficient suppression.
2) Determine the distance D from board to shorting via.
3) Determine the via radius r.
4) Compute the via pitch P by $A_{\rm odd}$ in (12) or use the design chart presented later.

III. Design Examples and Numerical Results

A. Computations of Total Radiated Power

Consider a pair of rectangular power-ground planes with length l = 140mm, width w = 140mm, thickness h = 1mm, and dielectric constant ε_r = 4.4 with a loss tangent of 0.02 and a conductivity of 5.8×10^7S/m as shown in the inset of Fig. 8. The location of the current excitation I_{inc} on the board is at (70mm, 70mm). Figure 8 shows the results for the total radiated power and for a single excitation I_{inc}= 1mA, calculated by (6) in a Matlab program using the theory presented in part B of Section II and the full-wave software tool HFSS [17]. Both are consistent at higher frequencies.

HFSS's results will be more accurate if a larger radiation box is employed. However, the larger radiation box implies longer computation time and the result given by the red-dashed line in Fig. 8 utilizing a 6m × 6m × 4m box consumes almost 1 day using an Intel Core 2 (2.4 GHz) CPU with 8G RAM. On the contrary, the proposed approach can obtain the black line in Fig. 8 in minutes, and its results are more reliable at low frequencies.

Note that the peaks of total radiated power appear at cavity resonances, which are -59.4dBW at TM_{20}, -70dBW at TM_{22}, -61.7dbW at TM_{40}, and -63.9dbW at TM_{42} respectively, since the fields are relatively strong at the board edge when resonating. The resonance frequency can be obtained by (14)

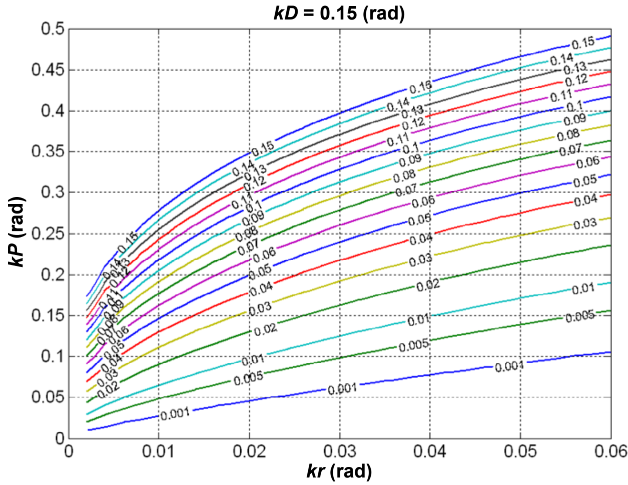


Fig. 10. Design chart of A_{odd} versus kP and kr based on $kD = 0.15$ in the canonical problem

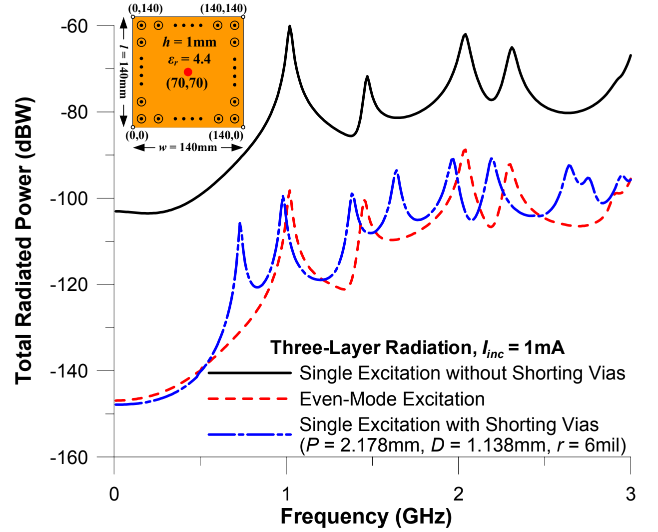


Fig. 11. Total radiated power for the three-layer structure with shorting vias for a 20dBW suppression design

$$\left(f_{res}\right)_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{l}\right)^2 + \left(\frac{n\pi}{w}\right)^2} \qquad (14)$$

where m and n are integers.

To discuss the effect of thickness, GPG structures with even- and odd-mode excitations based on different layer thicknesses of 1 mm and 0.5 mm are employed in Fig. 9 and simulated by HFSS. The other parameters are identical with those in Fig. 8 and the polarizations of the two modes are described in Fig. 4. The total radiated power for single excitation in the two-layer structure and odd-mode excitation in the three-layer structure are almost the same since the contribution of the even-mode field is much smaller.

Although not accurate at low frequencies, HFSS's results validate the theoretical predictions. From (2) it follows that half the board thickness leads to a 6dB reduction for odd-mode and single excitation because the far-field is proportional to the thickness of board. Moreover, the attenuation factor in (5) gives the difference between even- and odd-mode radiated powers, *e.g.*, about $0.5k_0h = 0.031$, or 30dB, for the case h = 1mm at 3 GHz.

B. Optimal Design for Shorting Vias

From the discussion in Section II, r, D, and P are the major design parameters in (12), hence one of the minor parameters, f, is set at the highest system frequency chosen to be 3 GHz. From the manufacturing and cost prospective, D is chosen as small as possible to minimize the amount of shorting vias. Then, for the convenience of design, the suppression ratio A_{odd} in (12) versus kP and kr under fixed kD is plotted as a design chart. Fig. 10 shows the result when $kD = 0.15$ (where $\varepsilon_r = 4.4$ and $D = 1.138$mm) is employed, with A_{odd} ranging from 0.001 to 0.15. For example, consider a design aiming at an EMI suppression by 20dB from dc up to 3GHz for the three-layer structure in Fig. 2(b). This requires $A_{\mathrm{odd}} = 0.1$, *i.e.*, 20dB. A possible choice is $kP = 0.287$ and $kr = 0.02$ at the highest frequency from the design chart, or $P = 2.178$mm and $r = 6$mil.

Fig. 11 shows the total radiated power from 0 to 3GHz calculated by HFSS. It can be seen that the total radiated power is suppressed in general by 20dB or more as compared with the structure without shorting vias, and yielding a still larger suppression for lower frequencies. By adding dense vias near the board periphery, the boundary of the cavity changes from open to nearly PEC for the odd-mode. If D = 1.138mm, and r = 6mil are left unchanged, the minimum via pitch in common PCB manufacturing is 0.56mm (~22mil). According to Fig. 10, almost 46dB ($A_{\mathrm{odd}} = 0.005$) suppression can be achieved with this minimum via pitch. However, it will be an over design since the maximum suppression is limited by the even-mode attenuation factor A_{ideal}, which is 30dB for h = 1mm or 36dB for h = 0.5mm at 3GHz.

IV. Experimental Validation

Three-layer GPG stack-up structures with/without shorting vias were fabricated to investigate the total radiated power from a centre-feeding structure with length l = 140mm, width w = 140mm, thickness h = 1mm, and dielectric constant ε_r = 4.4 with loss tangent of 0.02. The parameters for the shorting vias are the same as in Fig. 11. Note that the total radiated power is measured by the GTEM Cell (GTEM 500) method and using a spectrum analyzer (R&S FSP 9kHz-40GHz). The signal is generated using the function generator (SG-hp83650B 10MHz-50GHz) with input power P_{in} = 1mW. In order to be consistent with the simulation, the measured power P_{meas} should be transferred to that of a given current source I_{inc} by

$$P_{I_{inc}} = P_{meas} \times \frac{\left|Z_0 + Z_{11}\right|^2}{8Z_0} \cdot \frac{\left|I_{inc}\right|^2}{P_{in}} \qquad (15)$$

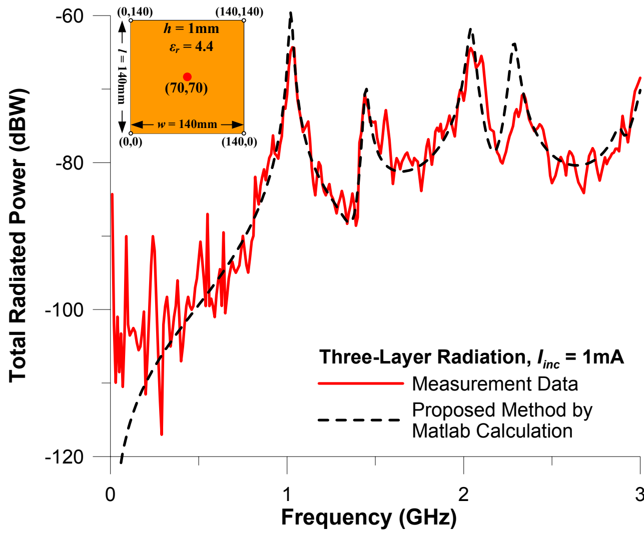


Fig. 12. Comparison between simulation and measurement for a bare three-layer board

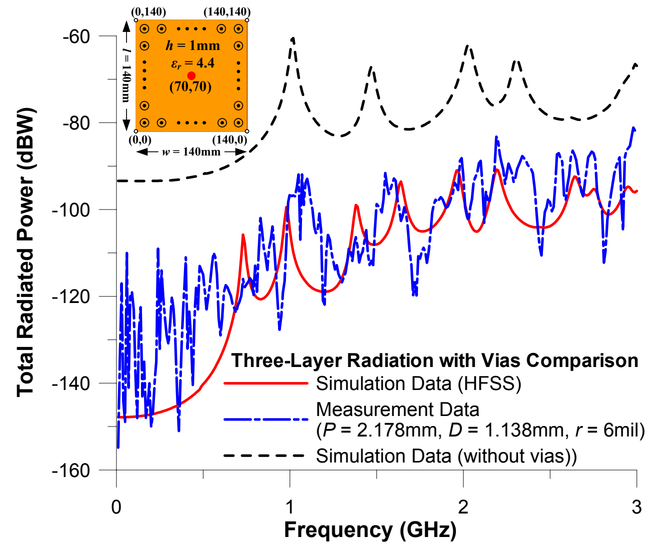


Fig. 13. Comparison between simulation and measurement for a three-layer board with shorting vias

where Z_0 = 50 Ω, is the system impedance, Z_{11} is the input impedance at the feeding port obtained from the simulation, and P_{Iinc} is the total radiated power due to I_{inc}.

Bare board measurement data and the simulated results by the proposed approach are compared in Fig. 12. The low frequency data from the GTEM exhibits large ripples due to measurement errors, but the mid frequencies up to 3GHz show good agreement with the proposed approach. Also, it can be seen that the maximum EMI level in the measurements and calculated by the proposed approach are -64.3dBW and -59.4dBW respectively at the first resonance of 1.02GHz.

By adding shorting vias near the periphery, the measured total radiated power is now depicted in Fig. 13. Compared with HFSS's results with vias, measured data shows good correlation both with respect to the numerical values and with respect to the resonance frequencies. In addition, 20dBW suppression is noticeably achieved from DC to 3GHz.

V. Conclusions

The radiated emission due to ground bounce in a multi-layer PCB causes EMI concerns and can be reduced by using stacked ground planes with via stitching. The radiation mechanism can be decomposed into even- and odd-mode parts. From the analytic form of the radiated far field, the radiation due to the even-mode excitation is much smaller than that of the odd-mode excitation and sets a reference level for the minimal radiation power of the system. The odd-mode radiation can be minimized by placing dense enough vias to reduce the fringing electric field on the PCB edges. In this way, the EMI due to the ground bounce in multi-layer PCB can be substantially suppressed.

A canonical problem which is simplified from the original shorting vias structure is constructed and then solved analytically. A systematic procedure is established for the placement design of shorting vias. Based on this, a design example to achieve 20dB EMI suppression from dc up to 3GHz is discussed in detail and validated by both full-wave simulations and by measurements.

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References

[1] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J. J. Whalen, T. H. Hubing, M. Coenen, and O. Wada, "The electromagnetic compatibility of integrated circuits - past, present, and future," *IEEE Trans. Electromagn. Compat*, vol. 51, pp. 78-100, Feb. 2009.

[2] J. Fang, Y. Liu, Y. Chen, Z. Wu, and A. Agrawal, "Modeling of power/ground plane noise in high-speed digital electronics packaging," in *Proc. IEEE 2nd Topical Meeting Elect. Perform. Electro. Packag.,* Monterey, CA, Oct. 20-22, 1993, pp. 206-208.

[3] K. B. Hardin, J. T. Fessler, and D. R. Bush, "Spread spectrum clock generation for the reduction of radiated emissions," *Proc. IEEE Int. Symp. Electromagn. Compat.*, Chicago, IL, Aug. 22-26, 1994, pp. 227-231.

[4] D. Panyasak, G. Sicard, and M. Renaudin, "A current shaping methodology for lowering EM disturbances in asynchronous circuits," *Microelectron. J.*, vol. 35, pp. 531-540, Jan. 2004.

[5] T. Sudo, "Behavior of switching noise and electromagnetic radiation in relation to package properties and on-chip decoupling capacitance," *Proc. 17th Int. Zurich Symp. Electromagn. Compat.*, Singapore, Feb. 27-Mar. 3, 2006, pp. 568-573.

[6] S.-H. Kim, S.-B. Lee, K.-I. Ouh, C.-B. Rim, K.-S. Moon, H.-G. Yoon, and T.-J. Moon, "Reduction of radiated emissions from

semiconductor by using absorbent materials," *Proc. IEEE Int. Symp. Electromagn. Compat.*, Washington, DC, Aug. 21-25, 2000, pp. 153-156.

[7] T.-L. Wu, Y.-H. Lin, T.-K Wang, C.-C. Wang, and S.-T. Chen, "Electromagnetic bandgap power/ground planes for wideband suppression of ground bounce noise and radiated emission in high-speed circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 2935-2941, Sept. 2005.

[8] J. Kim, H. Kim, W. Ryu, and J. Kim, "Effects of on-chip and off-chip decoupling capacitors on electromagnetic radiated emission," *Proc. Electron. Comp. Technol. Conf.*, Seattle, WA, May 25-28, 1998, pp. 610-616.

[9] L. van Wershoven, "Characterization of an EMC test-chip," *Proc. IEEE Int. Symp. Electromagn. Compat*., Washington, DC, Aug. 21-25, 2000, pp. 117-121.

[10] K.-B. Wu, F.-S. Chang, and R.-B. Wu, "Design of shorting vias in alternative PCB planes for suppressing ground- bounce induced electromagnetic emission," in *Proc. IEEE 18th Topical Meeting Elect. Perform. Electro. Packag.,* Tigard, OR, Oct. 19-21, 2009, pp. 247-250.

[11] X. Ye, D. M. Hockanson, M. Li, Y. Ren, W. Cui, J. L. Drewniak, and R. E. DuBroff, "EMI mitigation with multilayer power-bus stacks and via stitching of reference planes," *IEEE Trans. Electromagn. Compat.*, vol. 43, pp. 538-548, Nov. 2001.

[12] C. A. Balanis, *Antenna Theory – Analysis and Design*, 2nd ed., John Wiley & Sons, Inc.,1997. ch.14.

[13] T. Fischer, M. Leone, and M. Albach, "An analytical model for studying the electromagnetic radiation of power-bus structures," *Proc. IEEE EMC Symp.*, Boston, MA, Aug. 18-22, 2003, pp. 225-230.

[14] K.-B. Wu, G.-H. Shiue, W.-D. Guo, C. M. Lin, and R.-B. Wu, "Delaunay-Voronoi modeling of power-ground planes with source port correction for chip package co-Simulation," *IEEE Trans. Adv. Packag.,* vol. 31, no. 2, pp. 303-310, May 2008.

[15] R. F. Harrington, *Time-Harmonic Electromagnetic Fields*, A Classic Reissue, John Wiley & Sons, Inc., 2001, ch. 5.

[16] R. E. Collins, *Field Theory of Guided Waves*, 2nd ed., IEEE Press, 1991, chs. 4 and 7.

[17] HFSS, *High Frequency Structure Simulator*, Ver. 11.1, Ansoft Corporation (www.ansoft.com).