Technology development for a low-cost, roll-to-roll chip embedding solution based on PET foils

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Abstract

The aim of the research described in this paper is to develop a low-cost, roll-to-roll compatible process for the realization of electronic systems in foil using chip embedding. The small cost makes these systems suitable for disposable applications as food labels, medicine packages or smart bandages. Surface mount attaching of components on foils is a well-known process for building systems-in-foil. When using low-cost films like PEN and PET, there are serious restrictions on the maximum temperatures that can be used for the surface mounting process (soldering, adhesive bonding). Surface mounting has the additional disadvantage that the components are on the surface of the foil and are therefore not well protected mechanically and physically. The proposed process flow for embedding thin chips in PET foils overcomes these limitations. A key aspect of this technology is the application of a suitable adhesive to encapsulate the chips. The resulting product is based on full-metal copper which has a good thermal and electrical conductivity and allows for fine pitches. The process is compatible with several metal foils (Cu, Al …), offering further possibilities in cost reduction, and does not rely on bumping of the chips or plating of the interconnections to the chips.

Key words: chip embedding, low-cost, roll-to-roll, PET

Introduction

Chip embedding is in essence a three-dimensional packaging technology that offers an alternative to wire bonding and flip-chip interconnects. Nowadays, two different categories of chip embedding technologies are commercially available. Fan-out wafer level packaging (WLP) enlarges the area available for interconnect routing on top of the die by embedding the chip in a polymer matrix [1], [2]. More system level approaches, such as the direct embedding of chips into the printed circuit boards (PCB), result in a System-in-Package concept [3], [4].

Flexible electronic products are mostly realized on polyimide with copper tracks and traditional pad finishes (NiAu, Ag, Sn…) because of the compatibility with “normal” assembly technology as e.g. soldering. The resulting flex foils are often stacked or folded to form three-dimensional constructions. These technologies and applications are still based on established printed circuit board (rigid and flex) processing. While the thickness of the dies embedded in rigid boards is usually around 100 um to 200 um, the embedding of active components inside a flexible circuit board relies on chips thinned down to 30 um and below. The ultra-thin chip package (UTCP) [5] is such a technology, where the chips are embedded in polyimide foils. The resulting package is only 60 µm thick. The chips are placed face-up on a polyimide layer and covered with a spin-on, photo definable polyimide. Vias to the chip contacts are realized using photo lithography and metallized by sputtering and galvanic plating. The embedded die can be used as a package, e.g. solder balls can be placed on the contacts and the package can be solder assembled on interconnection substrates, or further embedded between the layers of a flexible circuit board [6].

Apart from this polyimide-based flex technology, there are also developments on low-cost substrate materials. A very important application in this area is RFID and smart card technology. The chips used here are typically around 100 µm thick, have a small number of I/Os (2 – 8) and a large pitch (> 0.2 mm). They are connected using wire bonding or flip-chip to printed or plated conductors. The Holst Centre in Eindhoven focuses mainly on these low-cost substrates, where the use of polyester-based materials imposes additional challenges as the temperature budget for the interconnection process is limited. Current research topics include the assembly of packaged chips and bare dies on PET or PEN films with silver or copper interconnections (Figure 1), low-cost interconnections for OLEDs and the embedding of chips in PET foil, which is discussed in this paper.

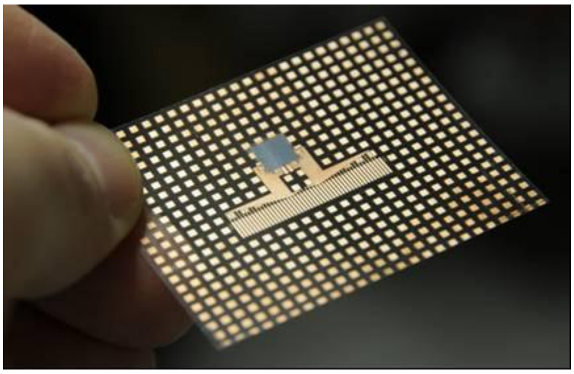

Figure 1: Thin die assembled on Cu/PET foil

The most quoted advantages of chip embedding include the reduced interconnection length and freeing up board space. Due to the limited frequency range employed on polyester-based substrates and the low material cost, these topics are less of a concern for Systems-in-Foil. The possibility of thin and flat systems with improved reliability thanks to the better mechanical and physical protection of the die, as opposed to surface mounting where the die protrudes from the foil, are much more of a driving force for chip embedding in foil.

The aim of this research is not just to develop a chip embedding process based on PET films, but to realize a roll-to-roll compatible process with maximum cost reduction. Using low-cost material is a first step towards lower cost, but combining these materials with expensive processing steps is counterproductive. Thin-film processing and chemical or galvanic deposition should be avoided. If possible, bumping of the chips will be avoided, although the cost for bumping is small compared to the chip cost.

The process flow for chip embedding in PET foil is described in the next section, followed by a detailed overview of possible adhesives for encapsulating the chips. After a short discussion on chip assembly, this paper concludes with some cost considerations.

Process Flow

To avoid thermo-mechanical restrictions during die placement, the process starts from a single copper foil. The first step of this embedding technology is the application of the die bonding adhesive. One option is screen printing of isotropic conductive adhesive bumps and dispensing of non-conductive adhesive in between the bumps. Uniformity of the bump height and the minimal attainable pitch are important parameters of the printing process. During placement of the thinned chips, the pads on the chip are aligned to the bumps on the foil, realizing the interconnection between the copper foil and the chip pads without the need for bumping the chip. As a backup solution for ultrafine-pitch applications, an anisotropic conductive adhesive could be used in combination with bumps on the chips. The actual embedding of the chips is performed in a lamination step using PET film and a suitable adhesive[1]. Void-free lamination, ensuring a good encapsulation of the chips, is a crucial step in the chip embedding process. In a final step, the copper is structured using conventional PCB processes or alternative patterning technologies to define the circuitry. The end result is a thin foil with embedded components and copper interconnects. Figure 2 shows a schematic overview of the process flow. Typical dimensions are a chip thickness of 30 µm, a 20 µm die bond adhesive layer, and a 50 µm thick PET film. The adhesive surrounding the chips will be about 70 µm to 100 µm in total, resulting in an overall thickness of less than 200 µm. For increased mechanical reliability, an additional cover layer can be laminated onto the copper side after structuring, moving the circuit closer to the neutral axis.

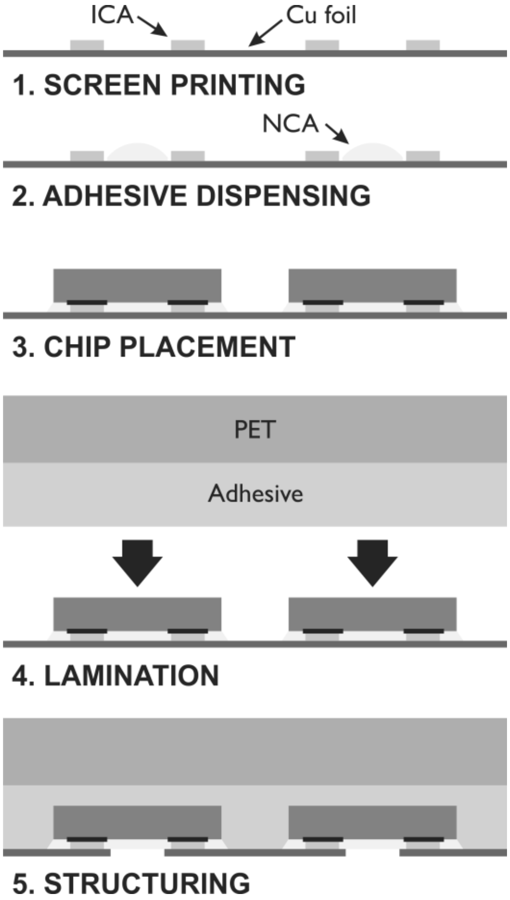

Figure 2: Process flow for chip embedding in PET foil

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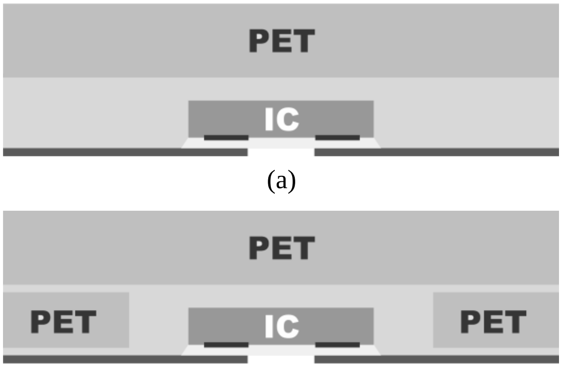
[1] Unless explicitly mentioned otherwise, the word “adhesive” in the following always refers to the adhesive used to encapsulate the chips.



(a)

(b)

Figure 3: (a) Embedding using thick adhesive (b) Cavity-based embedding

The use of a full-metal foil not only provides better thermal and electrical conductivity, but also allows for finer pitches than an additive printing process. Surface mount assembly on PET or PEN is severely restricted by the maximum temperatures that can be tolerated by the materials. Die placement on a full-metal foil does not suffer from these restrictions, enlarging the selection of possible die bond adhesives. The process flow is compatible with other metals, as for example lower-priced aluminum, and other polymer substrates (PEN, PI, PUR …). A disadvantage for mass manufacturing is that just like in conventional surface mount technology each component needs to be placed and interconnected individually.

The adhesive used to encapsulate the chips is a critical aspect of the technology. Due to the combination with PET film, the processing temperature is limited to a maximum of 120 °C for a few minutes. The need for good adhesion to copper and PET is evident, whereas a good flow behavior is vital to successfully enclose the chips. Since the adhesive cost is a dominant factor in the overall material cost, primarily general-purpose industrial adhesives are considered. A this point in the process development, no additional specifications (thermal conductivity, ionic content, moisture permeation) requiring a higher grade adhesive are encountered. The resulting gamut of possible candidates is very broad, ranging from pressure sensitive tapes, over thermoplastic or thermosetting film adhesives, to UV curing liquid adhesives.

Depending on the available thickness and the cost of the adhesive, two options for embedding the chips in between the copper foil and the PET film are presented. The first possibility relies on the use of a thick adhesive layer, which is simply pressed onto the chips mounted on the copper foil (Figure 3a). The advantage of this approach is that the process is simple and straightforward. Since a thick layer of adhesive is needed to cover the height difference of 50 µm formed by the chip and the die bond adhesive layer, the bulk material cost of the adhesive needs to be very low. The alternative is to use thin layers of adhesive coated onto PET film and create cavities at the intended locations of the chips (Figure 3b). A second coated PET film is laid on top of the first and during lamination both adhesive layers flow together to fill the cavity. While this approach saves on adhesive cost, or allows for the use of a more robust adhesive at the same price, the process flow is more complex and a certain alignment is needed during layup or lamination. A third option, where only an adhesive layer without additional PET film is used to embed the chips, imposes additional requirements on the adhesive, as for example all the mechanical strength needs to be carried by the adhesive. The top PET film in option one or two can also contain certain functionality, resulting in a higher integration density for more complex Systems-in-Foil.

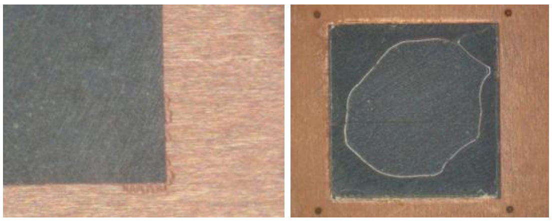
Material Evaluation

Since the preferred class for a suitable adhesive for chip embedding is general-purpose, industrial adhesives, instead of adhesives tailored for electronic applications, and no detailed set of specifications is available, the possible candidates are numerous. The chosen approach is to evaluate different types of adhesives based on processability, cost, performance and reliability.

Due to the restrictions in processing temperature, pressure sensitive double-sided tapes are a logical choice. A void-free encapsulation of the chips with these tapes requires a thick adhesive layer which is sufficiently soft to “flow” around the chips. A drawback of this type of adhesive is that it remains sticky, which might be an issues for the areas that are exposed after copper structuring.

The ideal adhesive for this technology would be a film adhesive which becomes liquid at a temperature below 80 °C, flows around the chips and subsequently solidifies. This could be either a thermoplastic or thermosetting polymer, although the latter would accommodate a low processing temperature without restricting the operational temperature of the circuitry. Alternatively, a liquid adhesive can be coated over the chips and cured during or after lamination of the PET film.

A total of seven different adhesives are evaluated: two pressure sensitive tapes with different softness (“PSA 1” and “PSA 2”), two thermoplastic



(a) (b)

Figure 4: (a) Air bubbles entrapped between the edge of the chip and the pressure sensitive tape; (b) Insufficient filling of cavity using thermo-plastic adhesive

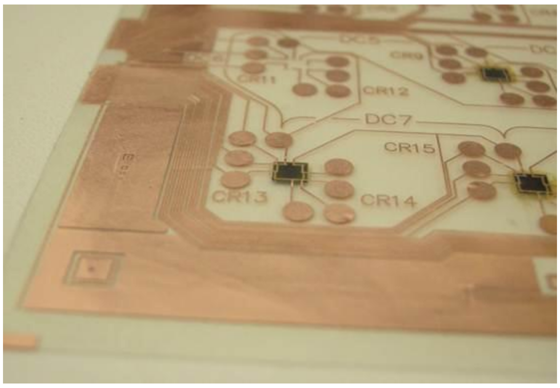


Figure 5: Chip embedding test vehicle (PSA 1)

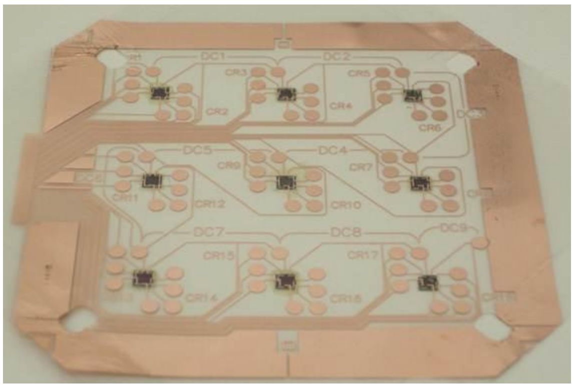


Figure 6: Chip embedding test vehicle (TP 1)

adhesives coated onto PET film (“TP 1” and “TP 2”), two heat-activated film adhesive with and without non-woven carrier (“HA 1” and “HA 2”) and finally, a liquid adhesive that becomes pressure sensitive after UV exposure (“UV 1”). The processability and performance of these adhesives is evaluated by embedding dummy chips mounted onto copper foil. While roll lamination would be the method of choice for a roll-to-roll compatible process, all material evaluation experiments are performed using sheet lamination in a vacuum lamination press (*Lauffer RLKV 25*).

PSA 1 and the softer PSA 2 are double-sided tapes with an adhesive thickness of 130 µm, necessitating a two-step lamination process. In the first step, the tape is laminated to the PET film using a pressure of 1 bar at 40 °C for 5 minutes. After removing the second release liner, the PET + adhesive is laminated onto the copper foil with assembled chips. For this second lamination a slightly higher pressure (5 bar) and longer dwell time (10 min) are applied to assure a good encapsulation of the chips. As is the case for all film adhesives, the sheet lamination makes it difficult to avoid entrapped air. Contrary to the expectations, the use of the softer PSA 2 leads to more air bubbles, both around the chips as across the foil (Figure 4a). Cracking of the chips did occur when areas underneath the chip were not completely filled by the die bond adhesive, predominantly at the corners of the chips. Further optimization of the die bonding process will mitigate this issue. Structuring the copper reveals that the stickiness of the exposed area of the adhesive is noticeable, but not critical.

The heat-activated adhesives HA 1 and HA 2 follow a similar process flow, although the first lamination step is replaced by a manual application of the adhesive to the PET film using a hand roller. The thickness of the baseless HA 1 is only 50 µm, so two layers of adhesive are sequentially laminated to the PET film. HA 2 contains a non-woven cellulose carrier and has a total thickness of 90 µm. These adhesives show a reasonable amount of flow, but are designed to start curing in seconds when reaching temperatures above 100 °C, giving the adhesive insufficient time to flow around the chips. A higher pressure and a slightly reduced temperature result in a void-free embedding without too much increase in processing time.

The low coating thickness of the thermoplastic adhesives TP 1 and TP 2 (25 µm and 14 µm, respectively) requires the use of cavities to overcome the height difference between the assembled chips and the copper foil. This complicates the process, since additional steps need to be introduced to cut out the cavities and to assure a good alignment of the cavities to the chips. The cutting of the adhesives coated on 50 µm PET film is done using a CO_2 laser (10.6 µm). On each side, the cavities are 100 µm larger than the chips and the parameters of the laser are optimized to obtain a well-defined cavity edge without affecting the flow behavior of the adhesive. The latter is very important for a successful embedding (Figure 4b). During the first trials, the fillet caused by the die bond adhesive at the edge of the chip appeared to be wider than 100 µm. As a result, the cavities would not fit around the chip and needed to be enlarged. With a margin of 200 µm and a better control of the die bonding process, a sufficient filling of the cavities was obtained. A dwell time of 20 minutes at 120 °C was needed to obtain these results, making the process not only more complex but also very slow. Due to the lengthy exposure of the PET film to elevated temperatures, a noticeable shrinkage occurred, resulting in severe warpage of the samples. The advantage of the thermoplastic materials is that insufficient filling of the cavities can be fixed by again heating the adhesive to above its melting point.

The last material under evaluation is a liquid, UV sensitive adhesive, which is applied over the chips by doctor blading. Care needs to be taken to allow sufficient spacing between the blade and the top of the chips. After applying the adhesive, the samples are exposed to a UV dose of 2 mJ/cm^2 and become tacky. A PET film is laminated on top using a pressure of 5 bar at room temperature for 5 minutes. First tests revealed that when the adhesive layer is too thin (100 µm or less), the UV-initiated

Table 1: Summary of material evaluation results

Mat.	Proc.	Cost	R2R	Perf.
PSA 1	+	++	++	+
PSA 2	+	++	++	+
HA 1	+	+	++	+
HA 2	++	+	++	+
TP 1	--	+	-	++
TP 2	--	+	-	++
UV 1	-	-	+	+

reaction does not continue to completion, resulting in insufficient adhesion to the PET film. Again, the exposed areas of the adhesive after structuring remain sticky.

Each of these adhesive types has its own advantages and drawbacks, making it difficult to identify a clear winner at this point. A single-sheet film adhesive with a one or two-step lamination would offer the best compromise between processability, cost and performance. Table 1 gives a summary of the behavior of the adhesives, evaluated in different categories: processability, including handling and complexity of the process flow, material cost, roll-to-roll compatibility of the process, and embedding performance. No lifetime or mechanical testing has been performed, so the reliability of these materials cannot be evaluated at this point.

Overall, the pressure sensitive tapes and the heat-activated films score the best. The embedding performance of the thermoplastic adhesives is very good, but the slow and complex process makes these materials less appropriate. The liquid adhesive does not have a clear advantage over the film adhesives due to the thickness requirements for this particular adhesive; although other types of liquid adhesives (e.g. thermosetting) could show better performance. Figure 5 and Figure 6 show chip embedding test vehicles using pressure sensitive tape and thermoplastic adhesive, respectively.

Assembly test run

To verify the contact resistance between the aluminum bond pads on the chip and the lands on copper foil, a dedicated test vehicle was designed containing daisy chain and four-point measurement test structures. This test design is realized on a single-sided polyimide flex (50 um PI and 18 um ED copper). The choice for PI was made to circumvent any temperature restrictions during die bonding, making it possible to use the same parameters as for bonding onto the copper foil. Two series of tests are performed. The goal of the first series is to determine the contact resistance at the copper side. To assure a good contact at the chip side, chips with Ni/Au bumps are used. The chips for the second series of experiments are not bumped, focusing on the contact between the isotropic conductive adhesive and the aluminum bond pads.

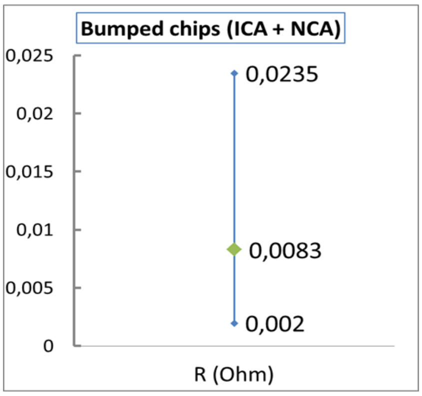


Figure 7: Contact resistance for bumped chips. (18 contacts measured: 6 showed no contact, 1 was non-ohmic, 1 had a resistance of 0.4 Ω, and the remaining 10 are included in the graph)

As expected, the series with bumped chips shows a very low contact resistance (Figure 7), while the non-bumped chips demonstrate non-ohmic contact resistance due to the presence of aluminum oxide on the chip pads. Some extra measures can be taken to remove this oxide prior to chip placement, although the long-term reliability without some form of bumping will remain a concern.

A complete filling of the die bond adhesive underneath the chip with a minimum fillet at the edge and a uniform thickness are essential to avoid damage to the chips during embedding.

Cost Considerations

The technology for embedding active components in foils is still under development, so a complete cost modeling cannot be performed at this time. Some general considerations concerning material cost can give an idea if this technology can truly be labeled “low-cost”. For the calculation, a high-volume production line with a yield *Y*, manufacturing over 1 million units per year, is assumed. Each unit is tested after production and only good units are shipped.

A possible application for this technology is the smart blister, a medicine package which is meant to improve therapy compliance. The smart blister detects if and when a dosage is taken out of the blister, processes this information, and communicates the action to the environment (patient, doctor, nurse etc.), thus supporting a well-controlled medicine taking process. Typical dimensions for these circuits are 5 cm by 10 cm, including a single chip (1 mm x 1 mm) to collect and transmit the data. The material costs for a 50 µm thick PET film is around € 1.0/m^2 and € 3.0 for one square meter of untreated 20 µm rolled-annealed copper foil. The cost for the adhesive used for embedding is targeted to be between € 1.0/m^2 and € 5.0/m^2. This results in an overall material cost of € 5.0/m^2 to € 9.0/m^2. The smart blister contains one chip per module and with the given size, 200 modules can fit in one square meter. Even when the price of the chip would be as low as € 0.1 per chip, the chip cost per square meter quickly rises to € 20.0/m^2. Bumping and thinning would add another € 0.0025 and € 0.006 per chip, respectively, or € 0.5/m^2 and € 1.2/m^2. Combining the different cost contributions, excluding the processing cost, leads to a total cost of € 26.7/m^2 to € 30.7/m^2.

Expressing the chip-related cost in euro per square meter, albeit unusual, helps to compare the different cost factors. The cost of the chip is clearly the dominant factor, while the cost of chip thinning for this application is similar to the material cost of the PET. The cost calculation is based on 200 modules per square meter, resulting in a price per unit of between € 0.13 and € 0.15 divided by the yield Y. As mentioned before, the cost reduction from developing a process without the need for chip bumping would be minimal. On the other hand, lowering the cost of the adhesive from € 5.0/m^2 to € 1.0/m^2 reduces the overall cost by more than 13 %.

A comparable process using spin-on polyimide to coat a layer of 100 µm over the chips would cost € 192.7/m^2. For this competing technology, the material cost (€ 171.0/m^2) would be far greater than the chip cost (€ 21.7/m^2). A more correct comparison would need to take into account the difference in processing cost and the integration density of both technologies.

The cost of more advanced modules with several embedded dies is completely dominated by the chip cost. For a body area network patch of 3 cm by 5 cm including three chips, the silicon cost would be more than 99 % of the total material cost. As such, the low-cost aspects of the proposed technology become more apparent for large substrates with one or two small chips. Changing to a lower cost material, however, will only lead to an overall cost reduction if the yield and reliability are not reduced in the same way.

Conclusion

Developing a chip embedding solution based on PET foil requires a completely different approach than traditional chip embedding in rigid or flexible substrates. A simple and cost-efficient process is crucial. Requirements concerning electrical and mechanical reliability will depend strongly on the intended application. These would not only be situated in medicine packages and smart bandages, but also in areas where chip integration is not considered at the moment.

Future work will include further optimization of the process using the current materials, but also investigating alternatives as hot melt adhesives and pressure sensitive adhesives that continue to crosslink under heat exposure. Increasing the reliability without raising the cost will prove the main challenge for the future.

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