Die-to-Die Adhesive Bonding for Evanescently-Coupled Photonic Devices

S. Stanković[a], D. Van Thourhout[a], G. Roelkens[a], R. Jones[b], J. Heck[b], and M. Sysak[b]

[a] Department of Information Technology, Ghent University - imec, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium
[b] Intel Corporation, 2200 Mission College Blvd. SC12-236, Santa Clara, CA 95054, USA

Heterogeneous integration of III-V semiconductor materials on a SOI (silicon-on-insulator) platform is a promising method for fabrication of active photonic devices. It requires a reliable and robust bonding procedure that also enables an effective optical coupling between III-V layers and SOI waveguides. Direct bonding is usually used for this purpose, but due to its strict requirements for contamination-free and smooth bonding surfaces, it might not be sufficiently robust for industrial-scale fabrication. As an alternative technique, in this paper we present an adhesive bonding procedure based on the use of DVS-BCB. We developed a die-to-die adhesive bonding procedure, resulting in less than 100nm-thick bonding layers thereby enabling evanescent optical coupling between III-V layers and silicon waveguides. The process shows very good robustness and bonding strength (break-down shear stress of 2MPa). In perspective, we plan to scale-up the process to a multiple die-to-wafer bonding procedure which would be suitable for industrial-scale fabrication.

Introduction

Silicon photonics is emerging as a very promising technology for the fabrication of high-performance photonic integrated circuits. Interest in this field has been steadily growing in the past decade, partially driven by the need for faster communication between the increasing numbers of microprocessors integrated on a single chip. Silicon is transparent at telecommunication wavelengths (1.3 μm and 1.55 μm) and offers a prospect for fabrication of high-speed communication photonic devices. Silicon photonics is based on the silicon-on-insulator (SOI) material platform and shares the same fabrication procedures and tools with microelectronics, which reduces the costs of development and fabrication. This also makes it a technology of choice for integration of photonic devices with microelectronic circuits on a single chip, which is envisioned as one of the most-promising strategies for developing the next-generation of high-performance integrated circuits.

Despite great advances that have been made recently in silicon photonics, particularly in the area of passive photonic circuits, fabrication of the light sources on this platform is still a big problem due to silicon's indirect bandgap. One solution is heterogeneous integration of III-V semiconductor materials, where the light emission from the III-V material is coupled to the SOI waveguides. The lattice mismatch between silicon and InP-based materials (used for light sources at 1.3 μm and 1.55 μm) is too large for successful

epitaxial growth of sufficiently thick layers of InP and related compounds. Thus, a reliable and robust procedure for bonding III-V materials on top of silicon-based waveguides is required. Preferably, it should also provide evanescent optical coupling between III-V layers and the underlying SOI waveguides. This coupling scheme enables the bulk of the guided mode optical power to be within the silicon waveguide itself and requires no additional coupling structures, such as tapers or gratings, which are not easy to fabricate. In recent years, direct bonding has been the preferred technology for this purpose and several evanescently-coupled hybrid III-V/Si lasers, based on this procedure, have already been reported (1-5). However, since direct bonding is very sensitive to surface topography, contamination or presence of small particles, this technique may not be sufficiently robust for industrial-scale heterogeneous integration of III-V dies and silicon wafers where such strict requirements are difficult to meet.

Compared to direct bonding, adhesive bonding is generally more tolerant to surface roughness, particle contamination and, to some extent, topography of the bonding surfaces. Since curing of adhesives is typically a low-temperature process, the stress induced due to the difference in thermal expansion of the bonded materials is also generally small. In literature, both thermoplastic polymers, like PMMA (6), SU-8 (7) and thermosetting polymers, such as spin-on glass (8), polyimide and BCB (9) are described. Our heterogeneous integration scheme assumes bonding of unprocessed III-V dies (with its epitaxial layers down) on top of previously processed SOI waveguide circuits, as shown in Figure 1a). Very precise alignment is not required, since III-V dies are further processed after the bonding. Thermoplastic polymers usually have a relatively small post-bonding thermal budget, which is a disadvantage since the III-V post-bond processing requires die exposure to 300 °C. Thus, thermosetting polymers are the focus of this work.

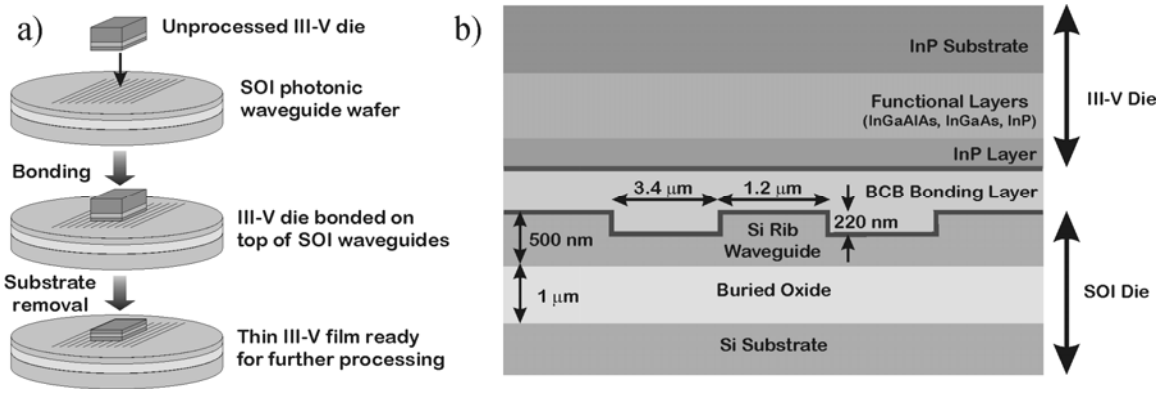

Figure 1. a) Heterogeneous integration of a III-V die on top of SOI waveguides based on bonding; b) Layout of our silicon rib waveguide structure with a III-V die comprising InGaAlAs active layers bonded on top of it.

The bonding adhesive of our choice is a thermosetting polymer, divinylsiloxane-bis-benzocyclobutene (DVS-BCB), also referred to as BCB. This is a commercially available polymer, known as Cyclotene®™, produced by The Dow Chemical Company. BCB is a well-known material and it has been studied for various applications including adhesive wafer bonding and packaging (9,10). During polymerization, it produces no byproducts (thus, no outgassing), and it can withstand temperatures required for III-V processing. In recent years, the Photonics Research Group at Ghent University in Belgium has reported a BCB bonding process (11) and it has demonstrated photodetectors (12,13), hybrid III-

V/Si lasers (14) and several other photonics devices (15) based on BCB bonding. However, all these devices were based on a manual BCB bonding process, suitable for research and development, but not for an industrial cleanroom environment. On the other hand, evanescently-coupled hybrid III-V/Silicon lasers show a great potential as light sources that are so much needed in silicon photonics. Therefore, we developed a reliable and robust, machine-based BCB bonding process that will provide sufficiently thin bonding layers (<100 nm), suitable for fabrication of evanescently-coupling hybrid lasers.

Die-to-Die Bonding – Tools and Experimental Setup

Our goal is to bond a III-V die, with epitaxially grown InP-based layers, on top of SOI photonic waveguides. Post-bonding processing of a III-V die is to be used to fabricate an evanescently-coupled hybrid III-V/Si laser. In our experiments, we use silicon rib waveguides as shown in Figure 1b). The width of the waveguides is 1.2 μm and they are surrounded by 3.4 μm wide and 220 nm deep trenches. Thickness of the silicon slab layer is 500 nm, while the thickness of the buried oxide layer is 1 μm. As it would be too costly to fully cover the SOI waveguide circuit with III-V wafers, we focus on a die-to-die bonding procedure, which can be scaled-up to die-to-wafer and eventually multiple die-to-wafer bonding procedure. The size of III-V dies that are used in the experiments varies, but it is never smaller than 5 mm × 5 mm, or larger than 8 mm × 8 mm. Size of the SOI die is either 20 mm × 20 mm or 10 mm × 10 mm. In our bonding procedures, we use Cyclotene 3022-35 which nominally produces the thinnest BCB cured films (1 μm - 2.4 μm) compared to other resins from the Cyclotene 3000 Series (16). To obtain bonding layers much thinner than 1 μm, we dilute BCB with mesitylene in different volume proportions. Such a diluted solution is spin-coated on the SOI die after which III-V and SOI dies are brought into contact and the BCB is subsequently cured.

Bonding Tool

Switching from a manual to a machine-based bonding procedure was a basic prerequisite for bringing our bonding process closer to industry-compatible procedures. For this purpose, we chose to work with a Süss MicroTec ELAN CB6L wafer bonding tool. It is classified as a manual bonding tool (as compared to fully automated bonders) and is specifically designed for the needs of research and development and for the pre-production wafer bonding market. The CB6L wafer bonder can handle wafers of up to 150 mm diameter. Wafers are placed on the transport fixture and loaded into the process chamber. The bonding process itself is defined by the user who creates the bonding recipe, which is a sequence of steps in which all the relevant process parameters and its tolerances are defined. However, ELAN CB6L wafer bonder is not designed for handling such a small dies as we are using in our experiments. The standard transport fixture of this wafer bonder can handle wafers of minimum 100 mm diameter, although with the special equipment, wafers of 50.8 mm diameter can be handled as well. Thus, we had to solve this problem and enable working with dies.

Die-to-Die Bonding Setup

Our approach is to temporarily attach both III-V and SOI dies to auxiliary wafers that act as die carriers. Then, we load these wafers into the processing chamber of the wafer

bonder, with the dies attached to them, and proceed with the bonding. In this way, we are able to use a standard transport fixture of the bonding tool, designed to handle the wafers, while in the end we bring only the dies into contact. The cross-section of this die-to-die bonding setup is given in Figure 2a). Before bringing the dies into contact, the metallic spacers (that are integral parts of the transport fixture) are placed between the top and the bottom carrier wafers. Specifically, the thickness of our III-V dies is around 375 μm and the thickness of SOI dies is around 725 μm, making our bonding stack roughly 1100 μm thick. On the other hand, the thickness of metallic spacers is only 100 μm. To compensate for this difference, two additional Si dies are bonded on the bottom carrier wafer at the exact locations were the metallic spacers are positioned. These dies act as the additional spacers. In this way, metallic spacers rest on these "spacer-dies" and enable the existence of a gap between the SOI die and III-V die, prior to the bonding. When we want to bring the dies into contact, metallic spacers are retracted and the III-V die falls on the SOI die, while the gap is now left between the Si spacer-dies on the bottom carrier wafer and the top carrier wafer (see Figure 2b)).

The additional advantage of this setup is that, once the metallic spacers are in place, the top carrier wafer can easily rotate around its vertical symmetry axis, as shown in Figure 2c). To some extent, it is possible also to have a translation movement of the top carrier wafer with respect to the bottom one. In this way, we can manually adjust the relative position of the bonding dies before placing the clamps that fix the top and the bottom carrier wafers, prior to loading the transport fixture into the processing chamber.

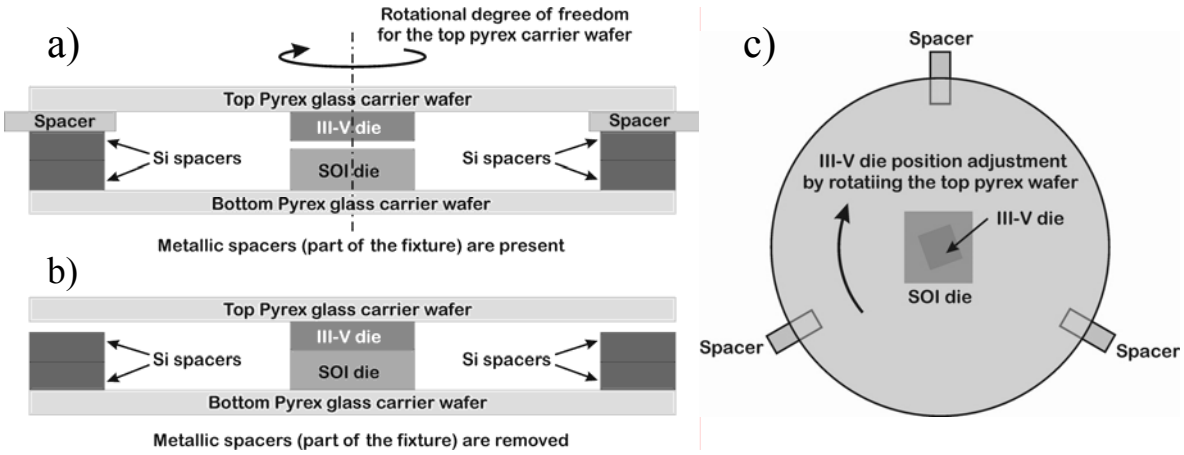

Figure 2. Die-to-die bonding setup: a) cross-section of the setup with spacers still in place – prior to bonding; b) cross-section of the setup after the spacers are retracted – III-V and SOI dies come into contact; c) top view of the setup – rotational degree of freedom enables easy positioning of a III-V die.

We have chosen 100 mm diameter Pyrex glass wafers to act as the carrier wafers. They are able to withstand the curing temperatures of BCB and provide relatively good mechanical strength, while being much less brittle than Si wafers. One of the basic problems was how to temporarily fix the dies to these glass carrier wafers prior to bonding. This attachment should be able to withstand some extreme conditions in the processing chamber (high vacuum, temperatures usually up to 250 °C) and also be able to easily detach after the bonding is finished. In our first experiments, we used Apiezon® H Grease, able to withstand temperatures up to 240 °C and suitable for use in a vacuum

environment. Although this grease did the intended job, it was not convenient to work with. Applying the grease required a lot of dexterity and it was not possible to have good control over the thickness of the grease between the attached die and the carrier wafer. It was not always easy to detach the samples after bonding, neither it was easy to clean them. Therefore, we started using thermal release tape Revalpha No.31950E from Nitto Denko. The release temperature of this tape is 200 °C, which is less than the usual curing temperature for BCB. However, we performed a series of tests and confirmed that the tape can withstand temperatures up to 240 °C, for 1 hour, without substantial increase in residual adhesive strength. The use of tape brings many advantages, like controllable and reproducible thickness of the bonding medium between the die and the carrier wafer, ability to easily tailor it to the shape of the dies and easy detachment of the dies from the carrier wafers after completion of the bonding process.

Description of the Bonding Procedure

The entire bonding process can be divided into two phases. The first one is preparation of III-V and SOI dies, while the second one is the bonding itself. Preparation of the samples has a goal to remove any contamination from the bonding surfaces of the dies and to condition these surfaces so that BCB can be easily and effectively applied. Although the adhesive bonding is somewhat tolerant to particle contamination, since we want to achieve bonding layers of less than 100 nm thickness, it is clear that removing any residual particles from the bonding surfaces is essential. Cleaning the surface of SOI dies is performed using Standard Clean 1 (SC-1) solution, comprising aqueous ammonia (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water in volume ratios of 1:1:5, respectively. The SOI die is exposed to SC-1 at 70 °C, for 15 minutes, after which it is rinsed with DI water, dried and placed on a spin-coater. Usually, we first spin-coat adhesion promoter AP3000 and then we spin-coat the BCB:mesitylene solution. Our usual spin-coating procedure comprises the spreading step, lasting 5 seconds at 500 rpm, followed by the spin-coating step of 40 seconds at 3000 rpm. After this, the SOI die is baked on a hotplate at 100 °C, for 4 minutes, to let mesitylene evaporate and the BCB film to stabilize. Finally, the SOI die is mounted on a carrier wafer and placed into the transport fixture.

In most of our experiments we have used III-V dies cleaved from epitaxially grown InP-based wafers, comprising layers of InGaAlAs and InGaAs. In all of these dies, the material that was in direct contact with the bonding BCB layer was indium phosphide. In some occasions, as a much cheaper alternative, we used pure InP dies instead. However, there is no equivalent cleaning solution for III-V dies, like SC-1 for SOI and silicon dies. To overcome this problem, we include two sacrificial layers that are grown on the top of our epi layer stack. On the wafer surface, there is a 100nm-thick InP layer, followed by a 100nm-thick InGaAs layer below. Prior to bonding, we use selective wet etching to remove these two layers, one at a time. In this way, any particles and contaminants present on the III-V die surface are removed during wet etching, exposing a clean InP layer that will come to contact with BCB during the bonding. For easier handling, the III-V die is first attached to the carrier wafer and then wet etching is performed. After removing sacrificial layers, the III-V die is rinsed with DI water, dried and mounted on the transport fixture.

Once both III-V and SOI dies, attached to their carrier wafers, are mounted on the transport fixture, the fixture itself is loaded into the processing chamber of the wafer bonder and the bonding recipe is started. Our bonding recipe starts with bringing the processing chamber into vacuum and heating top and bottom heaters to 150 °C. After 5 minutes in vacuum, the dies are brought into contact. After this, dies are kept at 150 °C for 20 minutes, while the bonding pressure is applied to them. Subsequently, the temperature is slowly increased up to 240 °C, with a ramp of 1.6 °C/min. The bonding head is raised at 180 °C and no pressure is applied afterwards. After reaching 240 °C, dies are kept at this temperature for 1 hour in a nitrogen atmosphere, at 1000 mbar. Although a usual BCB curing is performed at 250 °C for 1 hour, we have lowered this to 240 °C. Initially, this was to comply with temperature limit for Apiezon® H Grease and afterwards we wanted to avoid exposing thermal tape to temperatures much higher than 200 °C, as it would increase its residual adhesiveness. According to Dow Chemicals technical notes (15), the BCB degree of polymerization in these two cases should be around 98% and 95%, respectively, which should not result in a significant difference. After curing is finished, the bonded samples are cooled to room temperature and finally unloaded from the processing chamber. Afterwards, the InP substrate on a III-V die is grinded down to ~70 μm using a lapping tool and is subsequently removed by wet etching in a 37% HCl(aq.) solution. In the end, a thin III-V film with the functional layers remains bonded to SOI die, ready for further processing.

Results of the Bonding Experiments

A series of bonding tests was performed in order to optimize the bonding process and to find the best settings and parameters. After initial tests using Apiezon® H Grease, we have switched to thermal release tapes which provided more convenient die fixing and detachment, as well as more stable results. Due to a relatively small bonding area, limited by the III-V die size (see Figure 2b)), it was essential to find the optimum bonding pressure. The area of the bonding head in our wafer bonder (A_{bh}) is 222 cm^2, which is much more than the die bonding area (A_{die}) – usually around 0.5 cm^2. The actual bonding pressure exerted on the dies during the bonding is scaled up by A_{bh}/A_{die} ratio, compared to the bonding tool pressure, which is the differential pressure between the gas in the bonding head cushion and the processing chamber and is defined as a parameter in the bonding recipe. In our experiments, we keep this value at 10 mbar, which is at the lower limit of our wafer bonder. The size of III-V dies slightly varies in our tests, but the actual bonding pressure in most of our experiments is in the range of 4-5 bar (400-500 kPa).

Bonding Layer Thickness

In our first bonding experiments, we have focused on achieving bonding layers thinner than 100 nm. Since the bonding pressure (p_{die}) was already high and not easily reproducible, we have directed our attention to varying the rotation speed during BCB spin-coating and changing the BCB volume ratio in BCB:mesitylene solutions that we were using. To assess the impact of these to parameters we have spin-coated BCB solutions on flat, unpatterned, InP dies and subsequently cured them. Using lithography and dry etching of BCB, we would make “windows” in a cured BCB film and measure its thickness at the edges using a contact profilometer. BCB:mesitylene ratios that we used in out tests were 2:3, 1:2, 1:3 and 1:7, corresponding to BCB volume ratio in solutions of

40%, 33%, 25% and 12.5% (v/v). Results of these tests are shown in Figure 3. Obviously, changing BCB content in the solution has more impact on the final BCB film thickness than increasing the rotation speed. Other tests showed that spin-coating BCB on a patterned SOI die, at speeds above 5000 rpm, produced a non-uniform film immediately after spin-coating. To avoid this and further standardize our process, we have fixed our spin-coating speed at 3000 rpm and used this value in all the subsequent tests.

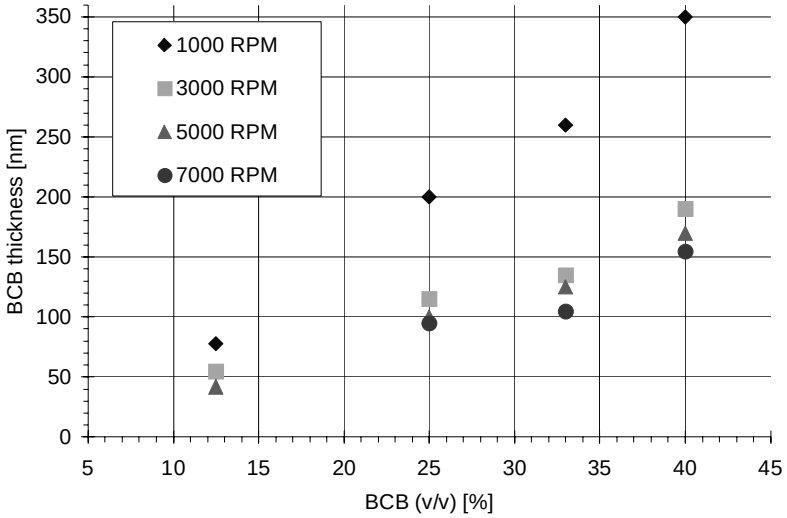

Figure 3. Thickness of cured BCB films, spin-coated on flat InP dies, depending on BCB volume ratio in BCB:mesitylene solution and rotation speed during spin-coating.

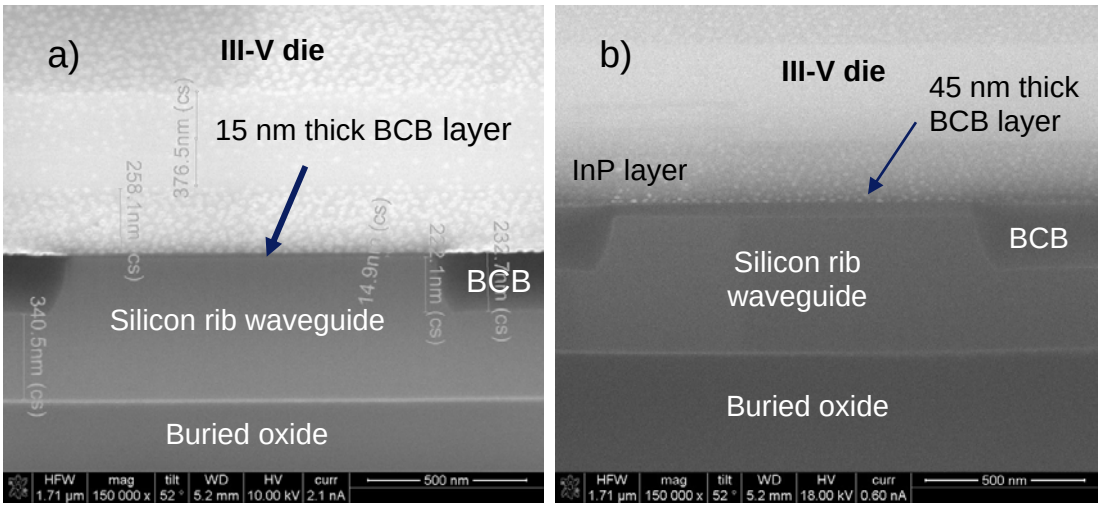

Figure 4. SEM images of ultra-thin BCB bonding layers on top of silicon waveguides: a) 15nm-thick layer, obtained using 1:7 BCB:mesitylene solution; b) 45nm-thick layer, produced by 1:3 BCB:mesitylene solution.

Thus, we were left with only BCB:mesitylene solution ratio as a variable parameter to achieve the desired bonding layer thickness. To measure this thickness, we would make a cross-section through a bonded III-V film, using a focused ion beam (FIB) tool and make a SEM image of it. After initial tests, we focused on 1:7 BCB:mesitylene solution. Using it, we managed to achieve bonding layers above Si rib waveguide as thin as 15 nm

(Figure 4a)). However, in our post-bonding die processing, we observed peeling of the III-V film around its edges during wet etching of the InP substrate. We also found that, in the bonding area, not all the trenches around Si rib waveguides were filled with BCB, which indicated that this solution was perhaps too much diluted and there was not enough BCB. Thus, we switched to 1:3 BCB:mesitylene solution, where we managed to achieve bonding layers of around 45 nm, as shown in Figure 4b). The bonding yield improved, but we sill saw some III-V film peeling during wet etching of the InP substrate. To improve process further, we started applying AP3000 adhesion promoter to the SOI die, prior to spin-coating BCB. Despite using the same "1:3" solution as before, we noticed that the BCB layer thickness increased to around 90 nm (Figure 5a), probably due to better BCB adhesion to the silicon surface and increased viscosity during spin-coating. In addition, III-V film peeling was drastically reduced and we were able to obtain high-quality III-V films, with regular, sharp edges, as shown in Figure 5b).

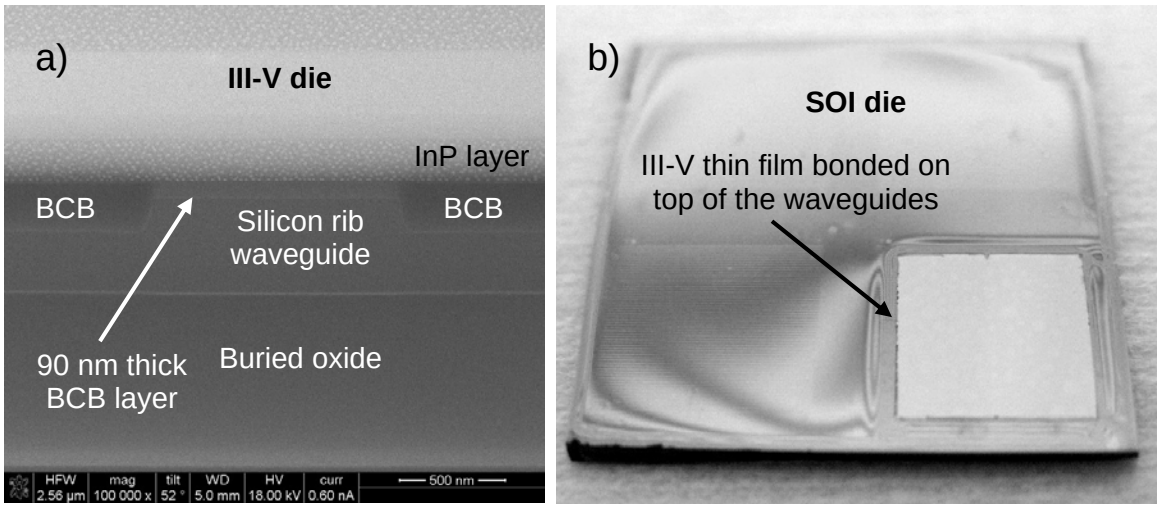

Figure 5. Impact of adhesion promoter AP3000 on the bonding test results: a) BCB layer thickness increased to 90 nm (using 1:3 BCB:mesitylene solution); b) peeling of III-V film is minimized during wet etching, resulting in clear and sharp III-V film edges.

Bonding Layer Uniformity

To assess uniformity of the BCB bonding layer, we have conducted several tests in which we were bonding pure InP dies on top of SOI waveguides. After the bonding, InP was etched in HCl until the III-V die was completely removed, exposing the underlying cured BCB film. We would than deposit a 40nm-thin layer of gold on top of this BCB film and use an optical profilometer to obtain information about the surface uniformity. Result of one of these tests, presented in Figure 6, shows the BCB surface profile along the direction perpendicular to SOI waveguides. We can clearly see notches (12-14 nm deep), corresponding to locations of the SOI waveguides, surrounded by 220nm-deep trenches. Despite this, and surface roughness of 3.5 nm we see no much variation in the profile, which implies a good BCB layer uniformity. In the cases when the III-V dies with epitaxially grown functional layers were bonded, uniformity was assessed by measuring BCB layer thickness in several locations, using the FIB tool. Usually, the variation in BCB thickness was around 10 nm. However, in several cases, when large pieces of III-V film peeled-off during wet etching, we observed variation in colour of the exposed BCB bonding layer, which indicates the variation in its thickness. Measurements

at several locations revealed that the bonding layer thickness in these cases could vary from 20 nm to 120 nm. The cause for such a deviation from an expected behaviour, might lay in the topography of the bonded III-V die itself. Optical profilometer measurements showed that bow in some III-V dies can be several hundreds of nanometers. Currently, we are proceeding with tests that should indicate if there is a strong correlation between III-V die topography and BCB bonding layer uniformity.

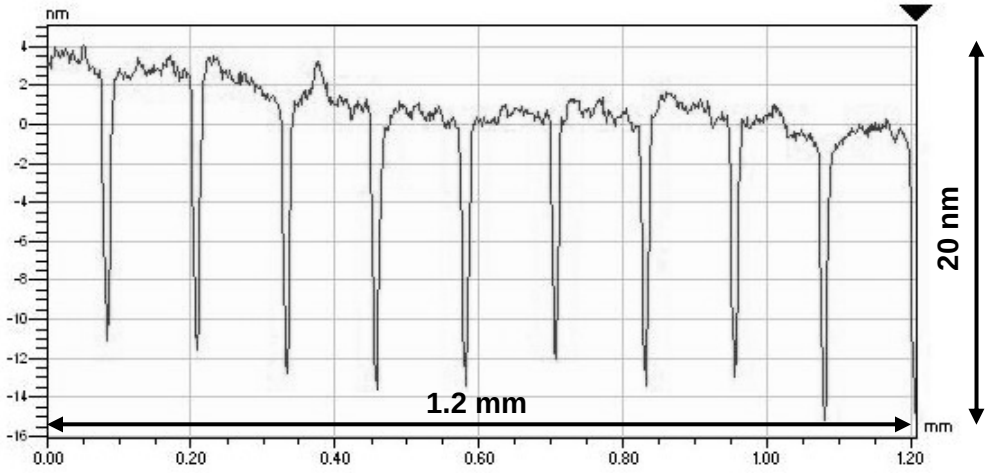

Figure 6. BCB surface profile perpendicular to SOI waveguides. Notches are observed at the locations of SOI waveguides, at 250 μm pitch.

Shear Stress Tests

To assess the strength of the bonded dies, we prepared a batch of 11 bonded samples with standardized die sizes: 5 mm × 5 mm for III-V dies and 10 mm × 10 mm for SOI dies. In this batch, we used "1:3" bonding solution, except in one case, where dies were bonded using undiluted BCB, as a reference. Shear strength was measured using a die shear test method. Measured sheared stress values, at which the dies broke, ranged from 1.98 MPa to 2.02 MPa, with an average value of 2 MPa and standard deviation 0.017 MPa. Bond strength was measured for different BCB layer thicknesses with no significant difference seen for BCB thicknesses between 32-83nm. Such a small variation (within 1%) in the shear stress indicates a very good robustness of our bonding process, while the average shear stress value of 2 MPa is testimony of a solid bonding strength.

Conclusions

We have developed a die-to-die adhesive bonding procedure, based on the use of DVS-BCB, suitable for heterogeneous integration of III-V dies on top of SOI photonic waveguides. The demonstrated BCB bonding layers thickness is less than 100nm which is sufficient for efficient evanescent coupling between III-V semiconductor layers and silicon waveguides. The process shows good robustness and solid bonding strength and we believe that it provides a promising alternative to direct bonding for the purpose of heterogeneous integration of III-V dies and SOI wafers. Although primarily targeted for hybrid lasers and optical amplifiers, this bonding procedure can also be used for fabrication of photodetectors based on evanescent coupling. In our future work, using this

bonding process, we plan to demonstrate evanescently-coupled photonic devices, based on III-V/Silicon heterogeneous integration. In perspective, this process has a potential to be scaled-up and, as a further improvement, we plan to develop a multiple die-to-wafer DVS-BCB bonding procedure, which would bring it closer to an industrial-scale level.

Acknowledgments

This work was supported by a grant from Intel Corporation. Hanan Bar from Numonyx was responsible for fabrication of SOI wafers. Liesbet Van Landschoot from Photonics Research Group at Ghent University made SEM images, while Steven Verstuyft, from the same group, provided technical assistance in the cleanroom work.

References

1. A.W. Fang, H. Park, R. Jones, O. Cohen, M. J. Paniccia, and J. E. Bowers, *IEEE Photonic Tech. L.*, **18**, 1143, (2006).
2. J. Van Campenhout, P. Rojo-Romeo, P. Regreny, C. Seassal, D. Van Thourhout, S. Verstuyft, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, and R. Baets, *Opt. Express*, **15**, 6744, (2007).
3. X. Sun, A. Zadok, M. J. Shearn, K. A. Diest, A. Ghaffari, H. A. Atwater, A. Scherer, and A. Yariv, *Opt. Lett.*, **34**, 1345, (2009).
4. H.H. Chang, A.W. Fang, M. N. Sysak, H. Park, R. Jones, O. Cohen, O. Raday, M. J. Paniccia, and J. E. Bowers et al., *Opt. Express*, **15**, 11466, (2007).
5. A.W. Fang, E. Lively, H. Kuo, D. Liang, and J. E. Bowers, *Opt. Express*, **16**, 4413, (2008).
6. W. P. Eaton, S. H. Risbud, and R. L. Smith, *Appl. Phys. Lett.*, **65**, 439 (1994).
7. F. J. Blanco, M. Agirregabiria, J. Garcia, J. Berganzo, M. Tijero, M. T. Arroyo, J. M. Ruano, I. Aramburu, and K. Mayora, *J. Micromech. Microeng.*, **14**, 1047 (2004).
8. H. C. Lin, K. L. Chang, G. W. Pickrell, K. C. Hsieh, and K. Y. Cheng, *J. Vac. Sci. Technol. B*, **20**, 752 (2002).
9. F. Niklaus, P. Enoksson, E. Kalvesten, and G. Stemme, *J. Micromech. Microeng.*, **11**, 100 (2001).
10. D-H. Choi, C-H. Yeo, J-T. Kim, C-W. Ok, J-S. Kim, Y. Kwon, and Y-H. Im, *J. Micromech. Microeng.* **19,** 075013, (2009).
11. G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, *J. Electrochem. Soc.*, **153**, G1015 (2006).
12. J. Brouckaert, G. Roelkens, D. Van Thourhout, and R. Baets, *J. Lightwave Technol.*, **25**, 1053, (2007).
13. Z. Sheng, L. Liu, J. Brouckaert, S. He, and D. Van Thourhout, *Opt. Express*, **18**, 1756, (2010).
14. G. Roelkens, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, *Opt. Express*, **14**, 8154, (2006).
15. L. Liu, G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, and R. Baets et al., *J. Nanosci. Nanotechno.*, **10**, 1461, (2010).
16. http://www.dow.com/cyclotene/prod/302235.htm (Processing Procedures for CYCLOTENE 3000 Series Dry Etch Resins)