Overview of three-phase inverter topologies for distributed generation purposes

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Abstract - The increasing presence of single-phase distributed generators and unbalanced loads in the electric power system may lead to unbalance of the three phase voltages, resulting in increased losses and heating. Distribution network operators are seeking to install larger DG units (viz. $>$ 5kVA in Belgium) by means of three-phase connections instead of single-phase to reduce voltage unbalance. There are several possible topologies to connect the DG units to the three-phase distribution network. These topologies can be divided into three groups: the three-phase three-wire inverters, the three-phase four-wire inverters and the multilevel inverters. In this paper, an overview of the aforementioned topologies is given.

INTRODUCTION

Over the last years, an increase of distributed generation units connected to the low-voltage distribution network is observed. These distributed generation units are fed by renewable resources like PhotoVoltaics (PV), (micro-)Combined Heat Power (CHP) and Wind Power [1, 2]. This leads to the development of relatively small generation units, geographically distributed and connected to the distribution network.
The distributed generation units are usually connected to the low-voltage distribution network by means of a single-phase connection. The increasing presence of single-phase distributed generators and unbalanced loads in the electric power system may lead to unbalance of the three phase voltages, resulting in increased losses and heating. Distribution network operators are seeking to install larger DG units (viz. $>$ 5kVA in Belgium) by means of three-phase connections to reduce voltage unbalance.
The three-phase inverter topologies can be divided into three groups: the three-phase three-wire inverters, the three-phase four-wire inverters and the multilevel inverters. In this paper, an overview of the aforementioned topologies is given. These three-phase inverter topologies can also be used for active power filter applications; a review of different active filters is given in [3] and different control techniques for active power filters are discussed in [4].

INVERTER TOPOLOGIES

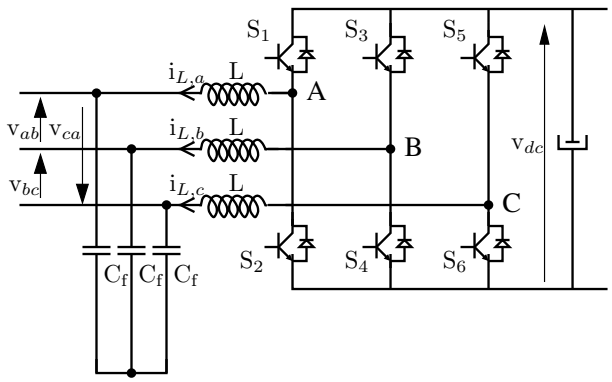
In this paper, three commonly used inverter topologies are discussed where each category is further classified into several subcategories.

Three-phase three-wire inverter topology

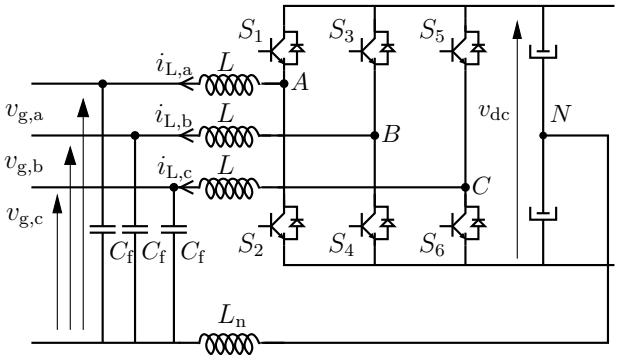
In Fig. 1(a) a three-phase three-wire inverter topology is depicted. Due to the lack of a fourth wire, this topology is less interesting for a low-voltage distribution network which is typically a four-wire system. A fourth wire can be added by connecting the three-wire inverter to a $\triangle/\mathrm{Y_g}$ isolation transformer which is heavy and costly and thus not desired in many applications [5]. In some countries (eg. United Kingdom) power supply companies demand connecting distributed resources via an isolating transformer for eliminating possible zero-sequence or dc components in the generated voltages and for the increased protection it affords [6]. This fact can be used as an advantage since the transformer can form part of a filter impedance and may, therefore, reduce the undesired harmonic content of the output current.
Using the three-phase three-wire topology, only two parameters can be controlled, which is disadvantageous in case active power filtering functions are desired [7].

Three-phase four-wire inverter topologies

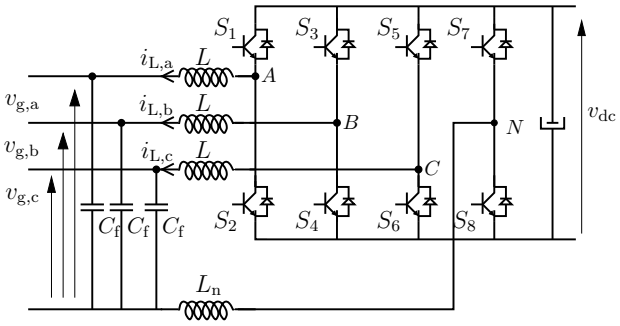
The second group of inverters are the four-wire transformerless inverters which are usually more preferable. There are two common ways to provide the neutral connection: retaining a three-leg inverter but splitting the dc-bus with a pair of capacitors to provide the fourth wire or retaining a single dc-bus capacitor by providing a fourth leg (and thus an extra pair of switches) [5, 8].



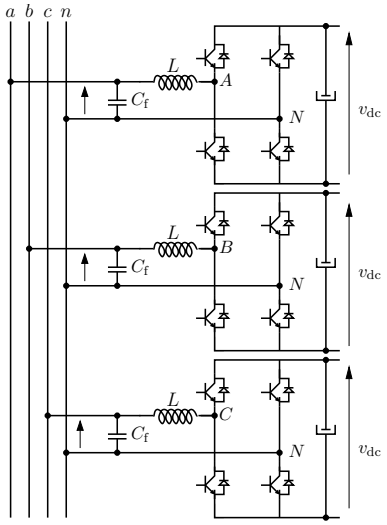
(a) Topology of the three phase three-wire inverter



(b) Topology of the three phase four-wire inverter with split dc-link



(c) Topology of the three phase four-leg inverter



(d) Topology of the three phase four-wire multi-string inverter

Figure 1: Inverter circuit topologies

Split dc-link

The split-link topology is interesting due to its simple topology, usage of fewer semiconductors (compared to the four-leg inverter). Another advantage is that a three-phase split-link inverter essentially becomes three single-phase half-bridge inverters and permits each of the three legs to be controlled independently, making its current tracking control simpler than the four-leg inverter [8]. The split-link topology is depicted in Fig. 1(b).

Several problems are introduced by choosing the split-link topology. One of them is ensuring equal voltage sharing between the split capacitors and the need to attenuate voltage ripple. This results in the need for large and expensive dc-link capacitors or even extra balancing structures [9]. A large neutral current (due to either unbalanced or nonlinear loads) causes a perturbation in the split voltages. Such a perturbation needs to be compensated for in the control scheme and risks malfunction of the inverter. Several solutions for balancing the split capacitor voltages are found in literature [5, 9–11].
Another disadvantage is caused by the fact that the split-link topology requires that the phase-voltage peak is less than or equal to half the total dc-link voltage, whereas the four-leg inverter can follow a line-voltage peak equal to half the total dc-link voltage. This gives an approximately 15% advantage in dc voltage utilization in favor of the four-leg inverter. In [8], a split voltage controller is developed to obtain maximum dc voltage utilization.

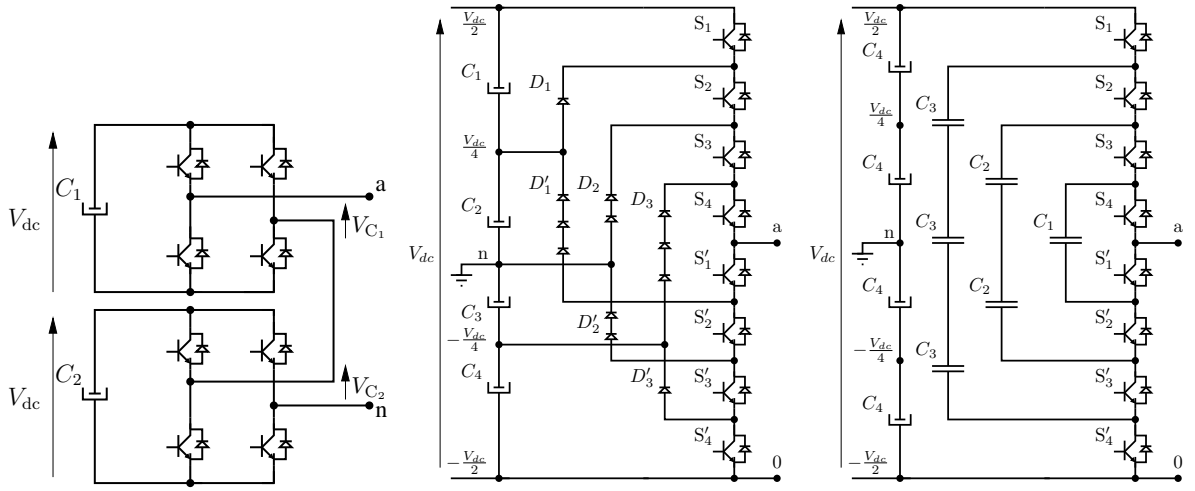
Despite the several disadvantages corresponding to this topology, this topology is preferable for active filtering and distributed generation applications due to its simple control. Different solutions are already described in literature [5,8–11] for the previously described disadvantages such that they not pose a fundamental problem.

Four-leg inverter

Another way of providing a neutral connection for three-phase four-wire systems is using a four-leg inverter topology and tying the neutral point to the mid-point of the fourth neutral leg [12]. A four-leg inverter topology is depicted in Fig. 1(c). The split dc-link topology suffers from an insufficient utilization of the dc-link and requires large and expensive capacitors, this is avoided when using the four-leg inverter [13]. The extra two switches result in a complicated control which makes the topology less interesting. Nevertheless there is a growing interest in four-leg inverters for three-phase four-wire applications [12].

Multi-string inverter

PV sytems as an alternative energy resource or an energy-resource complementary in hybrid systems have been becoming feasible due to the increase of research and development work in this area [14]. In order to maximize the succes of the PV systems a high reliability, a reasonable cost, and an user-friendly design must be achieved in the inverter topology. An inverter topology which possesses the previous described properties and is commonly used in PV applications is the multi-string topology. This topology permits the integration of PV strings of different technologies and orientations (north, south, eas and west) [2]. In Fig. 1(d) a single-phase multistring inverter is shown. This topology can be seen as three single-phase inverter which makes it uninteresting in view of voltage unbalance. This can be avoided by using three-phase multi-string inverters [2].



(a) Cascaded multilevel inverter topology (b) Five-level diode clamped multilevel inverter circuit topology (c) Five-level flying capacitor multilevel inverter circuit topology

Figure 2: Inverter circuit topologies

Multilevel inverter

The general idea of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources [15]. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. The number of achievable voltage levels is limited due to voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints [16].
The demand on high-performance inverters required by renewable energy systems has extended the applications of multilevel inverters for low-power systems ($<$ 20 kVA). Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-point clamped); capacitor-clamped (flying capacitors) and cascaded multicell with seperate dc sources [14–16].

Diode-clamped

The diode-clamped (also known as neutral-point-clamped) multilevel topology was the first widely popular topology and it continues to be extensively used [16, 17]. The fundamental building block of a phase leg five-level diode-clamped multilevel inverter is depicted in Fig. 2(b). The dc-bus voltage is split into five levels by four series-connected bulk capacitors, C_1 to C_4. The middle point (between capacitor C_2 and C_3) can be defined as the neutral point. The output voltage has five states:

$-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{4}$, 0, $+\frac{V_{dc}}{4}$, and $+\frac{V_{dc}}{2}$. There are five switch combinations to synthesize five level voltages across a and 0. Four complementary switch pairs exist in each phase. In this example, the four complementary pairs are (S_1,S'_1), (S_2,S'_2), (S_3,S'_3) and (S_4,S'_4).

The key components that distinguish this circuit are the diodes, D_i and D'_i which are used to clamp the switch voltage to the respective level of the dc-bus voltage. Although each active switching device only is required to block a voltage level of $\frac{V_{dc}}{m-1}$ (with m the level of the inverter), the clamping diodes must have different voltage ratings for reverse voltage blocking. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1) \times (m-2)$. This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under Pulse Width Modulation (PWM), the diode reverse recovery of the clamping diodes becomes the major design challenge [16].

Another (disadventageous) feature of the diode clamped topology is the unequal device rating, switch S_1 only conducts during $V_a = V_{dc}$, while switch S_4 conducts over the entire cycle except when $V_a = 0$. Such an unequal conduction duty requires different current ratings for the different switching devices. If the design is to suit the worst case, then each phase will have $2 \times (m-2)$ outer devices oversized.

In distributed generation applications, a transfer of real power from dc to ac takes place. When operating at unity power factor, the discharging time for each capacitor is different [15]. Such a capacitor discharging profile repeats every half cycle and this results in unbalanced capacitor voltages between different levels. Several solutions exist to solve this voltage unbalance problem such as applying voltage balancing control or adding voltage balancing circuits.

Flying capacitor

Fig. 2(c) depicts the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter [15,18] with independent capacitors clamping the device voltage to one capacitor voltage level [16]. The output voltage has five states: $-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{4}$, 0, $+\frac{V_{dc}}{4}$, and $+\frac{V_{dc}}{2}$. The voltage synthesis in a five-level flying capacitor inverter has more flexibility then a diode-clamped inverter because there are several switch combinations to achieve the desired voltage level. For example, for voltage level $V_{an} = \frac{V_{dc}}{4}$, there are four combinations:

1. S_1, S'_1, S'_2, S'_3 ($V_{a0} = V_{dc} - \frac{3V_{dc}}{4}$)
2. S_4, S'_2, S'_3, S'_4 ($V_{a0} = \frac{V_{dc}}{4}$)
3. S_3, S'_1, S'_3, S'_4 ($V_{a0} = \frac{V_{dc}}{2} - \frac{V_{dc}}{4}$)
4. S_2, S'_1, S'_2, S'_4 ($V_{a0} = \frac{3V_{dc}}{4} - \frac{V_{dc}}{4}$)

Like the diode-clamped topology, the flying capacitor topology also has unequal device duty problems.

By proper selection of the capacitor combinations, it is possible to balance the capacitor charge but this complicates the control. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, a m-level inverter will require a total of $(m-1) \times (m-2)/2$ clamping capacitors per phase leg in addition to $(m-1)$ main dc-bus capacitors. This requirement of a large number of storage capacitors is the major problem of this topology [15].

Cascaded inverter

The cascaded inverter is based on the series connection of single-phase inverter with seperate dc sources [19]. Fig. 2(a) depicts the power circuit for a phase-leg of a five-level inverter with two cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from $-2V_{dc}$ and $+2V_{dc}$ with five levels. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels.

For real power conversions, the cascaded inverter needs seperate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic which provide seperate dc sources [15]. The need for separate dc sources also limits its application.

The cascaded inverter requires the least number of components among all multilevel inverters to achieve the same number of voltage levels. Due to the fact that each level has the same structure, modularized circuit layout and packaging is possible. There are also no extra clamping diodes or voltage balancing capacitors required. Another advantage of this topology is that soft-switching can be used such that bulky and lossy resistor-capacitor-diode subbers can be avoided [15]. But the need for separate dc sources also limits its application.

CONCLUSION

In this paper an overview of three-phase four-wire inverter topologies is given. The most interesting topologies are the split dc-link and the four-leg inverter due to their simple topology. These topologies provide a three-dimensional control which is interesting in active filtering applications. Multilevel inverters posses the advantage of generating output voltages with extremely low distortion, generating smaller common-mode voltage and drawing current with very low distortion but a complex topology, a large number of components and a complicated control strategy have to be overcome. Nevertheless, the multilevel inverter will play an important role in the future.

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