1200 V dual-gate p-GaN bidirectional switches on 200 mm engineered substrates

G. Baratella, U. Chatterjee, S. Kumar, M. Borga, K. Geens, A. Vohra, S. Decoutere, B. Bakeroot

***Abstract*—In this paper, we present dual-gate bidirectional switches (BDSs) rated for 1200 V operation in both positive and negative bias, fabricated on 200mm GaN-on-QST® engineered substrates. The switches are p-GaN gate enhancement-mode (E-mode) high-electron-mobility transistors (HEMTs) that can conduct the current and block the voltage in both directions (drain to source or source to drain). The switches are fabricated with different design variations of the channel length and field-plates configuration and are tested in all 4 conduction modes (ON-state, forward and reverse diode modes and OFF-state). Additionally, a hard breakdown of the device well above the rated voltage is demonstrated, along with initial reliability tests that demonstrate promising performance of the devices.**

***Index Terms*—Bidirectional switch, gallium nitride (GaN), high electron mobility transistor (HEMT), 1200 V switch**

I. Introduction

GALLIUM Nitride (GaN) has emerged as a superior material for power electronics due to its wide bandgap, high electron mobility, and excellent thermal conductivity. These properties enable GaN devices to operate at higher voltages, frequencies, and temperatures compared to traditional silicon-based devices, resulting in improved efficiency and reduced system size [1], [2]. An enhancement mode (E-mode) high-electron-mobility transistor (HEMT) realized in GaN technology can achieve normally OFF operation, by incorporating a p-type GaN layer in the gate, which is crucial for safety and reliability in power applications [3].

Bidirectional switches can conduct current in both directions and block voltage in both polarities and are essential in modern power electronics for applications such as AC-AC and AC-DC converters, and battery management systems [4], [5], [6]. GaN-based bidirectional switches have been widely demonstrated and offer significant advantages over their silicon counterparts, including lower conduction losses, higher switching speeds, and reduced component count [7], [8], [9].

These benefits make GaN bidirectional switches highly efficient and compact, suitable for a wide range of high-performance power conversion applications [10], [11]. However, due to the increasing demand for higher voltages applications, such as the 800 V systems for electric vehicles, power switches with higher rating (i.e. 1200 V) are required [12]. Currently, the available commercial GaN bidirectional switch are rated for up to 650 V [13], [14] or lower voltages [15], and other companies [16] are doing research in the 650 V application range. Literature results show dual-gate GaN BDS with breakdown voltage high enough for 1200 V rating when fabricated on sapphire substrates [17], whereas when Si substrates are used, the breakdown voltage reaches up to ~1350 V, which is suitable for 650 V applications [9], [18], [19]. Research has also been done on reverse-blocking HEMTs (RB-HEMTs), which allows to realize a BDS by combining two in anti-parallel configuration [20], [21], [22]. They can reach breakdown voltages of up to 3 kV, however, they introduce a turn-on voltage offset due to the built-in diode, and limit the specific ON-resistance ($R_{ON,sp}$) as two of them are required to form a BDS.

In our previous work, we presented a 650 V dual-gate p-GaN BDS fabricated on a 200 mm GaN-on-SOI substrate, with breakdown voltage up to ±1.1 kV, limited by the buffer breakdown [9]. Given the promising results of that architecture, we made a different choice of substrate to overcome the previous limitations and target 1200 V operation, while still using large diameter substrates, that makes the technology commercially viable.

In the current work, we demonstrate a dual-gate bidirectional switch rated for 1200 V application, based on a p-GaN gate E-mode HEMT which has been fabricated with several design geometry variations using imec's GaN discrete process flow on a 1200 V ready substrate on QST® (Qromis Substrate Technology) [23], [24], [25]. The devices have been characterized on-wafer in all 4 conduction modes. The devices have been brought to hard breakdown in both positive and negative bias, demonstrating the OFF-state behaviour for both polarities. Furthermore, they have been evaluated by means of reverse bias stress at ±1200 V, to have preliminary reliability results at the rated voltage.

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II. Device under test

Si substrates are the most common choice of substrate for GaN technology, due to their well-established production process and low cost. However, the thick buffer layers that are required for 1200 V applications makes the wafer physically fragile and device processing very challenging due to the risk of wafer breakage. Alternative choices are SiC, sapphire or QST® substrates. SiC was not considered due to the high cost, which makes it difficult to use in commercial applications. QST® was preferred over sapphire as the substrate diameter can be scaled up to 300 mm, it can be used in a CMOS compatible cleanroom and its core has a coefficient of thermal expansion matched to GaN. [26]

The GaN epitaxial structure and the discrete process flow are developed and fabricated at imec. The epitaxial layer is grown with metal-organic chemical vapor deposition (MOCVD) on a 200 mm QST® substrate, including an AlN nucleation layer, two superlattice layers, a GaN:C layer, a 200 nm GaN channel layer, a 14 nm AlGaN barrier layer and an 80 nm p-GaN layer. The buffer schematic is shown in Fig. 1(a).

The device fabrication starts with the patterning of the p-GaN layer and the deposition of the gate metal for the formation of the gate contacts and the first field-plate (FP). Next, source contacts are formed by opening the oxide layer and depositing the ohmic metal, also forming the second FP. The ohmic metal is annealed subsequently to form an ohmic contact to the two-dimensional electron gas (2DEG). Afterwards, two additional source-connected FPs are formed, separated by SiO_2 inter-metal dielectrics (IMDs). All the field-plates are extended equally from both sources, yielding a symmetrical field plate configuration. Additionally, contact is made to the Si(111) layer in the substrate by creating a deep via from the front side. Contrary to imec's GaN-IC process flow, no planarization is processed in this flow below the power metal layer. Finally, a Si_3N_4 layer is deposited to cover the device, and openings are made to access the metal pads that connect the source and gate contacts. A schematic cross-section of the device is shown in figure Fig. 1(b). The starting gate-to-gate distance L_{GG} is equal to 22 µm, given the promising results obtained in [9], and it is scaled down to 10 µm. Several field-plate combinations have been tested for each value of L_{GG}, and the combination is indicated as $L_{G1FP,M0}/L_{G1FP,OM}/L_{G1FP,M1}/L_{G1FP,M2}$ to indicate the extension of Metal0, Ohmic-Metal, Metal1 and Metal2 field-plates from the previous one, respectively (for the source 1/gate 1 side, similarly for the source 2/gate 2 side). Due to the necessity of reaching high voltage operation in both directions, the gate and source field-plates are designed equally on both sides.

The device under test (DUT) has two gates which must be biased to their respective sources: source 1 for gate 1 and source 2 for gate 2, as shown in Fig. 1(c). The substrate (B) is internally shorted to source 1.

In a unidirectional HEMT, the substrate potential is typically tied to the source because it represents the lowest potential terminal. In a BDS, however, each source may be connected to a high voltage, which creates several options for managing the substrate:

- The substrate can be left floating.
- The substrate can be connected to one of the sources (as implemented in this work).
- The substrate potential can be set to the minimum of the two source voltages using a substrate bias managing circuit.

Utilizing a floating substrate is not recommended, as it can lead to operational instabilities during switching. Implementing a substrate management circuit (SMC) to fix the substrate potential at the lowest of the two source potentials [27] would be optimal, enabling a perfectly symmetric device. Nevertheless, this approach necessitates further investigation and the integration of additional components, which may increase design complexity and potentially affect device area and reliability. Alternatively, setting the substrate potential equal to one source offers a simpler design solution. The trade-off is structural asymmetry, which requires testing the device in both polarities to guarantee reliable bidirectional operation under all conditions. As a consequence, to test the bidirectional operation of our device, in one case (for one polarity), the source 2 is set to high-voltage with source 1 and substrate at zero volt – as would be the case for a structure without the source connected to the substrate. Yet for the second case (for the other polarity), where source 1 is set to high-voltage and thus also the substrate in our case, we need to perform a second test. This can be done by applying a negative HV to source 2 with source 1 (and the substrate) at 0 V. Indeed, this is equivalent to applying a positive HV to source 1 (and thus also the substrate in our case) and 0 V to source 2, since only the differential potentials inside the device matter, and allows to use the same setup for both polarities, as explained in the next section.

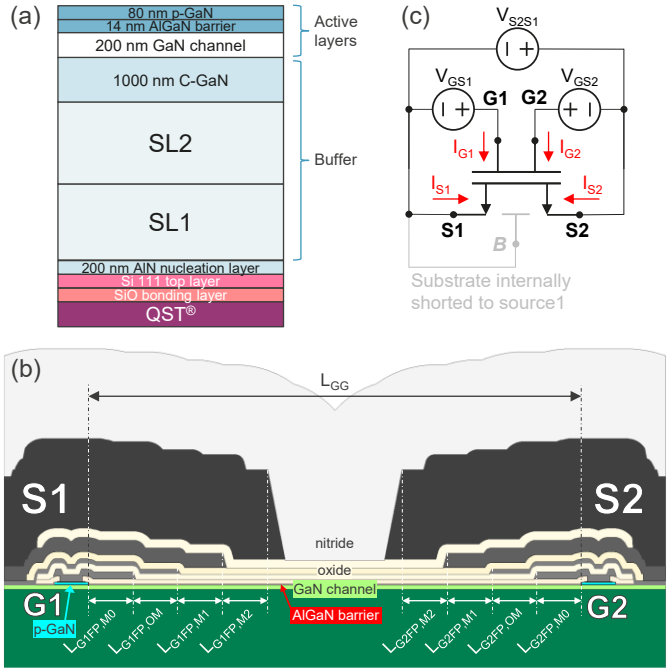

Fig. 1. (a) schematic of the GaN buffer on QST® substrate, (b) cross-section schematic of the DUT up to the GaN buffer and (c) bias scheme of a dual-gate BDS.

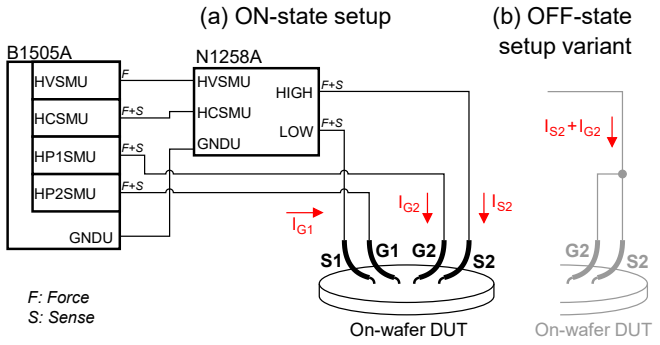

Fig. 2. Schematic of the test setup used for DC characterization in (a) ON-state and diode modes and (b) OFF-state, with shorted source 2 and gate 2.

A. Test methodology

The devices have been tested on-wafer using the DC setup that we presented in [9] and shown in Fig. 2. A Keysight B1505A with one HVSMU, one HCSMU, two HPSMUs and a MFCMU is used, connecting the devices via four manipulators, two with standard triaxial connectors on the low-voltage side (source 1 and gate 1) and two with SHV connectors on the high-voltage side (source 2 and gate 2). V_{GS1} is controlled via the HP1SMU, whereas V_{GS2} is set by sweeping the HP2SMU in sync with the HVSMU/HCSMU with an offset equal to V_{GS2}. All four conduction modes are tested: ON-state and diode modes using the ON-state setup, and OFF-state using the OFF-state setup.

In OFF-state both source 2 and gate 2 must be brought to HV, therefore they are shorted, ensuring $V_{G2S2} = 0$ V, but preventing to measure the two currents separately. For this reason only the sum of the two currents is reported in OFF-state, which still provide a good indication of the leakage level and the breakdown voltage. The use of Fluorinert™ FC-70 was required during HV measurements to avoid flashover.

Afterwards, reverse bias stress tests are conducted on several devices, applying a V_{S2S1} voltage of ±1200 V in OFF-state for 500 s, with a pre and post characterization phases consisting of:

1. An I_{S2}-V_{GS1} measurement at $V_{S2S1} = 0.1$ V, to check the ON-state operation of the device and extract the ON-resistance R_{ON} at $V_{GS1} = 7$ V;
2. An I_{S2}-V_{S2S1} OFF-state sweep from 0 V to ±1200 V to ensure that the device can reach the target voltage;
3. A second I_{S2}-V_{GS1} measurement at $V_{S2S1} = 0.1$ V to check that the device is still functional after the OFF-state sweep.

To execute the full sequence of measurements, the setup needs to be changed between the ON-state and the HV OFF-state measurements, as gate 2 must be shorted to source 2 during HV bias. Due to the number of devices under test and the requirement of switching setup for ON- and OFF-state measurements, the reverse bias stress is limited to 500 s per device, which provides a preliminary insight into the reliability of these devices. The test is considered passed when all measurements are terminated without failure of the DUT.

The use of Fluorinert™ excludes the reverse bias stress test at high temperatures, due to the highly decreased evaporation time. The test is therefore conducted at room temperature.

III. Results and Discussion

The different design variations have been tested in OFF-state until breakdown. Devices with $L_{GG} \leq 16$ µm do not meet the 1200 V target voltage, probably due to the small distance between the top field-plates (of about 2 µm in all cases) that cause a failure in the nitride passivation. Devices with $L_{GG} \geq 18$ µm are capable of high voltage OFF-state operation, with breakdown voltages (V_{BD}) from 1700 V. The upper limit is determined by the buffer, that can reach ~2200 V and ~ -2500 V in positive and negative bias respectively. The breakdown voltage results for devices with $L_{GG} = 22$ µm (the starting value) and $L_{GG} = 18$ µm (the minimum that allows to meet the target voltage) are shown in Fig. 3 for positive and negative bias, where 5 devices per design split are tested up to failure. It can be noted that the breakdown voltage is the same for both L_{GG} values and depends on the field-plate configuration: for the tested variations, the shorter the field-plates, the higher the breakdown voltage. This is a result in line with the results found in our previous work [9] for a 650 V dual-gate bidirectional switch and it means that the FP configuration can be further optimized to work with shorter L_{GG}. It can be noted that the Metal2 FP is not required in order to achieve high breakdown voltage, and 3 field-plates are actually enough to guarantee $V_{BD} > 2$ kV. In reverse bias, the scaling of breakdown voltage with shorter field-plates is more evident thanks to the higher breakdown voltage of the substate. The leakage current at ±1200 V for the tested design variations is reported in Fig. 4. It can be seen that the leakage value does not vary significantly for the different L_{GG}, but rather increases with shorter FP configurations. This is because with shorter FP, the higher electric field at the gate2 side yields to a higher electron density in the 2DEG [9]. In all cases, the leakage current is lower than 10 µA/mm in both directions.

The I_{S2}-V_{S2S1} measurement in OFF-state, equivalent to the I_D-V_{DS} for the traditional HEMT, for the device with $L_{GG} = 18$ µm and $L_{FP} = 0.5/1/2/0$ µm is shown in Fig. 5, showing its leakage current in both bias conditions. As discussed above, due to limitations of the test setup only the sum of the source 2 and gate 2 currents can be measured. The leakage current remains always below ~3 µA/mm, and the leakage starts increasing significantly only above about ±2 kV. The difference between the positive and negative bias leakages is caused by the asymmetric vertical leakage of the buffer. The buffer is made of several layers of different materials, which yield to many interfaces. Asymmetric behavior with voltages of opposite polarities is therefore expected. It has been engineered to be symmetric up to the rated voltage of ±1200 V, with margin until 1600 V.

The I_{S2}-V_{S2S1} measurements in bidirectional ON-state (with both gates ON, i.e. $V_{GS} = 7$ V referred to their respective sources), as well as in diode modes (i.e., gate 1 OFF and gate 2 ON or vice-versa), are shown in Fig. 6. In ON-state, the devices exhibited a symmetrical behavior and yield an R_{ON} of 15 Ωmm for both positive and negative V_{S2S1}. In diode modes, the current can only flow in one direction, with an R_{ON} at the point of maximum output conductance (g_{out}) of 30 Ωmm. Both diode modes present a voltage offset of about 2.5 V, required to turn ON the half of the device that has the gate in OFF-state.

The ON-resistance is extracted for all the design variations that have been tested in ON-state and diode modes, and the results are shown in Fig. 7. It can be seen that the R_{ON} scales well with the gate-to-gate distance, whereas in ON-state is always about half than in diode mode. This proves that a shorter L_{GG} is preferred, whenever possible, to minimize the resistance (and therefore the power consumption) during ON-state operation. The broader distribution of the R_{ON} extracted in diode mode is probably caused by the extraction method. In ON-state it can be extracted at V_{S2S1} = 0.1V, as the device is immediately ON for V_{S2S1} > 0V similarly to the HEMT; in diode mode the V_{S2S1} at which the device turns ON is not known in advance, and it is therefore extracted at the point of maximum output conductance.

The devices exhibit a typical threshold voltage (V_{TH}) of 2.0 V (calculated at the intercept of the I_{S2}-V_{GS1} slope at the maximum transconductance g_m with the x-axis) for both gates. It is equal to the threshold voltage of the standard HEMT and it is independent of the different design variations that have been studied.

The best performing switch among the proposed devices has been compared with the state-of-the-art GaN BDS fabricated on Si [7], [18], [28], [29], SOI [9] and sapphire [17] substrates, and the specific ON-resistance ($R_{ON,sp}$) versus V_{BD} is reported in Fig. 8. RB-HEMTs fabricated on Si [21], [30], sapphire [20], [31] and SiC [32] have also been considered for this comparison, as two of them can be monolithically integrated in anti-parallel configuration to make a single BDS. To keep a fair comparison, their $R_{ON,sp}$ has been multiplied by 2 to take into account the area required for the two devices and the fact that only one will conduct the current at the same time. The device presented in this work shows higher performance than BDS realized with two discrete devices and proves to be among the best performing solutions in literature. Performance limit lines for BDS realized with two discrete components in Si, SiC and GaN are also estimated as

$$R_{ON} \propto \frac{4V_{BD}}{\mu\epsilon E_{crit}^3} \quad (1)$$

where μ, ϵ and E_{crit} are respectively the permeability, the permittivity and the critical electric field of the materials [2]. The theoretical limit of GaN can be surpassed by a dual-gate BDS because it is calculated considering a unilateral and abrupt junction, where the electric field has a triangular shape, which is not the case here. [17]

Finally, reverse bias stress tests have also been carried out to have preliminary reliability results on the DUTs. Ten devices have been tested per design split, five at 1200 V and five at -21200 V for 500 s, which all passed the test. The leakage currents during the stress tests were monitored and are shown in Fig. 9(a) for a 1200 V stress test. The tests that are conducted at -1200 V show similar device performance. In Fig. 9(b) and Fig. 9(c) the ON-state I_{S2}-V_{GS1} and the OFF-state I_{S2}-V_{S2S1} are depicted respectively, before and after the stress test, showing a small R_{ON} reduction and almost no impact to the OFF-state current.

The R_{ON} degradation due to the stress has been calculated from the ON-resistance measured before the stress ($R_{ON,pre}$) and after the stress ($R_{ON,post}$) as

$$R_{ON}\ \text{degradation}\ (\%) = \frac{R_{ON,\text{post}} - R_{ON,\text{pre}}}{R_{ON,\text{pre}}} \times 100 \quad (2)$$

and the results for the design variations considered in this paper are shown in Fig. 10. All the devices show an R_{ON} degradation lower than 20% in most cases, with most of them having no significant degradation and there are no significant differences between the devices with longer and shorter L_{GG}, nor do the field-plate configurations play a role in this test. This again proves that L_{GG} = 18 µm and 3 field-plates can be a good design choice for a dual-gate BDS, although the results might be affected by the limited test conditions (500 s stress at room temperature). This initial assessment of the devices reliability exhibits good results, however, further studies are required to fully prove the device reliability, such as a full HTRB analysis, once the technical limitations of performing high-voltage stresses at high-temperature on-wafer will be overcome.

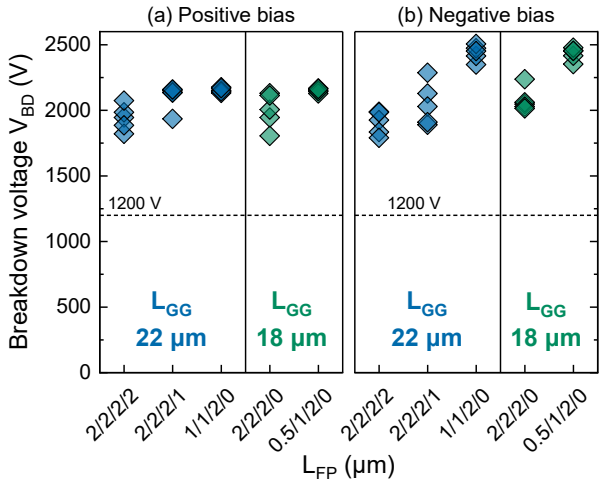

Fig. 3. Hard-breakdown voltages for (a) positive and (b) negative bias of the DUT for 5 design variations. 5 devices per design split and bias side are measured.

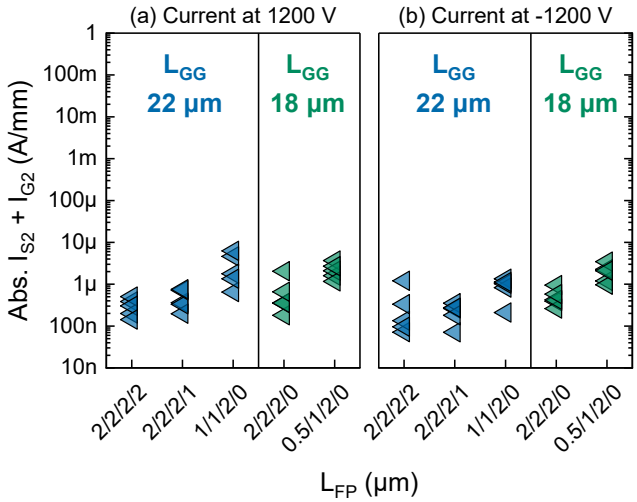

Fig. 4. Leakage current in OFF-state at (a) 1200 V and (b) -1200 V of the DUT for 5 design variations. 5 devices per design split and bias side are measured.

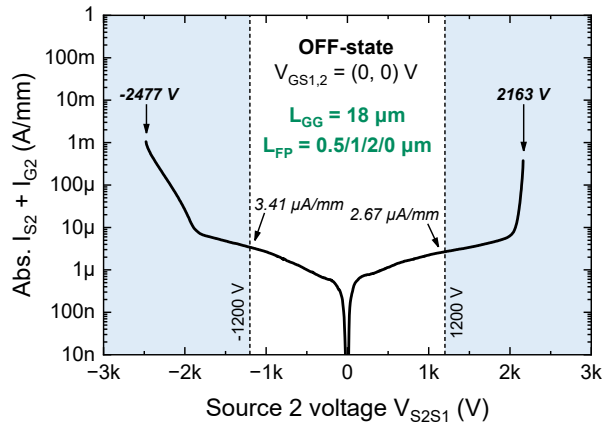

Fig. 5. I_{S2}-V_{S2S1} measurement in bidirectional OFF-state until hard-breakdown of the device with L_{GG} = 18 µm and L_{FP} = 0.5/1/2/0 µm in both positive and negative bias.

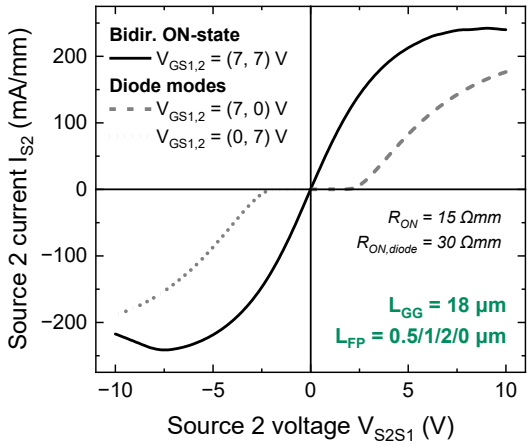

Fig. 6. I_{S2}-V_{S2S1} measurement in bidirectional ON-state (both gates ON) and diode mode (only one gate ON at the time) of the device with L_{GG} = 18 µm and L_{FP} = 0.5/1/2/0 µm.

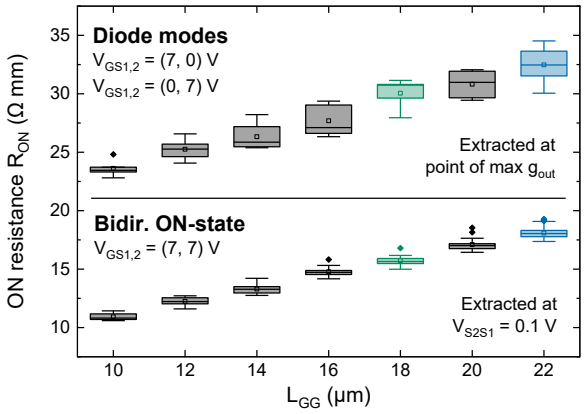

Fig. 7. ON-state resistance extracted for the different design variations in bidirectional ON-state and forward and reverse diode modes. The different field-plate configurations do not have impact on the ON-resistance and are grouped for the same L_{GG}. R_{ON} for L_{GG} = 18 µm and 22 µm are colored in green and blue respectively.

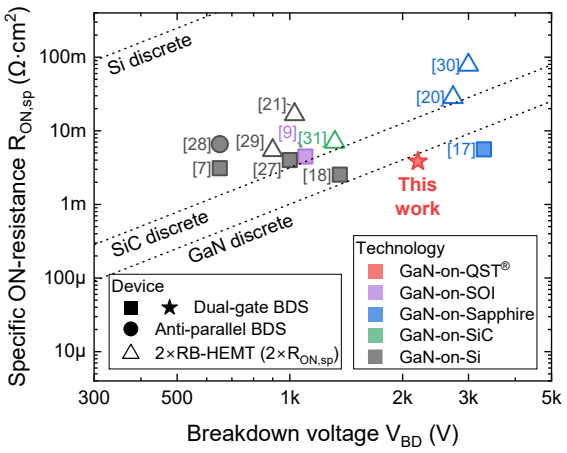

Fig. 8. Benchmark of the specific ON-resistance ($R_{ON,sp}$) versus breakdown voltage (V_{BD}) for GaN BDS. Works on RB-HEMTs are also considered, and twice the reported $R_{ON,sp}$ has been considered, as two of them are required to make a BDS. Performance limits are indicated for BDS realized with discrete components in Si, SiC and GaN.

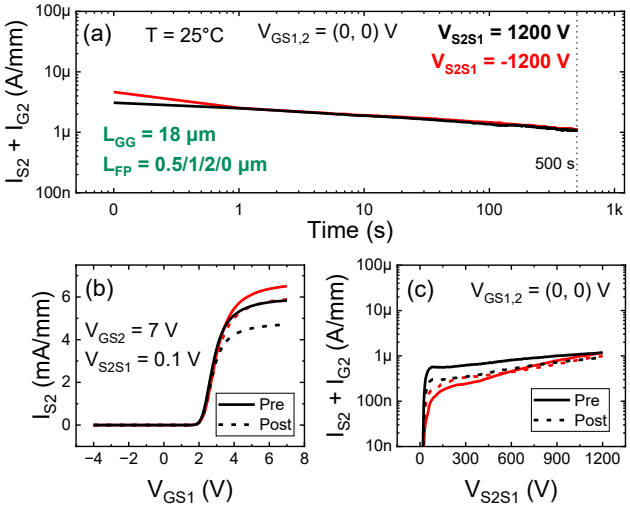

Fig. 9. (a) Leakage currents during a 500 s reverse bias stress test at room temperature. (b) I_{S2}-V_{GS1} ON-state measurement and (c) I_{S2}-V_{S2S1} OFF-state sweep before and after the stress test are reported.

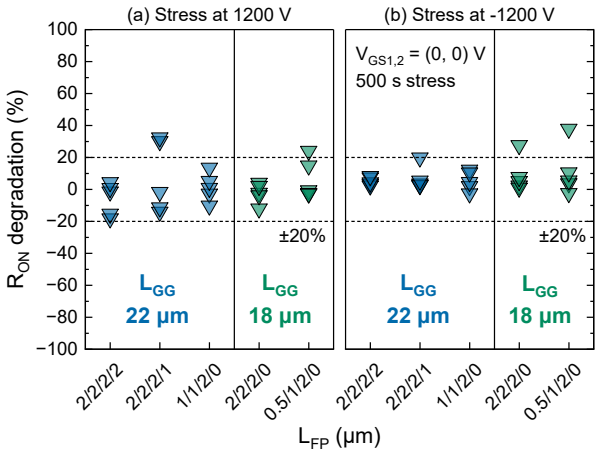

Fig. 10. ON-resistance degradation after 500 s stress at (a) 1200 V and (b) -1200 V in OFF-state for different design variations.

IV. Conclusion

We presented dual-gate p-GaN gate bidirectional switches fabricated on a 200mm GaN-on-QST substrate that are suitable for 1200 V OFF-state operation.

Several design variations have been studied and devices with L_{GG} down to 18 µm and a 3 field-plate design show the best electrical performance in ON-state DC operation, while still being able to operate at ±1200 V, with a breakdown voltage much higher than the rated voltage. Benchmark with the current state-of-the-art works in literature shows that these switches are among the best performing solutions. Preliminary reliability tests were conducted that showed promising results and no difference between a 3 and 4 field-plates design.

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