Complementary Field-Effect Transistors (CFET): Metrology Challenges and Solutions

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INTRODUCTION

While the industry is transitioning from Fin Field-Effect Transistors (FETs) to nanosheet (NSH) FETs, heavy research is already being carried out to define the next transistor architecture which will allow even more functionality from the same Si area. Complementary FETs (CFETs), whereby two n- and p-NSH transistors are stacked on top of each other, seem to reach a broad consensus [1-3]. Similarly, their monolithic integration, i.e. from a single piece of Si, also appears to be the industry's preferred route. However, monolithic CFET integration comes with an unprecedented level of complexity, which makes metrology and inspection more critical but also more challenging.

In this contribution, we start with a summary of the metrology challenges implied by the complexity of monolithic CFET integration. We then investigate the solution space and highlight existing inline metrology techniques which have the potential to solve CFET's needs. Finally, we demonstrate the concrete use of some of these techniques. We conclude that, although many capabilities remain to be demonstrated, the solution space is broad such that CFET metrology is not expected to suffer from a *capability gap.* However, we foresee a heavier resort to slower solutions, which is likely to lead to a *throughput* or *capacity gap*.

METROLOGY NEEDS

Compared to NSH transistors, the complexity of monolithic CFET integration comes from (i) the aspect ratio of these devices, (ii) the requirement of a middle dielectric isolation (MDI) between the top and bottom devices and (iii) the separate integration of the top and bottom devices. Metrology will therefore be needed to control these new processing challenges. The most critical metrology capabilities required for control of monolithic CFET integration are summarized in Fig. 1.

In a nutshell, complex material characterization is required for the complex blanket SiGe/Si multilayer and for the gate stack [Fig 1(a)]. Lateral and vertical control is necessary after the vertical fin and gate etches [Fig 1(b)]. The necessary and complex control of lateral etches is amplified by the presence of 2 SiGe materials with different Ge concentrations and a higher aspect ratio [Fig. 1(c)]. Lateral control will also be needed if a cover spacer is used to integrate the top and bottom devices separately. Finally, vertical control is required after the numerous steps of material fill and etch back, e.g. SiO_2 and Metal0 [Fig. 1(d)].

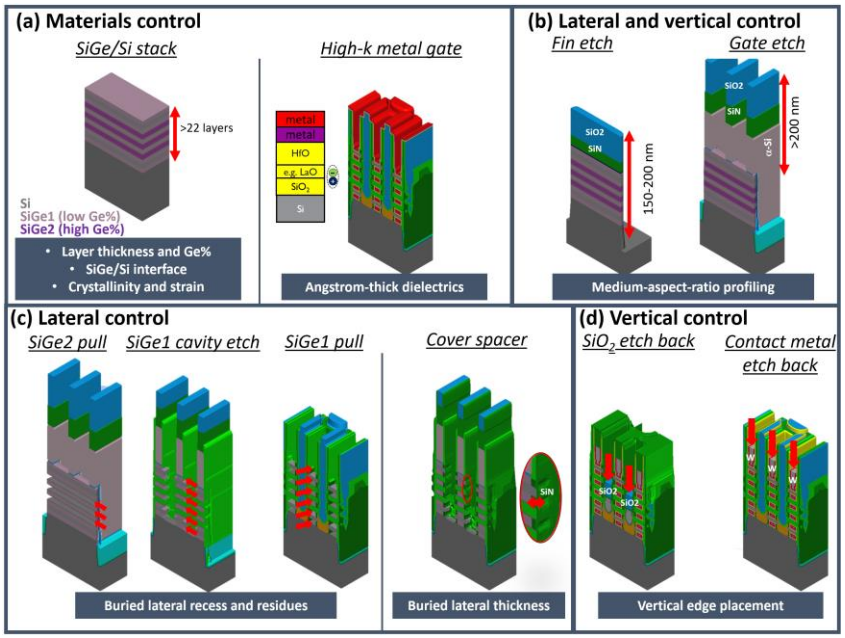

FIGURE 1. Summary of metrology challenges for monolithic CFET integration

METROLOGY SOLUTIONS

Since most of the challenges presented in Fig. 1 require the extraction of information buried deep inside the structure, CFET metrology inherently belongs to the field of 3D metrology. Building on our earlier work focused on 3D logic, 3D memory and 3D interconnects [4], we propose to map the solution space for CFET metrology along two main axes, i.e. lateral resolution and probing depth (Fig. 2). Given the nanometer-scale of CFET devices and their medium aspect ratio, relevant metrology solutions for monolithic CFET integration belong to the bottom left corner indicated by a dotted box.

In the rest of this contribution, we move from the global and strategic evaluation of CFET metrology to concrete demonstrations of the capabilities of a few technologies, i.e. Optical Critical Dimension (OCD) scatterometry, EUV scatterometry/reflectometry or X-ray Fluorescence (XRF) etc, to solve the needs highlighted in Fig. 1.

Our general conclusion is that solutions exist to solve most CFET metrology challenges. However, in too many instances, slow options have to be opted for, which compromises either the speed of the feedback or the level of control. We therefore recommend more focus on a third axis, i.e. the throughput (color scale of Fig. 2), by means of both software and hardware optimizations.

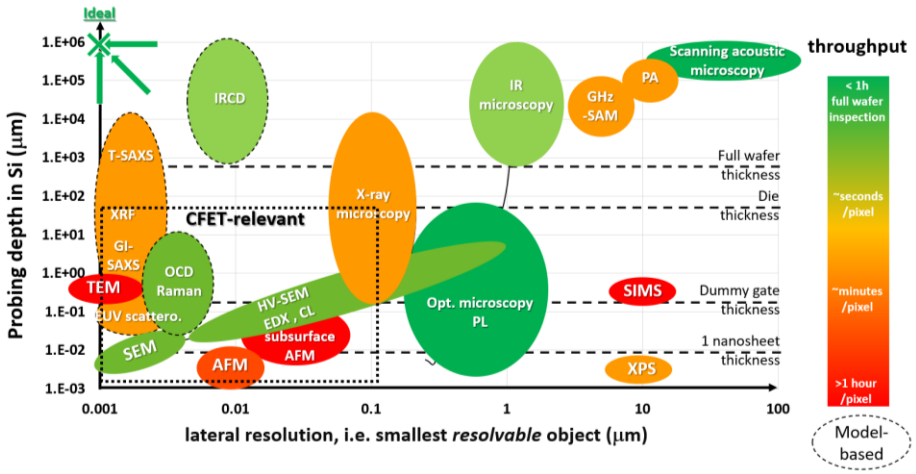

FIGURE 2. 3D metrology landscape and solutions relevant to CFET metrology

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KEYWORDS

CFET, gate all around, 3D metrology