DLTS assessment of grown-in defects in hetero-epitaxial gate stacks for stacked silicon nanosheet channels

E. Simoen[1], S. Khelifi[1], H. Vrielinck[1], A. Akula[2] and R. Loo[1,2]

[1] *Ghent University, Depart. Of Solid State Sciences, Krijgslaan 281 S1, B-9000, Gent, Belgium*
[2] *Imec, Kapeldreef 75, B-3001, Leuven, Belgium*
eddy.simoen@ugent.be

The fabrication of state-of-the-art Gate-All-Around (GAA) silicon nanosheet transistors usually relies on the hetero-epitaxial growth of Si/SiGe structures, like in Fig. 1. Such a stack is formed by Chemical Vapor Deposition (CVD) in an epi reactor using higher order precursors and temperatures ≤ 500°C [1]. This allowed the required two-dimensional epitaxial growth of smooth, fully strained SiGe/Si multi-stacks with Ge concentrations up to 50%. However, the low growth temperature results in an extremely long process duration and a concern for the incorporation of point defects in the active layers of the device. Improvements in the post-epi fabrication, especially the selective removal of SiGe, allow to reduce the Ge concentrations in the multi-stack. This opened the door to consider conventional process gases and higher growth temperatures for the epitaxial growth. The aim of the present work is to investigate the quality of these CVD gate stacks by Deep-Level Transient Spectroscopy (DLTS), probing electrically active defects and comparing high- and low-temperature deposited layers. The undoped epi-layers have been grown on 300 mm highly P-doped silicon wafers to a total thickness of around 107 nm. Al Schottky contacts have been evaporated on a wafer fragment enabling Capacitance-Voltage (C-V) measurements as shown in Fig. 2. Two distinct regions can be discerned in the bias range from V_R=-2 V to 0 V, corresponding with a different free carrier density in the n+ substrate and the SiGe/Si stack. It also defines the bias pulse voltages (V_R to V_P) for DLTS measurements, distinguishing the substrate region from the SiGe/Si hetero layers.

DLTS has been performed for a typical pulse period t_w of 51.2 ms and a filling pulse duration t_p of 100 μs. In the high-temperature sample, a clear electron trap peak is observed that shifts with the bias pulse towards lower peak position, when probing closer to the sample surface (Fig. 3). The corresponding Arrhenius plots in Fig. 4 confirm the reduction of the activation energy when probing closer to the sample surface. The change in the activation energy with probing depth could indicate a different local composition, as has been found previously for radiation-induced defects in relaxed Si_xGe_{1-x} with different composition x [2,3]. The nature of the observed point defects could be related to vacancy complexes, like, e.g., the E centre or P-V pair [4]. On the other hand, for the low-temperature sample in Fig. 5 a single broad peak is found when pulsing the gate stack region, while no detectable signal results from the silicon substrate. At the same time, logarithmic trap filling is found for the broad electron trap in Fig. 5, suggesting that extended defects (i.e., misfit and threading dislocations) are present in the low-T epi stack. This is confirmed by the results of Photoluminescence (PL) spectroscopy [1], demonstrating a partial relaxation of the low-T gate stacks.

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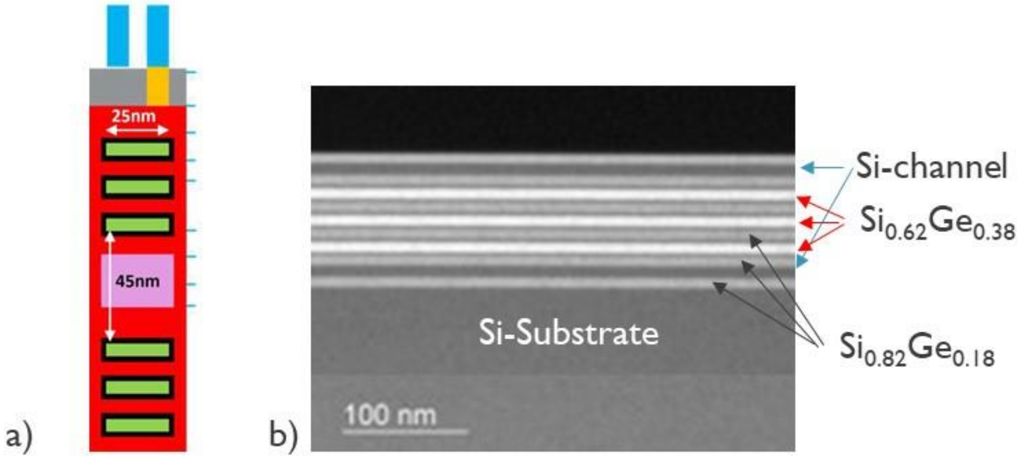

Fig. 1. Gate cross sections of a CFET Scheme and b) TEM image of a typical epi-stack used to fabricate CFET devices.

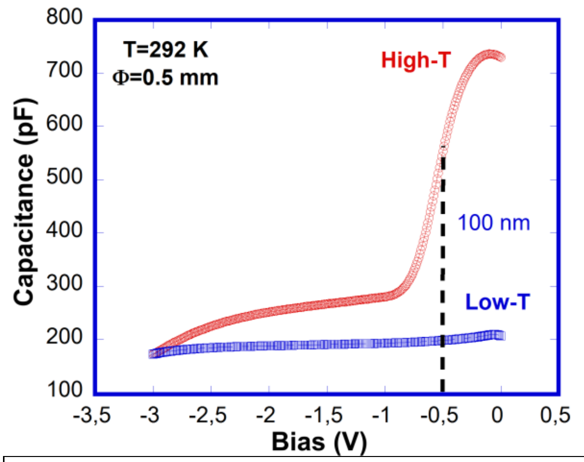

Fig. 2. Capacitance versus bias of a 0.5 mm diameter Al Schottky barrier on a low- and a high-temperature epi stack.

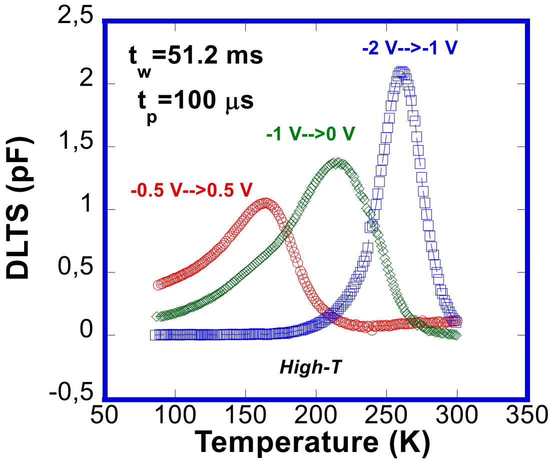

Fig. 3. DLTS spectrum of a high-temperature sample at different bias pulses. The pulse duration t_p=100 μs and the pulse period t_w=51.2 ms.

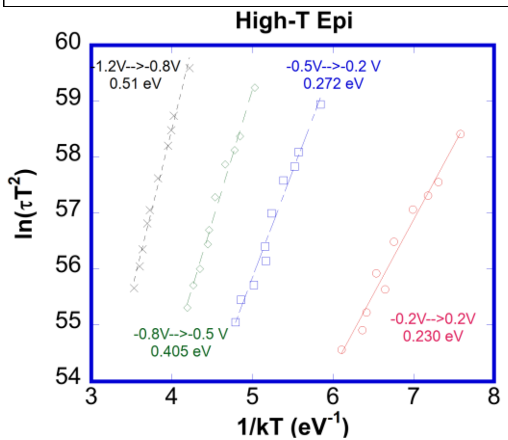

Fig. 4. Arrhenius plot of the high-temperature epi sample of Fig. 3, for different bias pulses.

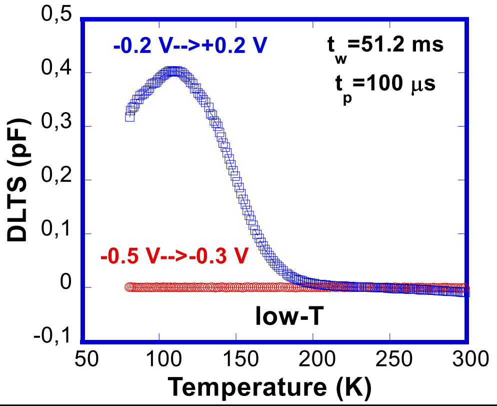

Fig. 5. DLTS of a low-temperature sample at different bias pulses. The pulse duration t_p=100 ms and the pulse period t_w=51.2 ms.