ECS Journal of Solid State Science and Technology

Epitaxial Si/SiGe Multi-Stacks: From Stacked Nano-Sheet to Fork-Sheet and CFET Devices

To cite this article: R. Loo *et al* 2025 *ECS J. Solid State Sci. Technol.* **14** 015003

ECS Journal of Solid State Science and Technology, 2025 **14** 015003

Epitaxial Si/SiGe Multi-Stacks: From Stacked Nano-Sheet to Fork-Sheet and CFET Devices

R. Loo,[1,2,*,z] A. Akula,[1] Y. Shimura,[1] C. Porret,[1] E. Rosseel,[1,*] T. Dursap,[1] A. Y. Hikavyy,[1,a] M. Beggiato,[1] J. Bogdanowicz,[1,*] A. Merkulov,[1] M. Ayyad,[1] H. Han,[1] O. Richard,[1] A. Impagnatiello,[1] D. Wang,[3] K. Yamamoto,[3,*] T. Sipőcz,[4] Á. Kerekes,[4] H. Mertens,[1] N. Horiguchi,[1] and R. Langer[1]

[1]*Imec, Kapeldreef 75, 3001 Leuven, Belgium*
[2]*Ghent University, Department of Solid-State Sciences, Krijgslaan 281, 9000 Ghent, Belgium*
[3]*Faculty of Engineering Sciences, Kyushu University, 6-1 Kasuga-koen, Kasuga, Fukuoka, Japan*
[4]*Semilab Semiconductor Physics Laboratory Co. Ltd, Prielle Kornélia u. 2. H-1117 Budapest, Hungary*

After a short description of the evolution of metal-oxide-semiconductor device architectures and the corresponding requirements on epitaxial growth processes, the manuscript describes the material properties of complicated Si/SiGe multi-layer stacks used for complementary field effect transistor (CFET) devices. They contain two different Ge concentrations and have been grown using conventional process gases. A relatively high growth temperature is used to obtain acceptable Si and SiGe growth rates. Still island growth has been suppressed for Ge concentrations up to 40%. Excellent structural and optical material properties of the Si/SiGe multi-layer stack will be reported, with up to 3 + 3 Si channels in the top and bottom part of the stack, respectively. The absence/presence of lattice defects has also been verified by room-temperature photoluminescence measurements. Photoluminescence measurements at low temperatures are used to study band-to-band luminescence from individual sub-layers and to illustrate the optical material quality of the CFET stack.
 [DOI: 10.1149/2162-8777/ada79f]

Manuscript submitted October 23, 2024; revised manuscript received December 23, 2024. Published January 20, 2025.

The scaling evolution from stacked nano-sheet devices to fork-sheet devices and complementary field effect transistor (CFET) architectures went together with increased complexities of the epitaxial growth schemes (Fig. 1). This is valid for both the Si/SiGe multi-layers, which define the thickness of the nano-sheet channels as well as the vertical distance between individual nano-sheets, and for the epitaxially grown source/drain (SD) layers which require a continuous increase in active doping concentration and a reduction in thermal budget without compromising material quality.

Fork-sheet transistors are lateral nano-sheet devices with a forked gate structure (Fig. 1c).[1,2] The physical separation of n- and p-devices by a dielectric wall enables device scaling and, consequently, sheet width maximization within the limited footprint of low-track-height standard cells. Bottom dielectric isolation has been proposed to circumvent the junction isolation trade-off between punch-through suppression on the one hand and junction leakage and capacitance on the other hand.[3] A typical fabrication scheme includes the challenging epitaxial growth of fully strained $Si/Si_{1-y}Ge_y$/multi-$\{Si_{1-x}Ge_x/Si\}$ epi stacks ($y > x$) where the bottom Ge-rich $Si_{1-y}Ge_y$ layer is later replaced by a SiN/SiCO isolation.[4,5]

In the CFET architecture, N- and P-MOS devices are placed on top of each other, thus completely removing the area consumption by the N-P spacing. This allows for further maximizing the effective channel width and, hence, the drive current.[6–12] The architecture can be fabricated following either a monolithic or a sequential approach. In the first option, N- and P-MOS transistors are built on the same wafer, while the sequential fabrication flow is based on wafer-to-wafer bonding techniques. The strengths and challenges of both approaches are discussed in Ref. 9. In the monolithic approach, device fabrication starts with the epitaxial growth of an even more complicated Si/SiGe multi-stack with two different Ge concentrations (Fig. 2),[9,12,13] and where Ge-rich $Si_{1-y}Ge_y$ layers are later replaced by isolating dielectrics forming a so-called middle dielectric isolation (MDI).[9,12] Owing to the very small dimensions (e.g., sub-10 nm nano-sheet channel width), high etching selectivity of the $Si_{1-y}Ge_y$ layers towards both $Si_{1-x}Ge_x$ and Si, and excellent process controls are mandatory. This sets stringent requirements on the epitaxial layer stacks (thicknesses and composition control, sharpness of interfaces, and absence of strain relaxation)[4,5,13,14] as well as on the $Si_{1-y}Ge_y$ etch process (high selectivity and limited consumption of $Si_{1-x}Ge_x$ and Si).[14–17]

High performance metal / SD junctions are key to alleviate scaling-related contact issues in these devices.[18] Selective epitaxial growth (SEG) processes yielding heavy active doping are therefore required, in addition to introducing innovative contact materials and designs.[19–21] The resulting electrical performance is, however, restricted by doping solubility limits and loading effects (impact of substrate patterning) inherent to scaling. Those must be circumvented to enable the upcoming generations of components. Moreover, novel device architectures add stringent constraints regarding pre-epi cleaning strategies, thermal budgets, and stability. Changes in how devices are connected are also being introduced into the roadmap. To address both wiring and power delivery bottlenecks, part of the interconnects are being moved to the wafer backside.[21] This backside processing starts with an extreme wafer thinning, for which a thin SiGe etch stop layer is being considered to compensate for within-wafer non-uniformities of the Si substrate removal process.[22–24]

The current work describes the material requirements for the different layers used in monolithic CFET device flows and the progress made on the associated epitaxial growth. The epitaxial growth processes used to deposit $Si/Si_{1-x}Ge_x$ multi-layers for GAA devices (Fig. 1b) is well understood and has been reported in.[25,26] Previous learnings from imec about the selective epitaxial growth of extremely highly doped SD layers as well as the growth against the vertical sidewalls of the nanosheets have been reported in e.g.[19,20,27,28] More recent results are discussed in.[29,30]

Experimental

The epitaxial layers were grown in a production compatible ASM Intrepid® RP-CVD cluster tool. Before layer deposition, the 300 mm Si(001) wafer surface received a conventional wet-chemical clean.

*Electrochemical Society Member.
[a]Present address: Soitec, 922 Parc Technologique des Fontaines, Chem. des Franques, 38190 Bernin, France.
[z]E-mail: roger.loo@imec.be

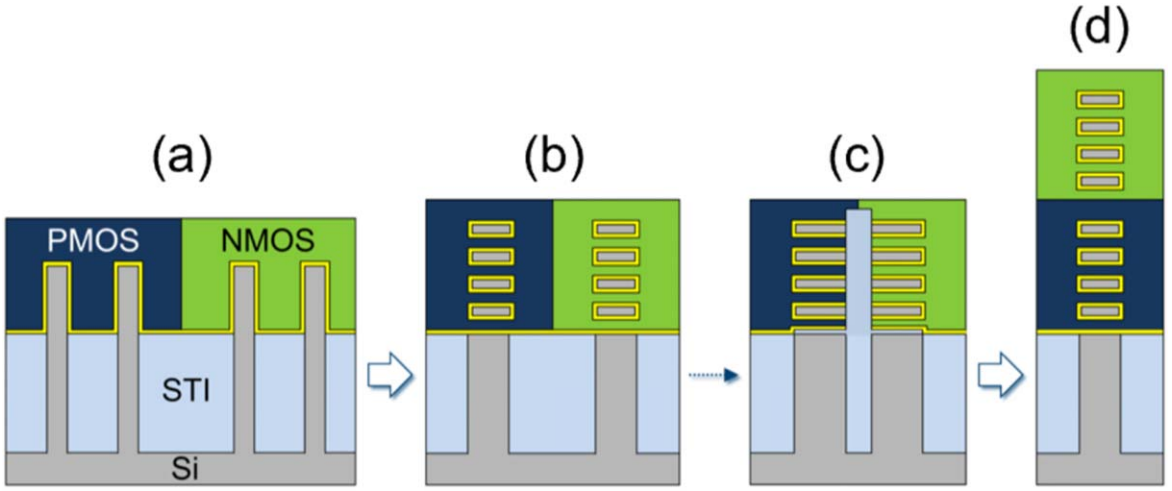

Figure 1. Evolution of MOS device architecture. (a) Triple-gate finFETs are being replaced by (b) gate-all-around (GAA) vertically stacked lateral nano-sheet FETs, which could potentially evolve into (c) the so-called fork-sheet configuration wherein neighboring devices are separated by a dielectric wall. Beyond that, (d) stacking of N/PMOS devices on top of each other in a CFET structure is currently being explored as an attractive concept for ultimate CMOS scaling.

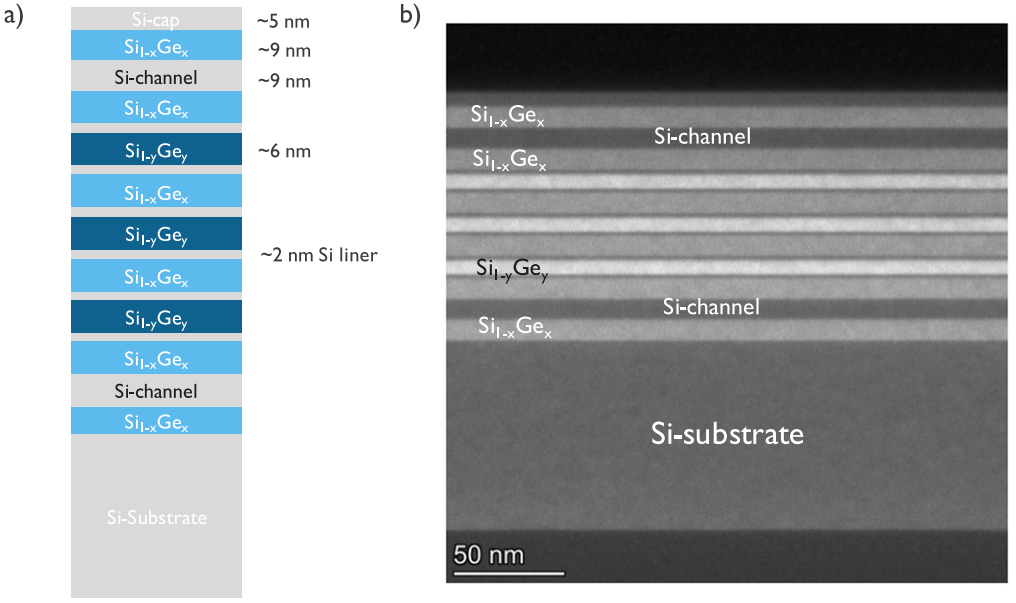

Figure 2. (a) Schematic cross-section and (b) cross sectional HAADF STEM image of a Si/SiGe multi-stack used for CFET devices with one channel for both the p-type and the n-type devices.

Depending on the incoming wafer, the native oxide was either removed *in situ* by a thermal treatment at a sufficiently high temperature (>1000 °C) or by a wet HF clean followed by an *in situ* anneal at 800–900 °C. Careful optimization of the temperature profile within the epi-reactor allows to avoid the formation of slip lines during the pre-epi bake and to deposit epitaxial layers with a uniform thickness over the wafer (relative standard deviation < 1.3%). Epitaxial growth was carried out at reduced pressure using H_2 as carrier gas and conventional precursor gases (SiH_4, SiH_2Cl_2, and GeH_4 (5% diluted in H_2)). The epitaxial layer stack consists of a complicated Si/SiGe multi-stack with two different Ge concentrations (Fig. 2). The $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers with y > x are separated by thin Si layers. After fin patterning, the $Si_{1-y}Ge_y$ layers are replaced by SiN/SiCO.[9,12] The presence of the Si liners prevents vertical etching of $Si_{1-x}Ge_x$ during $Si_{1-y}Ge_y$ removal.[14] A maximum in growth temperature is set by the requirements to enable two dimensional (2D) SiGe layer growth, steep gradients in concentrations at the Si/SiGe and SiGe/Si interfaces, and aiming a defect free and fully strained layer stack without the presence of misfit dislocations.[24,26,31–33] The abruptness of the compositional change at Si/SiGe interfaces is limited by Ge segregation occurring during Si layer growth on the SiGe surface. The most abrupt interfaces have been obtained when using a chlorinated chemistry.[34,35] This sets a preference for using $SiCl_2H_2$ as Si precursor gas. However, in the given temperature range, it provides significantly lower deposition rates compared to SiH_4, especially for the Si-growth.[36,37] The use of SiH_4 as Si precursor gas during Si-growth allows to reduce the growth temperature while still obtaining acceptable growth rates. The higher growth rate at relative low growth temperatures, as obtained when using SiH_4, instead of $SiCl_2H_2$, as Si precursor gas during Si-growth, goes together with an enhanced risk for the incorporation of crystal imperfections during the growth.[38] The formation of these growth imperfections has been avoided by keeping the Si growth rate / SiH_4 partial pressure below a critical value following the procedure described in.[38] The total process duration as required for the deposition of a CFET stack with 2 × 1 channel (2 × 3 channels) at top and bottom, ranges from 25 to 37 min (32 to 49 min), when considering the time between wafer

load and wafer unload. It varies, amongst others, as function of the chosen Ge concentrations in the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers.

A broad range of material characterization techniques have been used to study the epitaxial material properties. For a review of the metrology challenges encountered for GAA structures (including CFET) the reader is referred to the references[39] and Ref. 40. The interface abruptness between two sublayers of the epi-stack has been characterized by e.g. high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM)[41] and soft X-ray reflectometry.[42,43] Room temperature photoluminescence (PL) measurements have been performed using a production compatible EnVision-3000 system from Semilab.[44,45] This inspection system allows for automatic 200/300 mm wafer tests and targets quick, non-contact and non-destructive detection of nm scale PL active buried defects. The Micro-PL measurement, for characterizing optical properties of materials on a micron scale, is based on a high intensity illumination at 532 nm. The detection is carried out at either band-to-band PL, with a peak intensity at 1100 nm (1.127 eV), or at 1400 nm long pass filter PL, 1400-1600 nm (0.89–0.78 eV). Macro-PL applies 808 nm illumination for full wafer mapping. Temperature- (9–300 K) and power-dependent PL measurements, were used to study band-to-band luminescence. A continuous wave laser beam with an excitation wavelength of 532 nm and a spot diameter of ~2 μm creates excitons. Because of the valence band offsets, most excitons are trapped by the SiGe layers and the luminescence from the different layers is collected by a 50x object lens, dispersed by a Horiba LabRAMHR-PL system, and detected by an extended InGaAs array sensor cooled at 180 K.

Results and Discussion

Structural material properties of the CFET stack.—The epitaxial growth temperature has been chosen to be low enough to obtain two dimensional $Si_{1-y}Ge_y$ growth, without three dimensional islands, for single layers as well as for the complete CFET stack with Ge concentrations up to 40% (Fig. 2b). The smooth surface of the resulting CFET stacks is confirmed by both Scanning Electron Microscope (SEM) and surface haze measurements. No larger defects are observed across the wafer surface. Except for the area near the wafer edge, misfit dislocations are avoided by choosing suitable process conditions and taking limitations in layer compositions and individual thicknesses into account. The crystalline defect density, as measured for the layers shown in Fig. 2b, lies indeed below the detection limit of Electron Channeling Contrast Imaging (ECCI), which was in the given case $\sim 1 \times 10^5$ defects/cm^2. Near the wafer edge, misfit dislocations are nevertheless present, because the wafer edge reduces the critical thickness for layer relaxation.[26] The observed layer relaxation cannot be assigned to a non-uniformity in composition, because near the wafer edge, the Ge concentrations of both $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ turned out to be ~1%–1.5% lower. The absence of defects in the inner part of the wafer surface and the presence of misfits near the wafer edge is confirmed by room temperature PL measurements and reflected in the full wafer color map of the Macro-PL intensity (Fig. 3). A reduction of the growth temperature, together with the use of higher order precursors[14,25] might enable to suppress the formation of misfit dislocations at the wafer edge. However, avoiding reactions in the gas phase needs careful attention as it results in the formation of amorphous defects on the wafer surface which, in turn, also can act as nucleation sources for misfit dislocations, despite the lower processing temperature.[46] Suppressing gas phase reactions allows the deposition of similar layers stacks but without the presence of misfit dislocations at the wafer edge as reported by Rengo et al.[47,48] Another option to avoid misfit dislocations at the edge of the wafer is to reduce the lattice mismatch by adding C in the SiGe layers.[49]

The material quality of the layers reported in this work, is further confirmed by X-ray Diffraction (XRD) (Fig. 4a), X-ray Reflectivity (XRR), and XRD Reciprocal Space Maps (RSM) (Fig. 4b). The latter confirms the absence of strain relaxation as the RSM peaks originating from the strained Si/SiGe multi-stack are vertically aligned with the Si-substrate RSM peak. The peaks constituting the omega-2theta (ω-2θ) diffraction spectrum reflect the high material quality. The individual peaks are well resolved, and the spectrum has a low background signal (Fig. 4a). Figure 4c shows an example of the within wafer uniformity of individual layer thicknesses as obtained after optimization of the process settings, especially the optimization of the within wafer uniformity obtained by changing the temperature settings in the reactor, which are controlled by the different thermocouples.

The Ge concentrations in the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers might be adapted in function of the characteristics of the selective etching routines. Keeping the individual layer thicknesses unchanged, critical Ge concentrations exist, above which layer relaxation of the Si/SiGe multi-stack cannot be avoided, also not at the inner part of the wafer. As an example, Fig. 5 compares the XRD ω-2θ scans and plan-view (PV) SEM images of multi-stacks where the $Si_{1-x}Ge_x$ layers contain either 18% Ge (top figures) or 24% Ge (bottom figures) while the $Si_{1-y}Ge_y$ layers have in both cases the same nominal Ge concentration of 38%. The stack with the lower Ge concentration is fully strained and the XRD spectrum is well defined with well resolved peaks and a low background signal. The PV-SEM images show a smooth surface without suggesting the presence of misfit dislocations at the underlying $Si/Si_{1-x}Ge_x$ and/or $Si/Si_{1-y}Ge_y$ interfaces. For the stack with the higher Ge concentration, misfit dislocations are detected at different positions of the wafer surface. In Fig. 5 these misfits are marked by arrows. The corresponding XRD spectrum is less well defined with a higher background and less well resolved peaks.

The presence of a Si:P ground plane doped layer, eventually considered for bottom isolation, increases the risk for a degraded material quality, especially when the Si:P ground plane doped layer is formed by ion implantation. In addition, there is a risk for P segregation into the Si/SiGe multi-stack, which also affects final device properties. Both issues can be avoided by using an optimized combination of *ex situ* wet-chemical and *in situ* thermal pre-epi cleaning routines, as confirmed by Extremely Low Impact Energy Secondary Ion Mass Spectrometry (EXLIE-SIMS)[50] shown in Fig. 6. In the given examples, the epitaxial Si:P layers and the Si/SiGe multi-stacks were grown in two separate steps. A wet-chemical

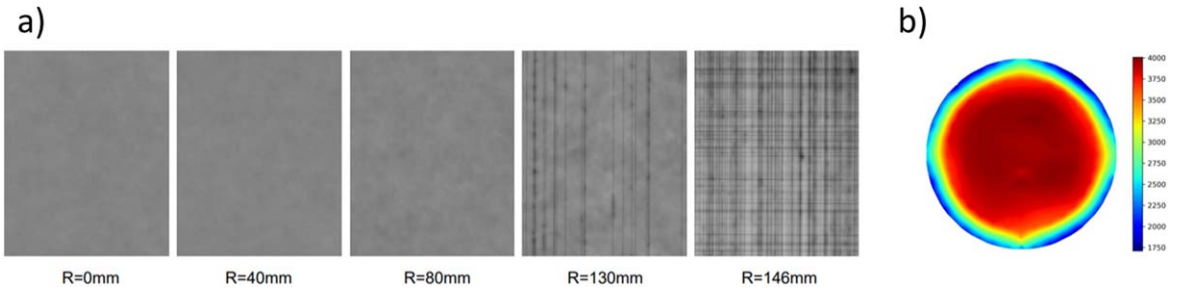

Figure 3. (a) 1400 nm long pass filter PL measured on an epitaxial CFET stack from center to edge over the wafer. The field of view is 140 × 175 μm^2 and R is the radial distance from the wafer center. (b) PL intensity map.

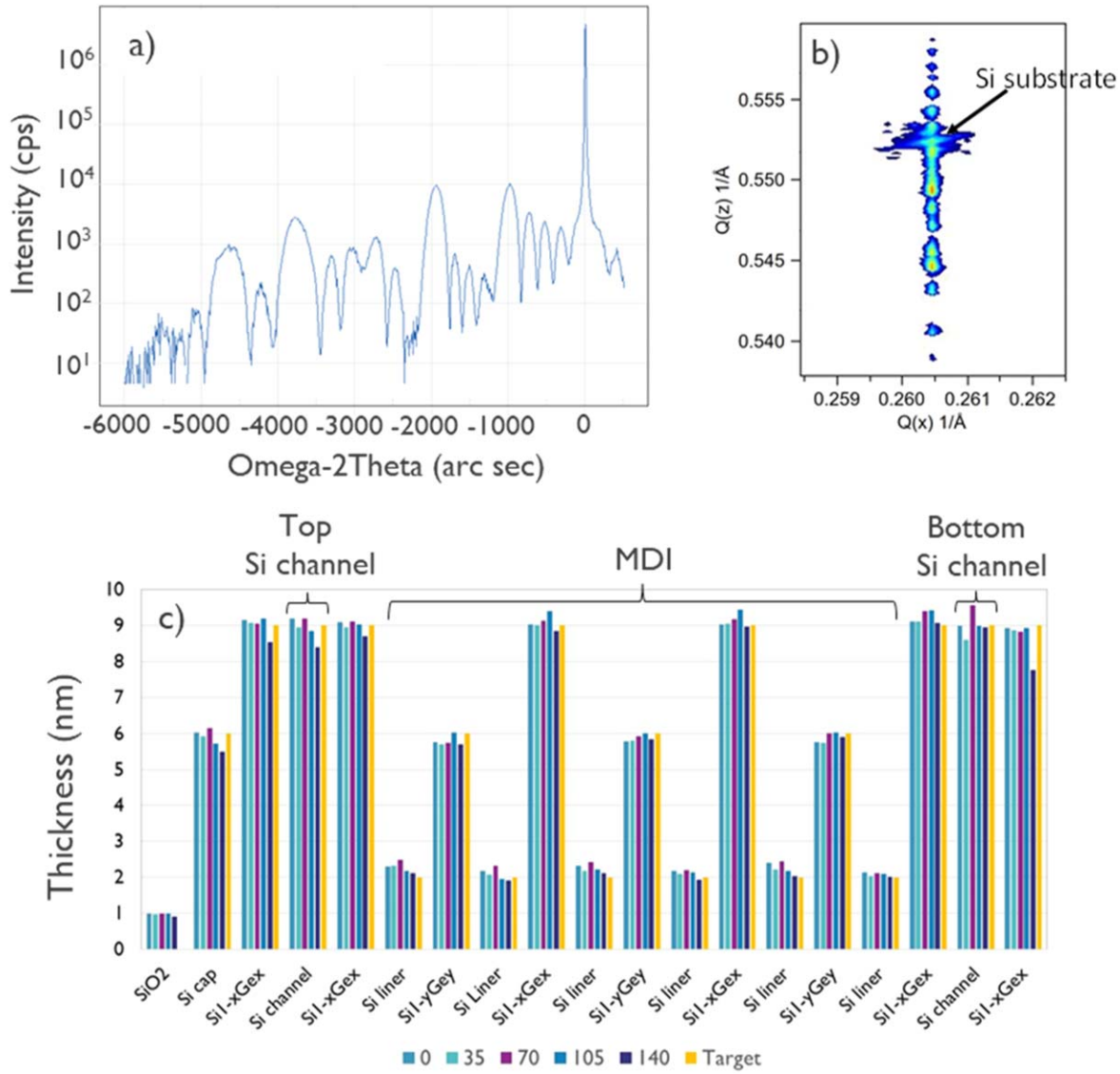

Figure 4. (a) XRD ω-2θ scan acquired around the Si 004 Bragg reflection for the CFET stack shown in Fig. 2b, grown on top of a Si:P ground plane doped layer, (b) XRD RSM acquired for the same stack around the Si 113 Bragg reflection, and (c) thicknesses of the individual layers as extracted from XRR and for different positions over the wafer, where the distance from the wafer center is given in mm.

clean after the Si:P growth, removes the segregated P from the top surface. Before the second epi step, the native oxide is removed in a diluted HF mixture. Using an optimized *in situ* thermal pre-epi treatment minimizes P segregation from the underlying Si:P into the Si/SiGe multi-stack as seen in Fig. 6b, although the phosphorus concentrations in the underlying epitaxial Si:P layers were slightly different for the reported samples (the nominal P concentrations are [P] = 1.3×10^{19} cm^{-3} and 6×10^{18} cm^{-3} for the samples shown in Figs. 6a and 6b, respectively). Both CFET layers have been grown with the same process conditions, except for applied thermal budget during the pre-epi treatment.

The epitaxial growth of the Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ multi-stack can be extended to multiple channels. Figure 7 shows a cross-sectional HAADF STEM of a Si/SiGe multi-stack for CFET devices containing 3 + 3 channels in both the top and the bottom part of the layer-stack. Again, no larger defects are observed across the wafer surface and the epitaxial layer remains free of misfit dislocations, except for the area near the wafer edge, as confirmed by surface haze measurements. The XRD signature, shown in Fig. 7b, is close to the spectrum as predicted by the simulation software. The different peaks are well resolved, and the low background illustrates the high material quality. The differences between the spectrum shown in Fig. 7b with respect to the one shown in Fig. 4a, are the result of the additional layers in the stack. The smooth surface is confirmed by plan view SEM inspections taken at the center and edge of the wafer (Fig. 7c).

The reproducibility of the deposition process has been monitored for 1+1 stacks by measuring the total difference in mass, before and after the epitaxial growth of the CFET stack. The wafer-to-wafer non-reproducibility in total thickness is defined by:

$$non - rep = \frac{\max(mass - increase) - \min(mass\ increase)}{\text{average(mass increase)}} * 100\%$$

For individual batches of 24 wafers, wafer-to-wafer non-reproducibility's in total thickness in the range of 0.9%–1.3% has been measured. A weekly monitoring of the epi process over a period of 4 months gave a process non-reproducibility of 1.7%. Here, it needs to be noted that the epi-system used in this work, was not solely used for the epitaxial growth of CFET stacks which might have a small effect on process reproducibility.

Interface sharpness.—The presence of thin Si liners in between the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers aims to prevent vertical etching of

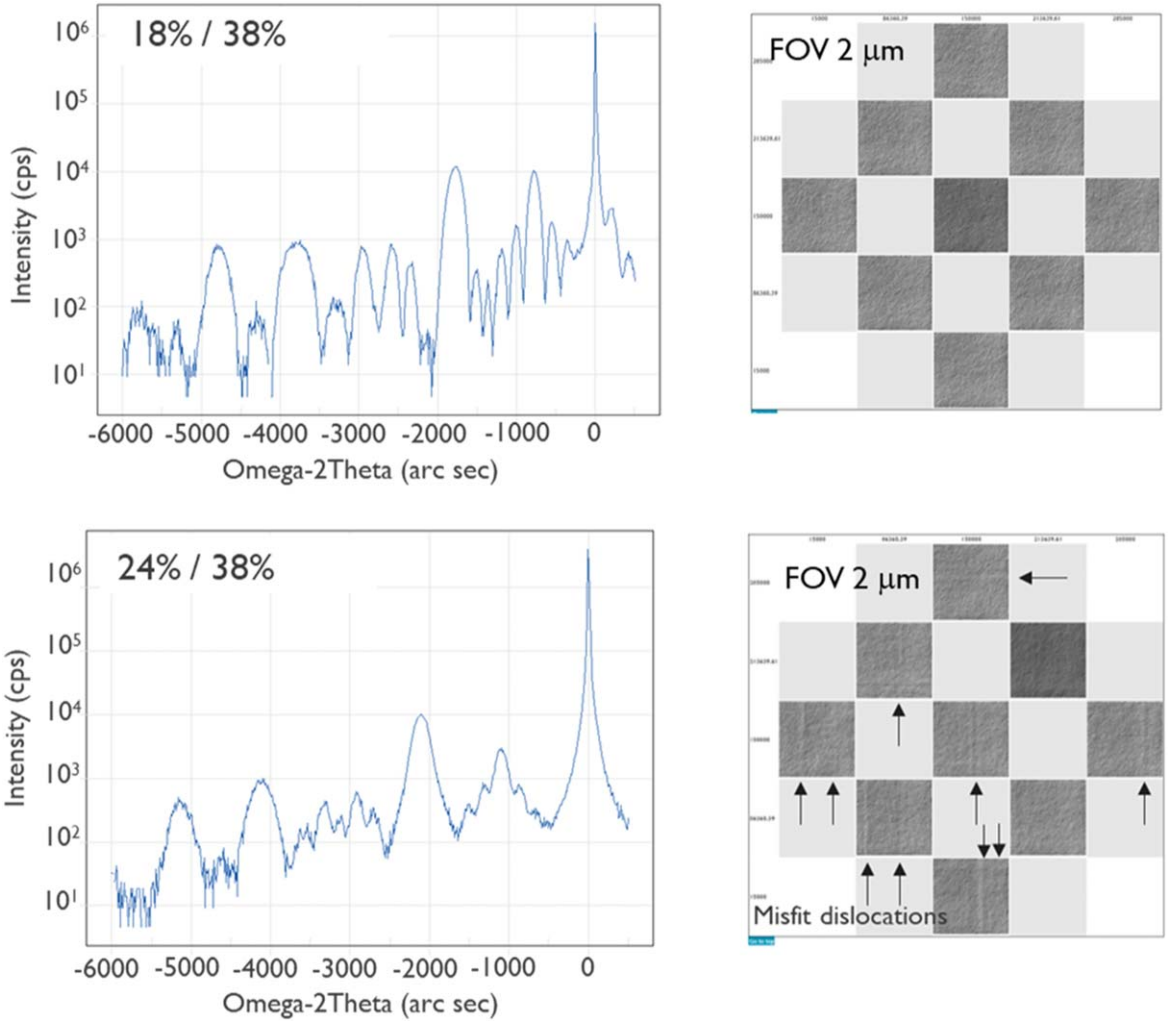

Figure 5. Left: XRD ω-2θ scans acquired around the Si 004 Bragg reflection for CFET stacks with different Ge concentrations in the $Si_{1-x}Ge_x$ layers and grown on top of Si:P ground plane doped layers. Right: plan view SEM inspections taken on multiple locations of the wafer surface. $Si_{1-x}Ge_x$ layers contain 18% Ge (top) and 24% Ge (bottom). In both cases the $Si_{1-y}Ge_y$ layers contain 38% Ge.

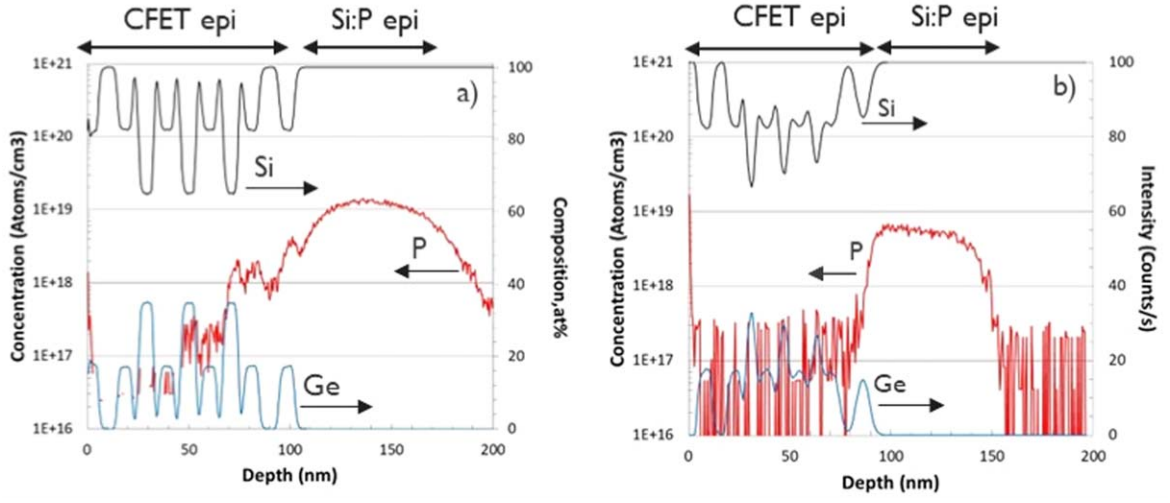

Figure 6. P, Si, and Ge profiles as measured by EXLIE-SIMS for epitaxial CFET stacks grown on top of pre-existing Si:P epi-layers. (a) Non-optimized pre-epi treatment before growing the CFET stack and (b) optimized pre-epi treatment for which the P segregation from the bottom Si:P layer into the CFET multi-stack is clearly suppressed. In (b), the measurement conditions were optimal for P, but not for Si and Ge.

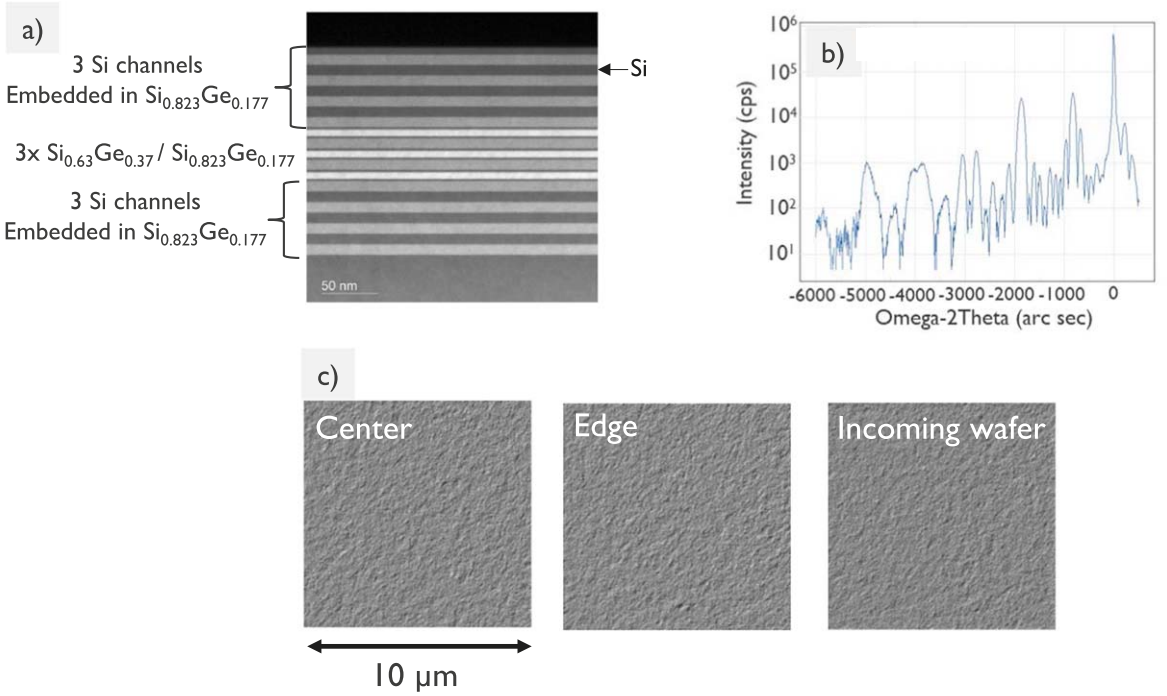

Figure 7. Si/SiGe multi-stack for CFET devices containing 3 + 3 channels in both the top and the bottom part. (a) Cross-sectional HAADF STEM, (b) XRD ω-2θ scans acquired around the Si 004 Bragg reflection, and (c) plan view SEM inspections taken at the center and edge of the wafer and compared with a picture taken on an unprocessed Si wafer.

$Si_{1-x}Ge_x$ during the lateral $Si_{1-y}Ge_y$ removal.[14] Still, the required high etching selectivity of the $Si_{1-y}Ge_y$ layers towards both $Si_{1-x}Ge_x$ and Si, and also of $Si_{1-x}Ge_x$ towards Si later in the processing flow, sets requirements on the sharpness of the interfaces between different layers. EXLIE-SIMS,[50] Energy-Dispersive X-ray spectroscopy (EDX), integrated STEM contrast analysis,[41] and soft X-ray reflectometry[42,43] confirm the sharp gradients in Ge concentration at the different interfaces. A typical example of Ge and Si profiles as measured by EXLIE-SIMS is shown in Fig. 8a, which also confirms the layer-to-layer reproducibility in composition. All interfaces are extremely sharp. The depth resolution of the EXLIE-SIMS is therefore not sufficient to extract interface steepness.

The interface abruptness has nevertheless been extracted from horizontally integrated HAADF-STEM contrast images (Fig. 8b). The HAADF-STEM contrast is approximately proportional to the square of the atomic number, which allows to extract the Ge depth profiles (Fig. 8c). integrated contrast has been fitted with the Sigmoid function which is expressed as:

$$f(x) = \frac{C}{1 + e^{\frac{\pm(z_0 - x)}{\tau}}} + b \qquad [2]$$

where C and b are constants and z_o denotes the position of the interface. The value of 4τ is used as the interface thickness.[51] Note that the integrated contrast profiles shown in Fig. 8c have been obtained by integrating over an area of the TEM specimen. The extracted 4τ values include contributions from interfacial roughness and are therefore larger than the values obtained when extracting the contrast profile from a vertical line scan. The TEM specimens were prepared by focused ion beam (FIB), with a target lamella thickness of ~80 nm. The effect of the lamella thickness on the extracted interface thickness is supposed to be negligible.

The interfaces from the Si-channel (bottom side) towards $Si_{1-x}Ge_x$ (top side) are, as expected, slightly sharper than the interfaces from $Si_{1-x}Ge_x$ (bottom side) towards the Si-channel (top side) (Fig. 8c, top and bottom figures). For the latter one, the abruptness of the compositional change is limited by Ge segregation, occurring during Si layer growth on the $Si_{1-x}Ge_x$ surface. The Si-liners placed in-between $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers, are too thin to enable extraction of interfacial thicknesses between the $Si_{1-y}Ge_y$ and Si layers, as Si-top and bottom interfaces are overlapping (Fig. 8c, middle part). The presence of the Si-liners does allow a successful selective $Si_{1-y}Ge_y$ removal without damaging $Si_{1-x}Ge_x$ as reported in[9] and,[12] which illustrates the interfacial sharpness in a different way.

Low temperature photoluminescence.—The low temperature PL spectra contain four well defined luminescence peaks (Fig. 9a). By temperature- and excitation-power-dependent measurements, combined with a comparison with the PL spectra obtained on reference samples which contain only one group of SiGe layers (either the low-Ge $Si_{1-x}Ge_x$ or the Ge-rich $Si_{1-y}Ge_y$), the peaks could be assigned to the no-phonon (NP) transitions and their transverse optical (TO) phonon replicas arising from the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers with the two different Ge concentrations.[52,53] The largest fraction of the laser light is absorbed in the Si substrate where consequently the majority of the excitons are created. At the lowest measurement temperature, these excitons are trapped by the SiGe layer which is next to the substrate. This explains the higher intensity of the low-Ge $Si_{1-x}Ge_x$ luminescence. With increasing laser intensity, the NP peaks shift to a higher energy as the luminescence changes from localized excitons (LE's) to bound excitons (BE's), and free excitons (FE's) (not shown). Increasing the measurement temperature results in a thermal quenching of the low-Ge $Si_{1-x}Ge_x$ luminescence and a negative thermal quenching of the Ge-rich $Si_{1-y}Ge_y$ luminescence (Fig. 9b). Excitons can escape from the low-Ge $Si_{1-x}Ge_x$ layer(s) and are trapped by the Ge-rich $Si_{1-y}Ge_y$ layers which have a larger valence band offset, with respect to Si. The fact that excitons can escape from low-Ge $Si_{1-x}Ge_x$ layer(s) and move to Ge-rich $Si_{1-y}Ge_y$ layers without being trapped by non-radiation recombination centers illustrates the high material quality of the epitaxial stack and the absence of defects. Above ~120 K, there is no luminescence signal at energies above 0.9 eV (no luminescence arising from the low-Ge $Si_{1-x}Ge_x$ layers) and the PL intensity at 0.8–0.9 eV shows normal thermal quenching.

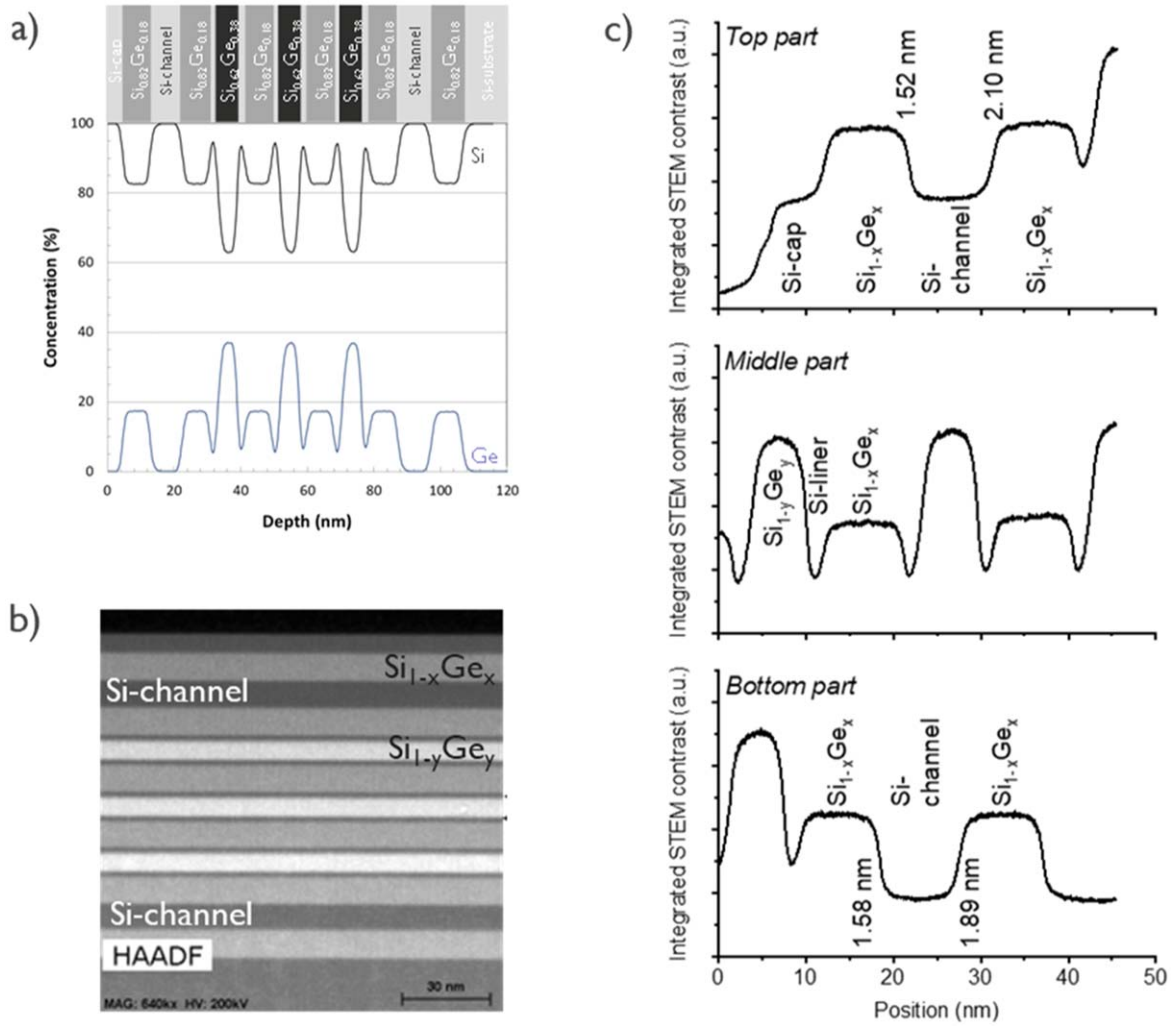

Figure 8. Si/SiGe multi-stack as used for CFET devices with one channel for both the p-type and the n-type devices. (a) Ge and Si EXLIE-SIMS profiles, (b) cross-sectional HAADF STEM, and c) horizontally integrated contrast profiles extracted from high resolution HAADF STEM images. The numbers mentioned at the $Si_{1-x}Ge_x$/Si and Si/ $Si_{1-x}Ge_x$ interfaces are the interface thicknesses obtained after fitting the contrast profiles with the Sigmoid function.

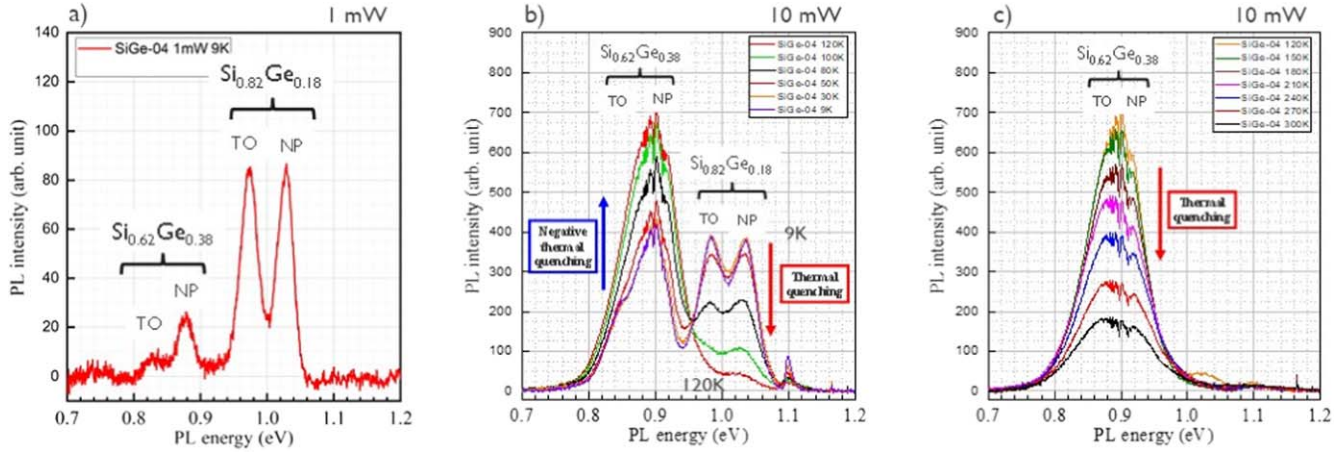

Figure 9. PL intensity as function of PL energy as measured on a complete CFET stack. (a) Spectrum measured at 9 K and an excitation power intensity of 1 mW. (b) and (c) Temperature dependent PL spectra measured at an excitation power intensity of 10 mW and in temperature regimes of 9–120 K and 120–300 K, respectively.

Conclusions

The material properties of Si/SiGe multi-layer stacks used for CFET devices have been presented. The epitaxial layers contain two different Ge concentrations and have been grown using conventional process gases. Despite the relative high growth temperature, island growth can be suppressed for Ge concentrations up to ∼40%.

Excellent material properties have been reported. A carefully optimized pre-epi surface preparation routine prevents both degradation of the material quality as well as phosphorus segregation when depositing the CFET stack on top of a Si:P ground plane doped layer. The optimized epitaxial growth process allows the deposition of the Si/SiGe CFET stack with multiple channels as demonstrated for 3 + 3 channels at the top and bottom part of the layer stack. Room temperature PL measurements allow for a fast and reliable verification of the absence/presence of lattice defects including full wafer mapping. Complementary low temperature PL measurements have been used to study the optical material properties of individual sublayers and to further demonstrate the material quality of the CFET stack.

Acknowledgments

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007254. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Germany, France, Czech Republic, Austria, Spain, Belgium, Israel. The project is also supported by the Chips Joint Undertaking and its members, including the top-up funding by VLAIO. Parts of the results were achieved using the NanoIC pilot line, which is supported by the Flemish government (Belgium) and received funding from the Chips Joint Undertaking through *the Horizon Europe program under grant agreement No 101183277."* As set out in the Grant Agreement, beneficiaries must ensure that at the latest at the time of publication, open access is provided via a trusted repository to the published version or the final peer-reviewed manuscript accepted for publication under the latest available version of the Creative Commons Attribution International Public Licence (CC BY). For the purpose of open access the author has applied a CC BY public copyright licence to any Author Accepted Manuscript version arising from this submission.

Parts of this work were supported by a JSPS-FWO Bilateral Joint Research Project (file number: VS01522N). The imec core CMOS program members, local authorities and the imec pilot line are acknowledged for their support.

ORCID

R. Loo https://orcid.org/0000-0003-3513-6058
A. Akula https://orcid.org/0009-0002-8111-1513
Y. Shimura https://orcid.org/0000-0002-1944-9970
C. Porret https://orcid.org/0000-0002-4561-348X
E. Rosseel https://orcid.org/0000-0002-2737-8391
T. Dursap https://orcid.org/0009-0004-8907-4969
A. Y. Hikavyy https://orcid.org/0000-0002-8201-075X
M. Beggiato https://orcid.org/0000-0003-0873-9021
J. Bogdanowicz https://orcid.org/0000-0002-7503-8922
A. Merkulov https://orcid.org/0000-0003-4101-0873
M. Ayyad https://orcid.org/0000-0003-2222-8295
H. Han https://orcid.org/0000-0003-2169-8332
O. Richard https://orcid.org/0000-0002-3994-8021
A. Impagnatiello https://orcid.org/0000-0002-0923-4642
D. Wang https://orcid.org/0000-0003-0634-953X
K. Yamamoto https://orcid.org/0000-0001-8730-598X
H. Mertens https://orcid.org/0000-0002-3392-6892
N. Horiguchi https://orcid.org/0000-0001-5490-0416
R. Langer https://orcid.org/0000-0002-1132-3468

References

1. P. Weckx et al., *2017 IEEE International Electron Device Meeting (IEDM)* (2017), 20.5.1.
2. H. Mertens et al., *2021 IEEE Symposium on VLSI Technology* (2021), T 2.1978-1-6654-1945-1.
3. J. Zhang et al., *2019 IEEE International Electron Device Meeting (IEDM)* (2019), 11.6.1.
4. A. Hikavyy, C. Porret, R. Loo, M. Mencarelli, P. Favia, M. Ayyad, B. Briggs, R. Langer, and N. Horiguchi, *ECS Trans.*, **104**, 139 (2021).
5. H. Mertens et al., *2022 IEEE International Electron Device Meeting (IEDM)* (2022), 23.1.1.
6. P. Schuddinck et al., *2022 IEEE Symposium on VLSI Technology*365 (2022).
7. S. Subramanian et al., *2020 IEEE Symposium on VLSI Technology* (2020), TH3.1.
8. A. Vandooren et al., *2022 IEEE Symposium on VLSI Technology*330 (2022).
9. N. Horiguchi et al., *2023 IEEE International Electron Device Meeting (IEDM)* (2023), 29.1.1.
10. M. Radosavljević et al., *2023 IEEE International Electron Device Meeting (IEDM)* (2023), 29.2.1.
11. S. Liao et al., *2023 IEEE International Electron Device Meeting (IEDM)* (2023), 29.6.1.
12. S. Demuynck et al., *2024 IEEE Symposium on VLSI Technology* (2024), T5.2.
13. R. Loo, Y. Shimura, A. Akula, C. Porret, A. Merkulov, M. Ayyad, H. Han, O. Richard, A. Impagnatiello, and A. Hikavyy, *2023 International Conference on Solid State Devices and Materials (SSDM)*291 (2023), (paper F-5-03).
14. R. Loo, N. Gosset, M. Isaji, Y. I. Kawamura, A. Y. Hikavyy, E. Rosseel, C. Porret, A. Nalin Mehta, and J-M. Girard, *ECS Trans.*, **109**, 135 (2022).
15. Y. Muraki et al., *Proc. SPIE 12056, Advanced Etch Technology and Process Integration for Nanopatterning XI* (2022) PC1205604.
16. Y. Oniki, K. Kenis, K. Wostyn, E. Altamirano-Sánchez, and F. Holsteyn, *Surface Preparation and Cleaning Conference (SPCC)* (2020).
17. J. M. Hartmann, V. Destefanis, G. Rabillé, and S. Monfray, *Semicond. Sci. and Technol.*, **25**, 105009 (2010).
18. P. Raghavan et al., *2015 Custom Integrated Circuits Conference (CICC)*1 (2015).
19. C. Porret et al., *2022 IEEE International Electron Device Meeting (IEDM)* (2022), 34.1.1.
20. C. Porret et al., *2023 International Conference on Solid State Devices and Materials (SSDM)*287 (2023), (paper F-5-01).
21. F. Panciera, K. Hoummada, C. Perrin, M. E. Kousseifi, R. Pantel, M. Descoins, M. Gregoire, M. Juhel, and D. Mangelinck, *Microelectron. Eng.*, **120**, 34 (2014).
22. A. Veloso et al., *IEEE Trans. Elec. Dev.*, **69**, 7173 (2022).
23. A. Jourdain et al., *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*42 (2020).
24. R. Loo, A. Jourdain, G. Rengo, C. Porret, A. Hikavyy, M. Liebens, L. Becker, P. Storck, G. Beyer, and E. Beyne, *ECS J. Solid State Sci. Techn.*, **10**, 014001 (2021).
25. A. Hikavyy, I. Zyulkov, H. Mertens, L. Witters, R. Loo, and N. Horiguchi, *Mater. Sci. Semicond. Process.*, **70**, 24 (2017).
26. C. Porret et al., *ECS J. Solid State Sci. Technol.*, **8**, P392 (2019).
27. E. Rosseel, C. Porret, A. Hikavyy, R. Loo, M. Tirrito, B. Douhard, O. Richard, N. Horiguchi, and R. Khazaka, *ECS Trans.*, **98**, 37 (2020).
28. E. Rosseel, C. Porret, A. Hikavyy, R. Loo, O. Richard, G. T. Martinez, D. Batuk, H. Mertens, E. Dentoni Litta, and N. Horiguchi, *ECS Trans.*, **109**, 93 (2022).
29. E. Rosseel et al., *ECS Meet. Abstr.*, **MA2024-02**, 2298 (2024).
30. E. Rosseel et al., *ECS Trans.*, **114**, 29 (2024).
31. L. Vescan, W. Jäger, C. Dieker, K. Schmidt, A. Hartmann, and H. Lüth, *MRS Online Proceedings Library*, **263**, 23 (1992).
32. D. J. Paul, *Semicond. Sci. Technol.*, **19**, R75 (2004).
33. J. M. Hartmann, A. Abbadie, and S. Favier, *J. Appl. Phys.*, **110**, 083529 (2011).
34. D. Kohen, V. D'Costa, N. Bhargava, and J. Tolle, *Semicond. Sci. Technol.*, **33**, 104003 (2018).
35. Z. Kong et al., *ACS Appl. Mater. Interfaces*, **15**, 56567 (2023).
36. J. M. Hartmann, V. Loup, G. Rolland, P. Holliger, F. Laugier, C. Vannuffel, and M. N. Séméria, *J. Cryst. Growth*, **236**, 10 (2002).
37. B. Vincent, R. Loo, W. Vandervorst, G. Brammertz, and M. Caymax, *J. Cryst. Growth*, **312**, 2671 (2010).
38. P. Meunier-Beillard, M. Caymax, K. Van Nieuwenhuysen, G. Doumen, B. Brijs, M. Hopstaken, L. Geenen, and W. Vandervorst, *Appl. Surf. Sci.*, **224**, 31 (2004).
39. J. Bogdanowicz et al., *ECS Meet. Abstr.*, **MA2024-02**, 2302 (2024).
40. J. Bogdanowicz, A-L. Charley, and P. Leray, *Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII* (2023) 1249617.
41. P. Favia et al., *Semicond. Sci. Technol.*, **34**, 124003 (2019).
42. R. Ciesielski, J. Bogdanowicz, R. Loo, Y. Shimura, A. Mani, C. Mitterbauer, M. Kolbe, and V. Soltwisch, *Proc. SPIE 12955, Metrology, Inspection, and Process Control XXXVIII* (2024) 1295507.
43. R. Ciesielski, J. Bogdanowicz, R. Loo, Y. Shimura, A. Mani, C. Mitterbauer, M. Kolbe, and V. Soltwisch, *J. Micro/Nanopattern. Mater. Metrol.*, **23**, 041405 (2024).
44. J. Frascaroli et al., *IEEE Trans. Semicon. Manuf.*, **35**, 540 (2022).
45. J. Frascaroli, S. Colombo, R. Fumagalli, I. Mica, L. Livellara, V. Samu, and G. Molnár, *Phys. Status Solidi a*, **219**, 2200150 (2022).
46. R. Loo, A. Hikavyy, D. Wang, K. Yamamoto, T. Sipőcz, Á. Kerekes, A. Akula, and Y. Shimura, *2023 International Conference on Solid State Devices and Materials (SSDM)*525 (2023), (paper M-3-05).
47. G. Rengo, D. Casey, B. Marozas, N. Claessens, and R. Khazaka, *ECS Meet. Abstr.*, **MA2024-02**, 2300 (2024).
48. G. Rengo, D. Casey, B. Marozas, N. Claessens, and R. Khazaka, *ECS Trans.*, **114**, 47 (2024).
49. H. Arora and J. Tolle, *ECS Meet. Abstr.*, **MA2024-02**, 2297 (2024).
50. W. Vandervorst, *Appl. Surf. Sci.*, **255**, 805 (2008).
51. O. Dyck, D. N. Leonard, L. F. Edge, C. A. Jackson, E. J. Pritchett, P. W. Deelman, and J. D. Poplawsky, *Adv. Mater. Interfac.*, **4**, 1700622 (2017).
52. G. Brémond, A. Souifi, T. Benyattou, and D. Dutartre, *Thin Solid Films*, **222**, 60 (1992).
53. J. C. Sturm, H. Manoharan, L. C. Lenchyshyn, M. L. W. Thewalt, N. L. Rowell, J. P. Noel, and D. C. Houghton, *Phys. Rev. Lett.*, **66**, 1362 (1991).