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Comparative Analysis of Space Vector Pulse-Width Modulation Techniques of Three-Phase Inverter to Minimize Common Mode Voltage and/or Switching Losses

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Abstract: Inverter-based systems encounter significant challenges in mitigating common-mode voltage (CMV) and minimizing inverter losses. Despite various space vector pulse-width modulation (SVPWM) techniques proposed to address these issues, a comprehensive comparative analysis has been lacking. This paper addresses this gap through an experimental and simulation-based evaluation of nine SVPWM techniques. A new discontinuous SVPWM technique, DSVPWM-K4, is introduced, which involves reversing the use of the two zero vectors in DSVPWM-K3. DSVPWM-K3 delivers superior performance in terms of CMV reduction, total harmonic distortion (THD), and inverter losses across all modulation indices (MI = 1, 0.75, 0.5, and 0.25), making it the most effective overall. Although DSVPWM-K4 is a novel approach, it ranks second in effectiveness. The RSPWM technique achieves the lowest CMV with a zero peak-to-peak value but is most effective at lower modulation indices (0.25 and 0.5) due to higher harmonic distortion at higher modulation indices. AZSPWM performs optimally at higher modulation indices, providing a 66.66% reduction in CMV compared to continuous SVPWM and significantly lower THD compared to RSPWM. In contrast, NSPWM exhibits nearly double the THD compared to continuous SVPWM.

Keywords: three-phase inverter; SPWM; SVPWM; DSVPWM; inverter losses; CMV; THD; AZSPWM; RSPWM; RSPWM

MSC: 65K10



Citation: Tawfiq, K.B.; Sergeant, P.; Mansour, A.S. Comparative Analysis of Space Vector Pulse-Width Modulation Techniques of Three-Phase Inverter to Minimize Common Mode Voltage and/or Switching Losses. *Mathematics* **2024**, *12*, 2832. <https://doi.org/10.3390/math12182832>

Academic Editor: Senthil Krishnamurthy

Received: 15 August 2024

Revised: 9 September 2024

Accepted: 11 September 2024

Published: 12 September 2024



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1. Introduction

The two-level voltage source inverter (VSI) is at the core of numerous applications, including motor drive systems, wind energy generating systems, and renewable energy grid integration. Most prior and ongoing research has focused on improving the performance of the VSI. These improvements are reducing both inverter losses and common mode voltage (CMV). The control technique is the fundamental basis for realizing these improvements [1,2].

Several pulse-width modulation (PWM) strategies for controlling the VSI have been developed in the literature [3–7]. These PWM techniques are categorized into two types: sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM). In SPWM, a sine wave is compared to a triangle wave. The switching points are generated by intersecting the triangular carrier wave of frequency f_c with the reference modulating sine wave of frequency f_m . The output voltage is proportional to the size of the

sine wave, and the output frequency is equal to the sine wave frequency f_m [4]. SVPWM differs from and outperforms SPWM. SVPWM provides PWM load line voltages that are, on average, equal to the reference load line voltage. The implementation of SVPWM is based on the suitable selection of inverter switching states, the computation of appropriate switching time periods, and space vector transformation. SVPWM offers several advantages, including lowering switching losses by minimizing superfluous switching. As a result, the inverter's output capability improves. SVPWM makes more efficient use of the supply voltage compared to SPWM and also reduces the harmonic content in the output voltage waveforms. Since the copper losses of the machine are influenced by the harmonic content of the inverter output, and these losses constitute a significant portion of the machine's total losses, a lower total harmonic distortion (THD) means the voltage waveform is closer to a pure sine wave [5,6]. Figure 1a plots the percentage of total harmonic distortion (%THD) for both SPWM and SVPWM output voltages versus the modulation index. The output line-to-line voltage of both SPWM and SVPWM is shown against the modulation index in Figure 1b. The data in Figure 1 demonstrate that SVPWM outperforms SPWM, making SVPWM the preferred control mechanism [7].

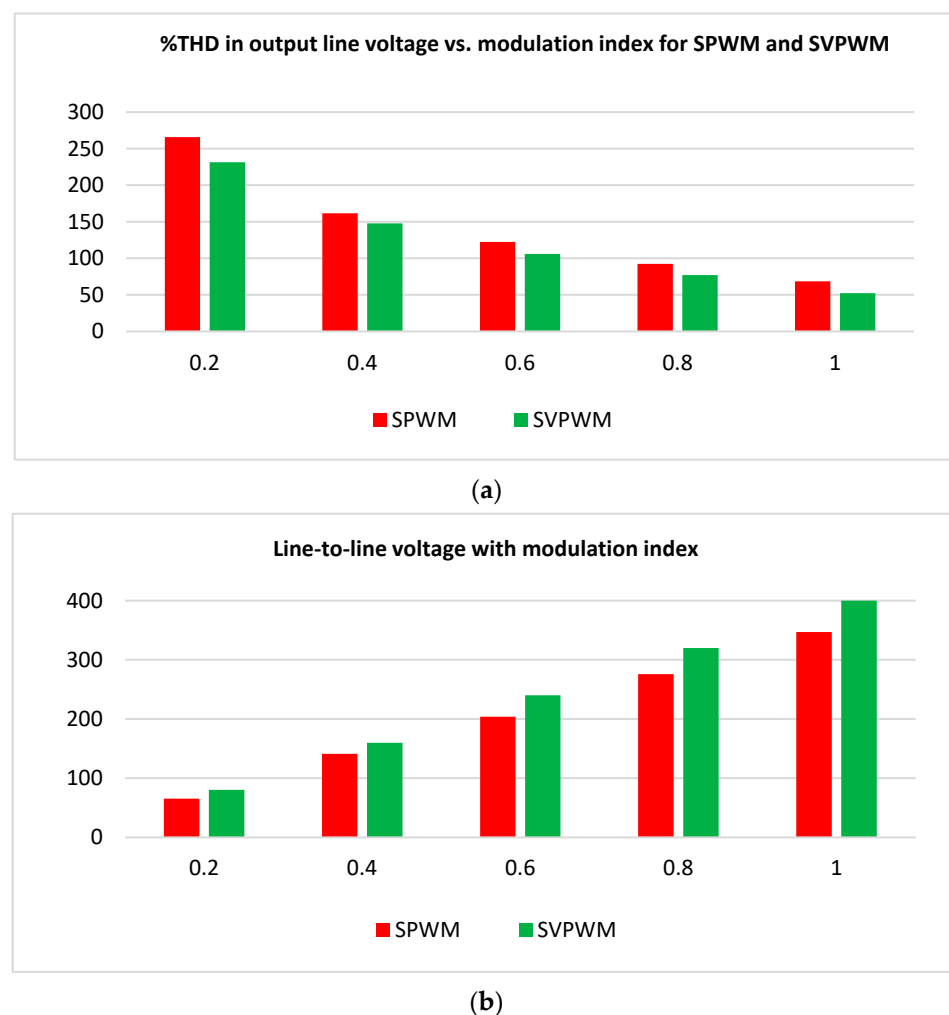


Figure 1. (a) %THD in output line voltage versus modulation index for SPWM and SVPWM, and (b) line-to-line voltage with modulation index.

In continuous SVPWM, each leg achieves a single commutation every switching cycle. To minimize switching losses, the zero vectors can be adjusted so that one of the three legs remains either always ON or always OFF throughout the switching cycle. This approach is referred to as discontinuous SVPWM (DSVPWM) [8–10]. Several DSVPWM techniques aimed

at reducing switching losses have been documented in the literature [11–28]. In [11–13], DSVPWM techniques were explored to decrease both switching losses and common mode voltage. In [14,15], these techniques were applied to three-phase four-leg VSIs. Reference [16] developed a generalized discontinuous PWM (GDPWM) approach, which offers improved performance across high modulation ranges and achieves the lowest switching losses across all modulation ranges. Reference [17] proposed an alternative GDPWM approach based on two-phase rotating dq coordinates, along with various discontinuous PWM (DPWM) strategies. In [18,19], the DPWM approach was applied to multilayer inverters.

While SVPWM has gained favor in industrial applications for its higher harmonic performance and ease of installation, it creates significant CMV in both amplitude and frequency. To offset the negative CMV effects caused by SVPWM, researchers have developed various space vector-based reduced-CMV PWM approaches. The most common of these include active zero-state pulse-width modulation (AZSPWM) [20], remote-state pulse-width modulation (RSPWM) [21,22], and near-state pulse-width modulation (NSPWM) [23]. Each reduced-CMV PWM approach has distinct properties, and no existing research study has conducted a comparison evaluation of these three PWM methods in terms of CMV patterns, switching losses, and THD.

The literature lacks a comprehensive comparison of earlier PWM types focused on reducing inverter losses, CMV, and harmonic currents. A new discontinuous SVPWM technique, DSVPWM-K4, is introduced, which involves reversing the use of the two zero vectors in DSVPWM-K3. Therefore, this paper investigates and compares nine SVPWMs with the goal of minimizing CMV, inverter losses, and harmonic currents. The experimental validation of the nine SVPWMs was compared to the results of the MATLAB R2023a simulation under the same conditions and across different modulation indices.

2. Description of the Different SVPWMs

This section describes and discusses the considered nine SVPWM techniques. According to Figure 2a, the three-phase inverter has six switches. The inverter's switches can be configured in only eight distinct ways, as the output cannot be short-circuited through any of the three half-bridge terminals, and the load cannot be disconnected at any time. Among the eight allowed combinations, there are six active voltage vectors (V_1 – V_6) and two zero-output voltage vectors (V_0 [000], V_7 [111]), as shown in Figure 2b. According to voltage vector V_7 (111), the top switches in the inverter are on and the bottom switches are off. The reference output voltage of the inverter is computed utilizing the neighboring active vectors and zero vector in each sector. The duty cycles of these vectors are computed as in (1). In (1), the entire duration periods of the vectors V_α , V_β and zero vector are T_α , T_β and T_z , respectively. The variables θ_v and m_v denote the angle of the reference output vector within the hexagonal sector and the modulation index, respectively [24,25].

$$\begin{cases} V_o^* = d_\alpha V_\alpha + d_\beta V_\beta + d_z V_z, \\ d_\alpha = \frac{T_\alpha}{T_s} = m_v \cdot \sin\left(\frac{\pi}{3} - \theta_v\right) \\ d_\beta = \frac{T_\beta}{T_s} = m_v \cdot \sin(\theta_v) \\ d_7 = d_0 = \frac{T_z}{T_s} = 1 - (d_\alpha + d_\beta) \end{cases} \quad (1)$$

The different pulse-width modulation algorithms differ in their approach to zero vector selection, the sequence of consecutive vectors, and duty cycle splitting. These modulation algorithms can be classified into continuous SVPWM and discontinuous SPVWM.

2.1. Continuous SVPWM

SVPWM is a commonly used algorithm for controlling the three-phase drive systems. The switching sequence of the SVPWM is shown in Figure 2c. In this algorithm, the two zero vectors are employed during each switching cycle, as shown in Figure 2c. The switching cycle begins and ends with zero vector V_0 , while zero vector V_7 is used in the

middle of the cycle [25]. This PWM method will be the first considered in this paper and will serve as the reference PWM method.

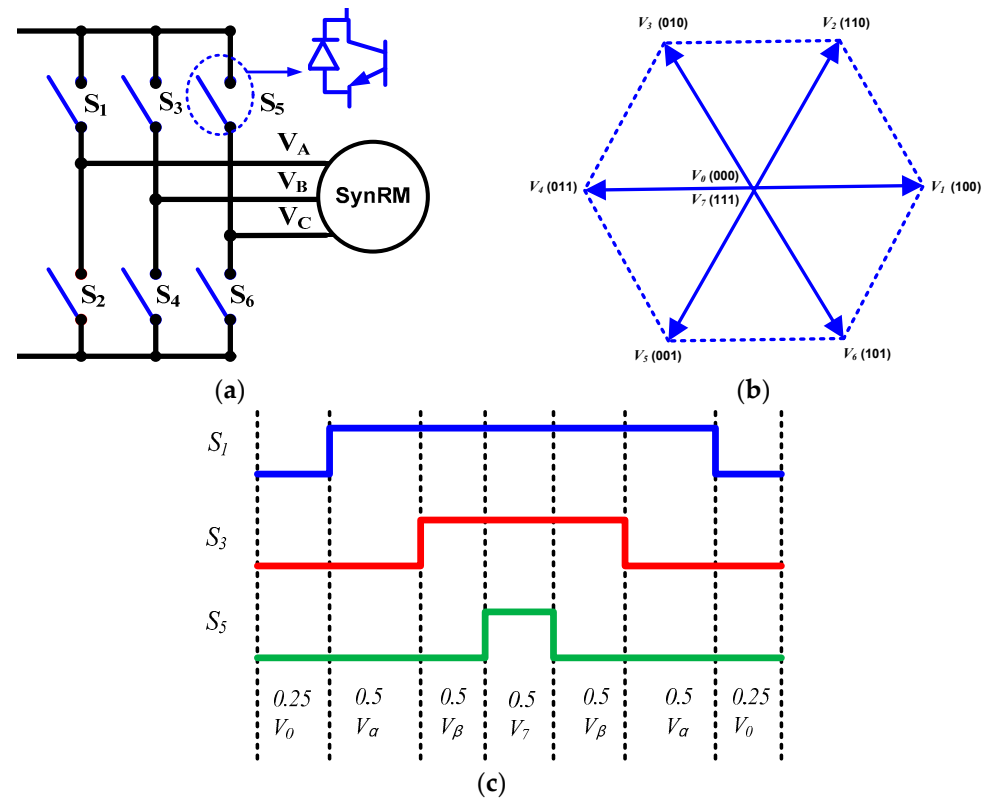


Figure 2. (a) Three-phase inverter, (b) hexagon for three-phase inverter, and (c) switching sequence for continuous SVPWM for one cycle in the first sector.

2.2. Discontinuous SVPWMs

Due to the recent focus on enhancing drive system efficiency, considerable attention has been given to employing the DSVPM approach to minimize switching losses and thereby boost drive system efficiency. Reference [26] introduced a DSVPM technique aimed at reducing the switching losses. In [26], one leg of the inverter was not modulated for one-third of the period of the fundamental frequency, and only one zero vector was used during the switching cycle. However, in [26], the state of two switches sometimes changed between adjacent switching actions to compensate for the reduction in switching losses caused by the non-modulation of one leg of the inverter. As a result, several DSVPM techniques have been proposed in the literature [20–28], which keep only one switch's state changing between the adjacent switching actions and avoid modulating the inverter leg for one-third of the period time. This paper compares the continuous SVPWM with eight DSVPM techniques. The concept of the DSVPM techniques are as follows:

2.2.1. DSVPM-K1

In [27], zero vector $V_7(111)$ is exclusively used as the zero vector, applied only at the beginning and at end of the switching cycle, with no zero-vector applied in the middle of the cycle. Moreover, the sequence of the active vectors is selected to ensure that only one switch's state changes between two adjacent switching actions. For example, and as shown in Figure 3a, the switching sequence in the first sector is $V_7(111)$, followed by $V_\beta(110)$, then $V_\alpha(100)$, then back to $V_\beta(110)$, and finally $V_7(111)$ again. As can be seen from Figure 3a, only one switch commutates between the adjacent switching action, which helps reduce the switching losses of the power converter. This PWM technique will be referred to as DSVPM-K1 in this paper.

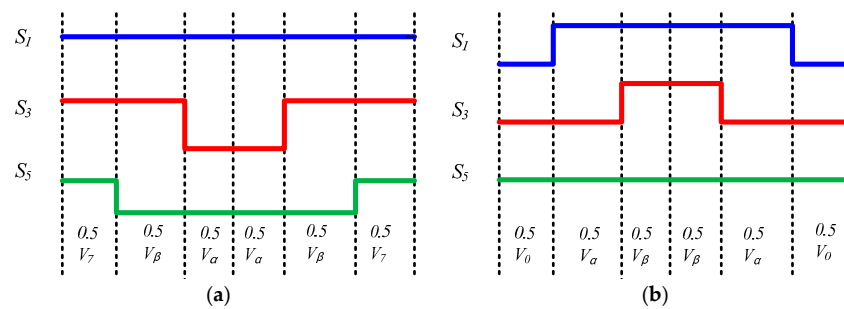


Figure 3. Switching sequence in the first sector of (a) DSVPWM-K1 and (b) DSVPWM-K2.

2.2.2. DSVPWM-K2

In [28], zero vector V_0 (000) is exclusively used as the zero vector, applied only at the beginning and at end of the switching cycle. Additionally, the order of the active vectors is chosen to ensure that only one switch state changes between two adjacent switching actions. As an illustration, in the first sector, the switching order is V_0 (000), followed by V_α (100), then V_β (110), then back to V_α (100), and finally V_0 (000) again, as illustrated in Figure 3b. Only one switch commutates between the neighboring switching action, as can be observed in Figure 3b. This PWM technique will be referred to as DSVPWM-K2 in this paper.

2.2.3. DSVPWM-K3

The third DSVPWM technique, referred to as DSVPWM-K3, combines the previous two methods and was introduced in [27]. It employs DSVPWM-K1 in the odd sectors and DSVPWM-K2 in the even sectors.

2.2.4. DSVPWM-K4

The six sectors of the hexagon are divided into two regions, resulting in a total of six sectors and twelve regions. In odd sectors, the first region utilizes zero vector V_0 (000), while the second region uses zero vector V_7 (111). Conversely, in even sectors, the first region employs zero vector V_7 (111), and the second region uses zero vector V_0 (000). This control method is novel and has not been introduced before; it will be included in the comparison in this paper as DSVPWM-K4.

2.2.5. DSVPWM-K5

The fifth DSVPWM technique (DSVPWM-K5) discussed in this paper uses the same topology as the previous method and was introduced in [27]. The difference with DSVPWM-K5 is that zero vector V_0 (000) is used in the first region of the even sectors and the second region of the odd sectors, while zero vector V_7 (111) is used for the rest of the regions.

2.2.6. AZSPWM

In this method, the two zero vectors are not used to minimize the CMV [20]. The reference output voltage (V_o^*) is synthesized using two neighboring active voltage vectors, while the effective zero voltage vector is generated by two opposing active voltage vectors, as illustrated in Table 1.

Table 1. The active and the effective zero vectors in different sectors for AZSPWM.

Sector	V_α	V_β	Zero Vectors
1	(100)	(110)	(101), (010)
2	(010)	(110)	(011), (100)
3	(010)	(011)	(110), (001)
4	(001)	(011)	(101), (010)
5	(001)	(101)	(011), (100)
6	(100)	(101)	(110), (001)

2.2.7. RSPWM

In this method, vectors with the same common-mode value, such as V_1, V_3, V_5 , or V_2, V_4, V_6 , are used to generate the required output voltage [21,22]. As introduced in [22], this technique alternates between the two vector groups every 60° , as shown in Figure 4 and Table 2. The sequence of vectors in RSPWM is defined in Table 2.

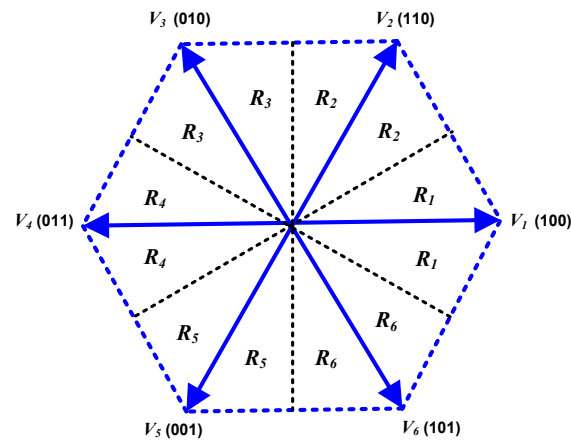


Figure 4. Regions in the hexagon of RSPWM.

Table 2. Vector definition and sequence for RSPWM.

Region	Vectors (V_x, V_y, V_z)	Sequence
R_1	V_1, V_3, V_5	$V_y - V_x - V_z - V_x - V_y$
R_2	V_2, V_4, V_6	$V_y - V_x - V_z - V_x - V_y$
R_3	V_3, V_5, V_1	$V_y - V_x - V_z - V_x - V_y$
R_4	V_4, V_6, V_2	$V_y - V_x - V_z - V_x - V_y$
R_5	V_5, V_1, V_3	$V_y - V_x - V_z - V_x - V_y$
R_6	V_6, V_2, V_4	$V_y - V_x - V_z - V_x - V_y$

2.2.8. NSPWM

The NSPWM technique described in [23] generates the required output voltage by combining three active voltage vectors. It employs the active vectors closest to the reference voltage and selects a near-neighbor voltage vector based on the position of the reference voltage. On the vector plane, the voltage vectors used vary every 60° , while the sequence of these vectors varies every 30° , as illustrated in Figure 5 and Table 3.

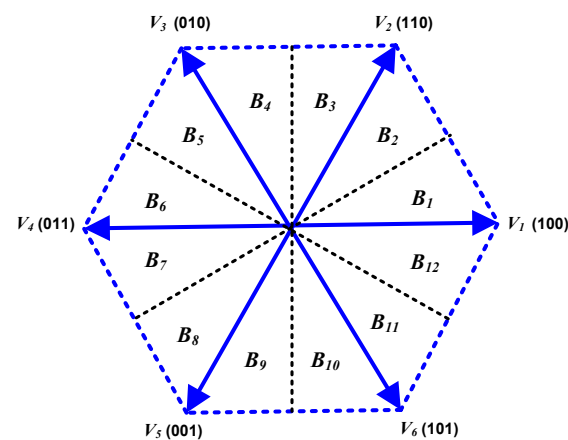


Figure 5. Regions in the hexagon of NSPWM.

Table 3. Vector definition and sequence in NSPWM.

Sector	Region	Vectors (V_x, V_y, V_z)	Sequence
1	B_1	V_1, V_2, V_6	$V_y-V_x-V_z-V_x-V_y$
	B_2	V_2, V_1, V_3	$V_y-V_x-V_z-V_x-V_y$
2	B_3	V_2, V_3, V_1	$V_y-V_x-V_z-V_x-V_y$
	B_4	V_3, V_2, V_4	$V_y-V_x-V_z-V_x-V_y$
3	B_5	V_3, V_4, V_2	$V_y-V_x-V_z-V_x-V_y$
	B_6	V_4, V_3, V_5	$V_y-V_x-V_z-V_x-V_y$
4	B_7	V_4, V_5, V_3	$V_y-V_x-V_z-V_x-V_y$
	B_8	V_5, V_4, V_6	$V_y-V_x-V_z-V_x-V_y$
5	B_9	V_5, V_6, V_4	$V_y-V_x-V_z-V_x-V_y$
	B_{10}	V_6, V_5, V_1	$V_y-V_x-V_z-V_x-V_y$
6	B_{11}	V_6, V_1, V_5	$V_y-V_x-V_z-V_x-V_y$
	B_{12}	V_1, V_6, V_2	$V_y-V_x-V_z-V_x-V_y$

3. Calculation of CMV and Switching and Conduction Losses

This section mathematically introduces the calculation of the CMV, conduction losses, and switching losses of the three-phase two-level inverter. The circuit diagram of the two-level three-phase inverter topology, consisting of six switches, is shown in Figure 2a. Due to the arrangement of these switches, each phase's pole voltage has two levels (0, V_{DC}). The pole voltages for phases A, B, and C are denoted as V_{AO} , V_{BO} , and V_{CO} , respectively. The CMV can be given as follows:

$$\text{CMV} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \quad (2)$$

For this study, the data sheet of the semiconductor IGBT, shown in Figure 6, is used to calculate the conduction and switching losses of the inverter. Figure 6a,b show the forward characteristics of the IGBT. Using these forward characteristics, the conduction loss can be calculated by multiplying the forward voltage by the current flowing through the element.

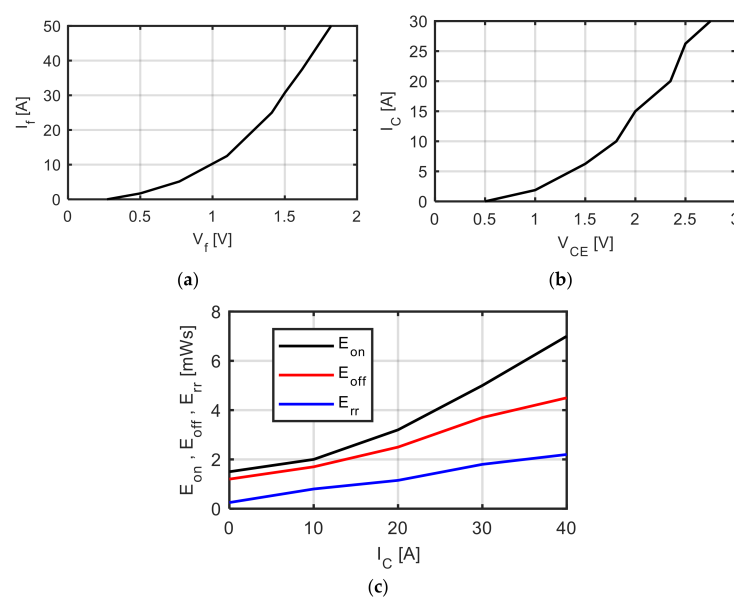


Figure 6. (a) Forward characteristics of the body diode, (b) forward characteristic of the switch, and (c) turn-on, turn-off energy loss of the IGBT and the reverse recovery energy of the diode [29].

Figure 6c shows the characteristics of the switch during turn-on and turn-off, as well as the reverse recovery energy of the diode [29–32]. The switching losses of the IGBT during turn-off (P_{SW-off}) can be given by multiplying the turn-off energy loss (E_{off}) by the switching frequency (f_{sw}), as described in (3) [30–32]. Similarly, the switching losses of the IGBT during turn-on (P_{SW-on}) can be given by multiplying the turn-on energy loss (E_{on}) by the switching frequency (f_{sw}) as described in (4) [30–32]. The switching losses of the diode (P_D) are calculated by multiplying the reverse recovery energy loss (E_{rr}) of the diode by the switching frequency (f_{sw}), as described in (5) [30–32]. Then, the total switching losses are the sum of the switching losses of all components (diodes and IGBTs). The turn-off and turn-on energy losses of the IGBT and the reverse recover energy loss of the diode are given based on the data sheet of the switch, as shown in Figure 6c. The switching losses and conduction losses are shown in Figure 7.

$$P_{SW-off} = E_{off} * f_{sw} \quad (3)$$

$$P_{SW-on} = E_{on} * f_{sw} \quad (4)$$

$$P_D = E_{rr} * f_{sw} \quad (5)$$

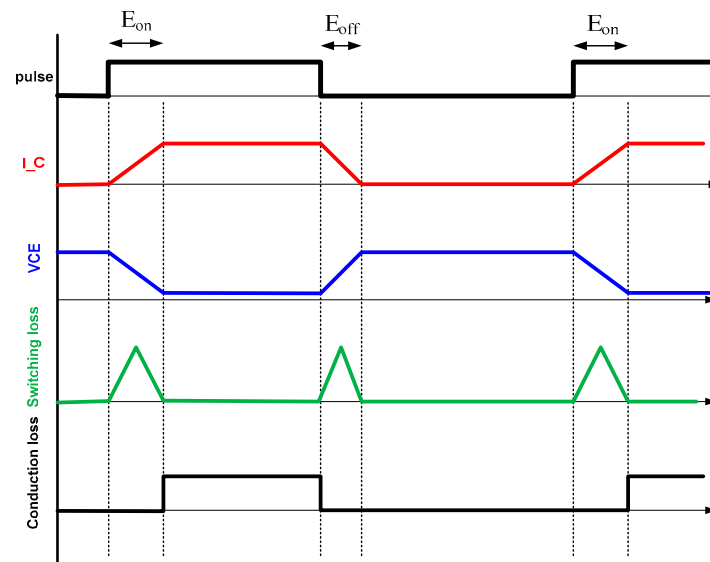


Figure 7. Calculation of switching and conduction losses.

4. Results and Discussion

This part compares the simulation and experimental results of the nine SVPWMs, focusing on the CMV, inverter losses, phase and line voltages, and current harmonics across various modulation indices ($MI = 1, 0.75, 0.5$, and 0.25). The simulation and experimental findings were evaluated under identical conditions, including a 20 kHz sampling frequency and R-L load ($R = 1.5 \, \Omega$ and $L = 0.03 \, H$). Figure 8 provides a snapshot of the experimental setup used to assess the performance of the nine SVPWM techniques. Table 4 displays the parameters used in the comparison.

Table 4. Parameters utilized in the comparison.

DC Voltage	100 V	Output Frequency	25 Hz
Load Resistance	1.5 Ω	Load Inductance	0.03 H
Sampling Frequency	20 kHz	DC-Link Capacitor	4700 μF

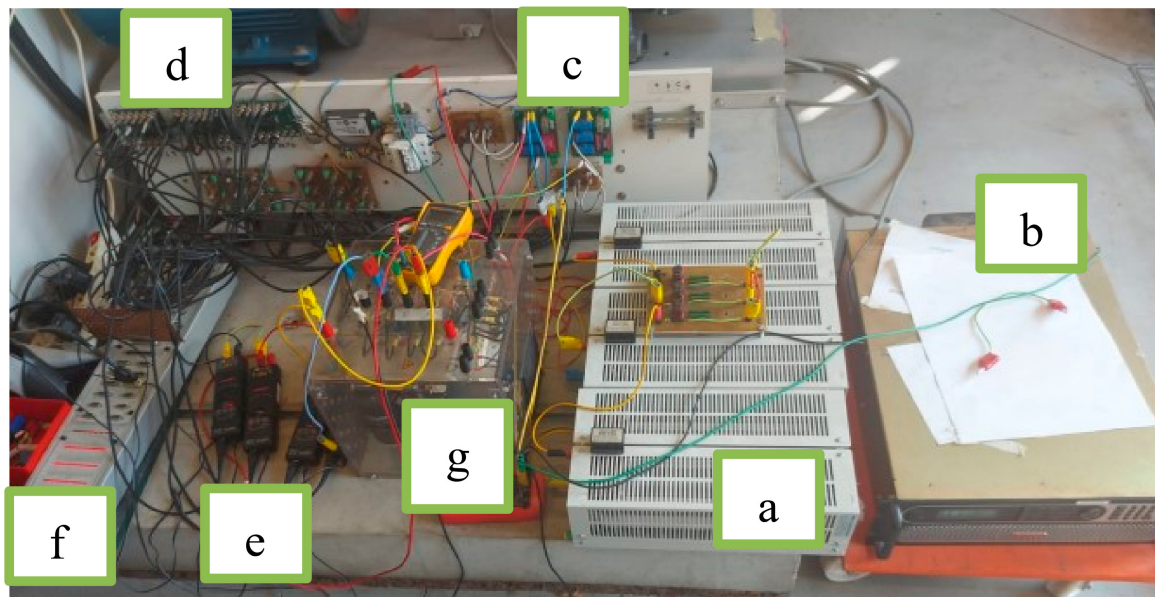


Figure 8. Picture of the experimental setup: (a) R-L load, (b) DC supply, (c) current sensors, (d) level shifters, (e) voltage probes, (f) DS 1103, and (g) three-phase two-level inverter.

4.1. CMV Comparison

This section examines the CMV under conditions of a 100 V DC-link voltage, a 25 Hz output frequency, and a unity modulation index. The modulation index does not affect the CMV; instead, the CMV is influenced by the type of SVPWM used and the value of the DC-link voltage.

Figure 9 presents a comparison between the simulation and experimental results for the CMV across the nine SVPWM techniques, all evaluated under the same conditions (100 V DC-link voltage, unity modulation index, and 25 Hz output frequency). The comparison shows an excellent match between the simulated and experimental results, confirming the accuracy of the simulations. For the standard SVPWM technique, the peak-to-peak CMV reaches 100 V. However, the DSVPM techniques (K1, K2, K3, K4, and K5) reduce the CMV by 33.33%, bringing the peak-to-peak value down to approximately 66.67 V. Among all the techniques, RSPWM stands out as the most effective, achieving a complete elimination of CMV with a peak-to-peak value of zero. Furthermore, the AZSPWM and NSPWM methods also offer significant improvements, reducing the CMV by 66.66%, resulting in a peak-to-peak value of around 33.33 V. These reductions highlight the superior performance of the modified SVPWM techniques in minimizing CMV, which is critical for improving the overall efficiency and reducing EMI in inverter-based systems.

4.2. Output Voltage Comparison

This section examines both the simulated and measured outputs of phase and line voltages under the conditions of a 100 V DC-link voltage, a 25 Hz output frequency, and a unity modulation index. The results are illustrated in Figures 10 and 11, which provide a comprehensive comparison of the performance of the nine SVPWM techniques.

Figure 10 presents a detailed comparison of the simulated and measured phase voltages for each of the nine SVPWM techniques. This figure illustrates the degree of agreement between the simulation results and experimental measurements, demonstrating that the simulations accurately predict the phase voltage behavior. Similarly, Figure 11 focuses on the comparison of simulated versus measured line voltages. This figure shows how closely the experimental results align with the simulated data, further validating the accuracy of the simulations. Overall, both Figures 10 and 11 confirm an excellent correlation between the simulation results and experimental measurements, highlighting the reliability and precision of the simulation model in representing the actual performance of the SVPWM

techniques. This agreement underscores the effectiveness of the simulation approach in accurately predicting the behavior of the inverter systems under the specified conditions.

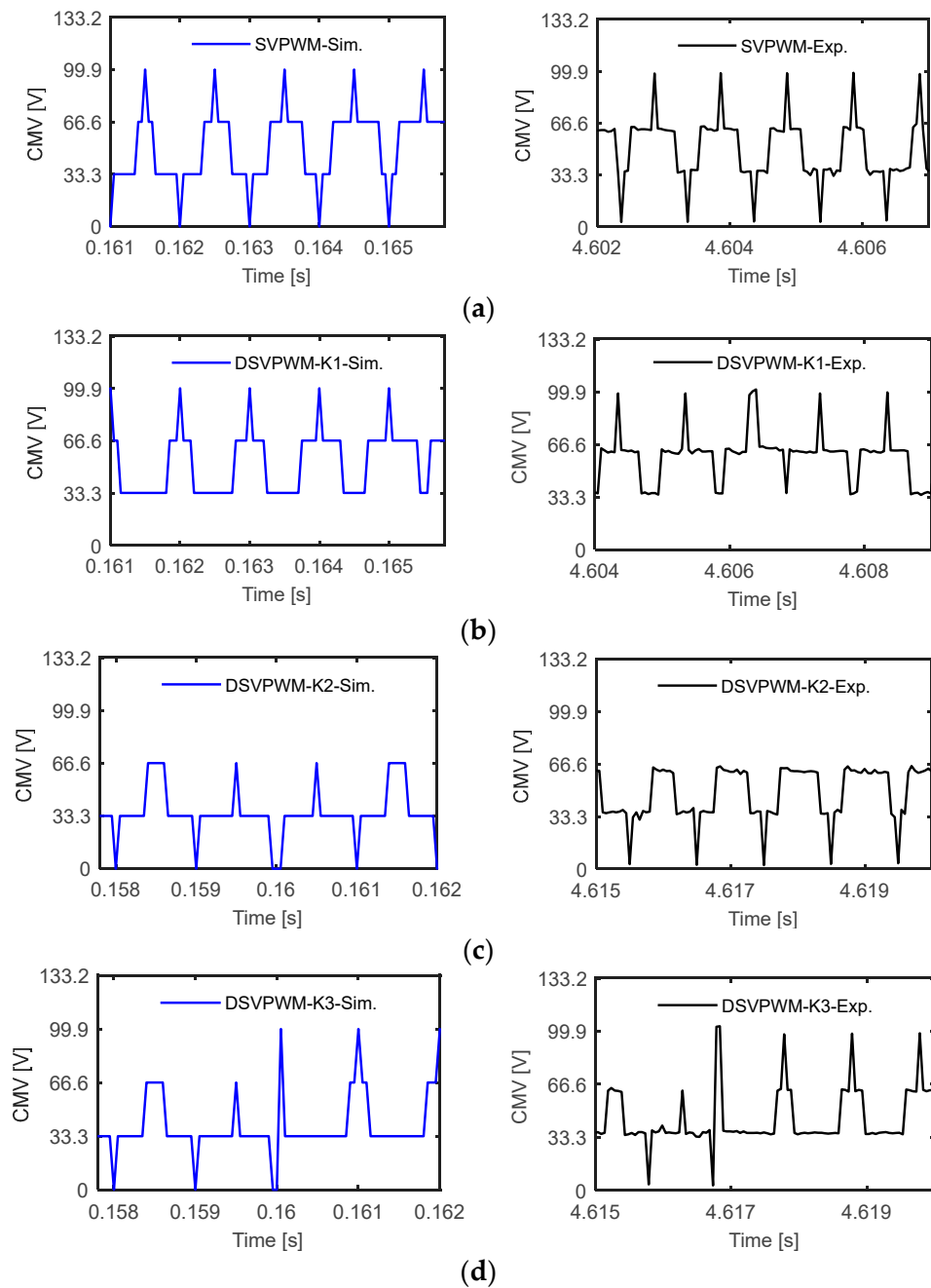


Figure 9. Cont.

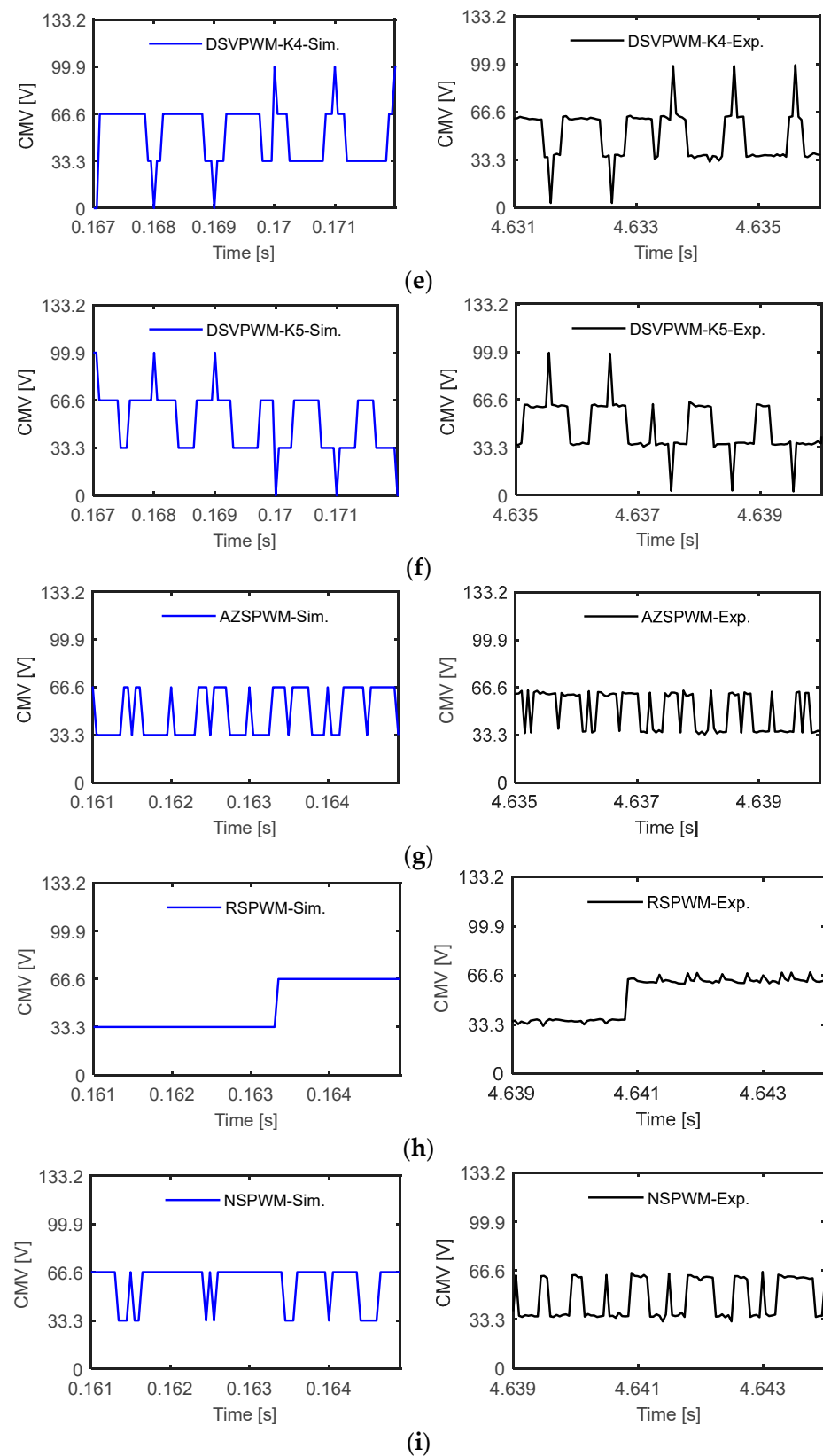


Figure 9. Measured (Exp.) and simulated (Sim.) results of the CMV at 25 Hz and unity modulation index for (a) SVPWM, (b) DSVPWM-K1, (c) DSVPWM-K2, (d) DSVPWM-K3, (e) DSVPWM-K4, (f) DSVPWM-K5, (g) AZSPWM, (h) RSPWM, and (i) NSPWM.

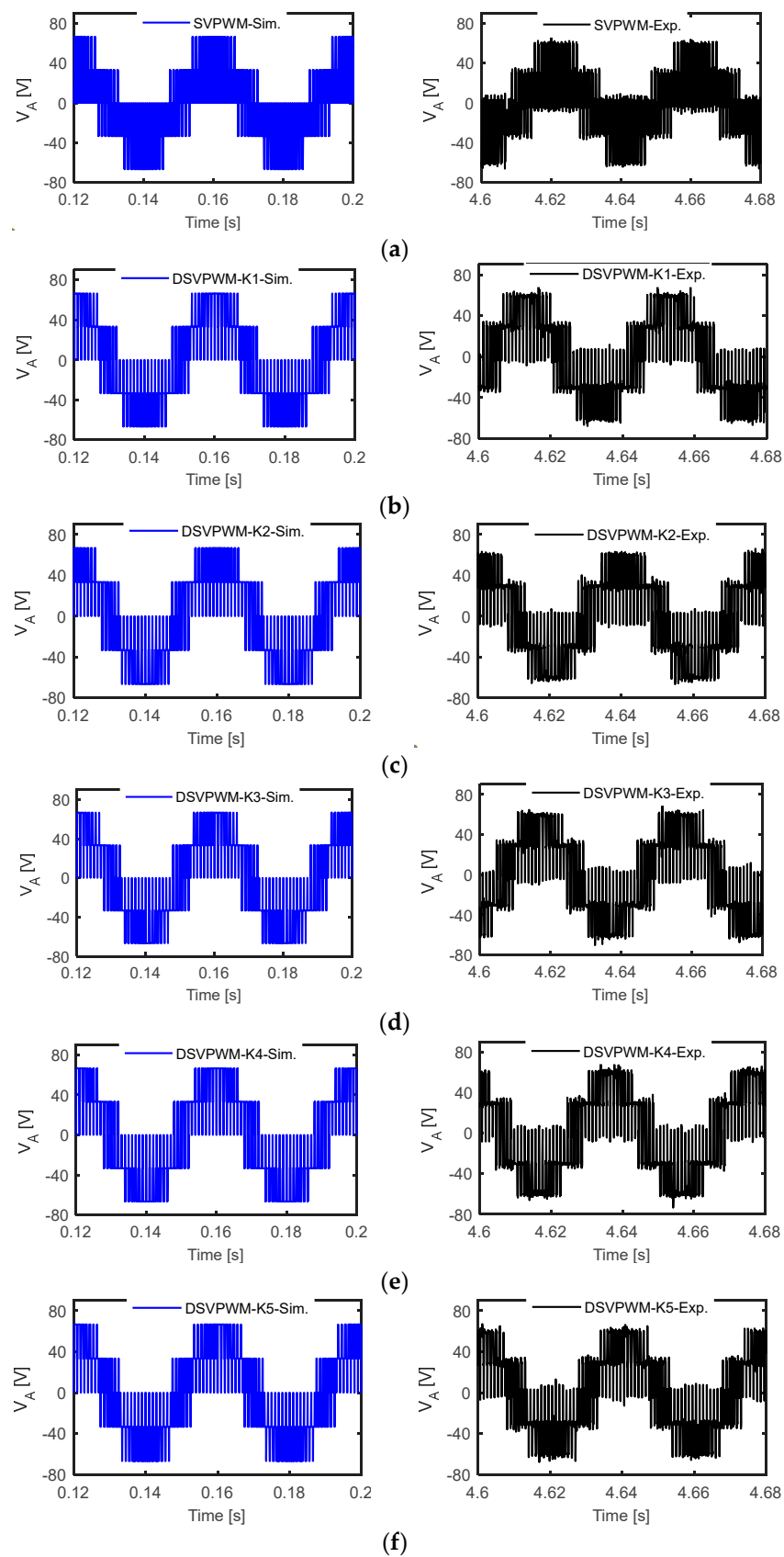


Figure 10. Cont.

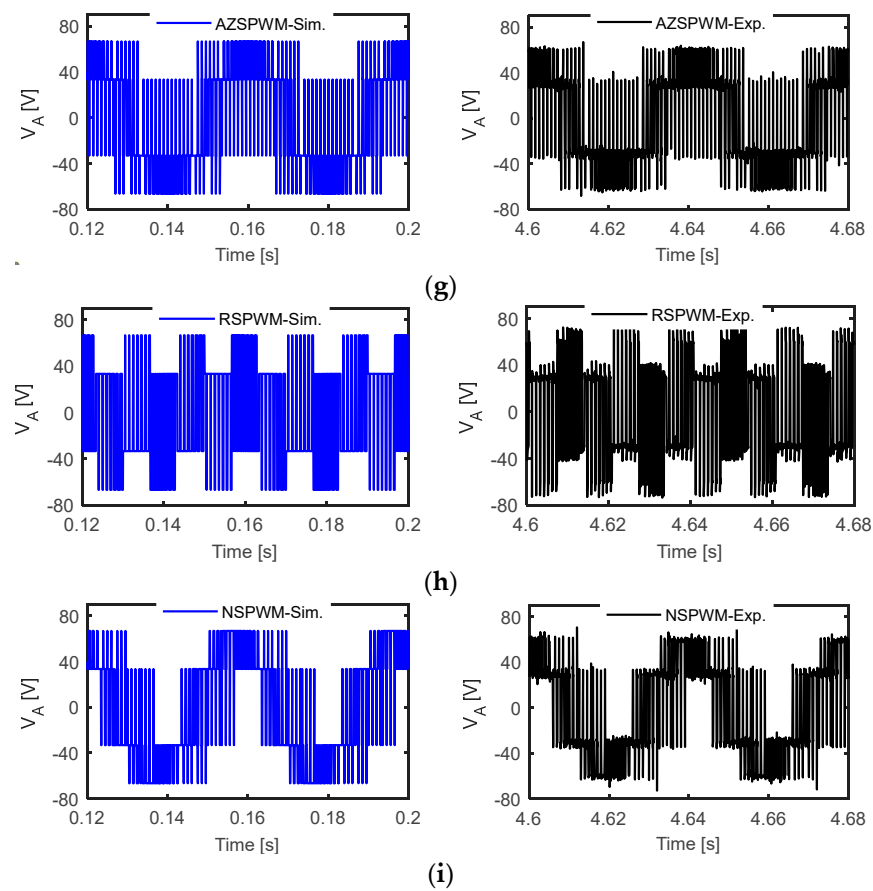


Figure 10. Measured (Exp.) and simulated (Sim.) results of the phase voltage V_A at 25 Hz and unity modulation index for (a) SVPWM, (b) DSVPM-K1, (c) DSVPM-K2, (d) DSVPM-K3, (e) DSVPM-K4, (f) DSVPM-K5, (g) AZSPWM, (h) RSPWM, and (i) NSPWM.

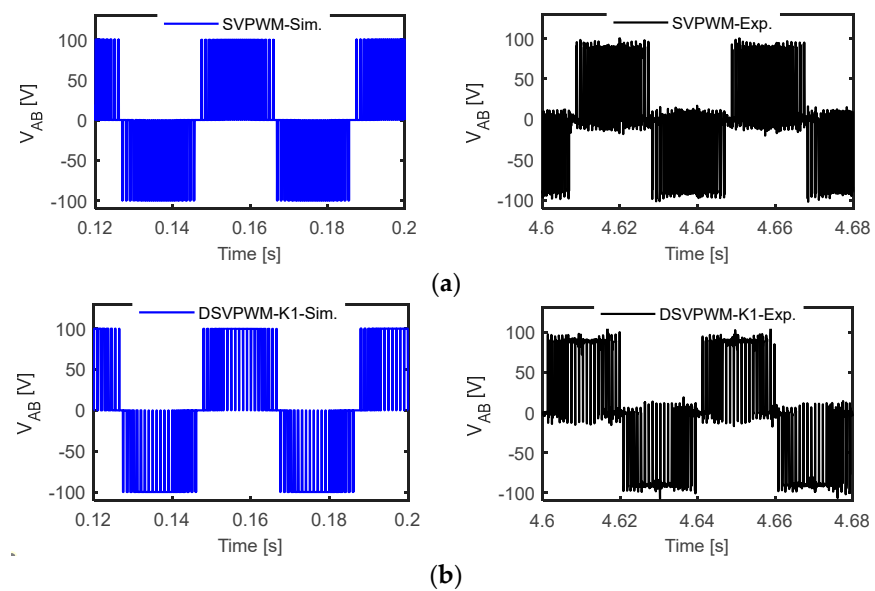


Figure 11. Cont.

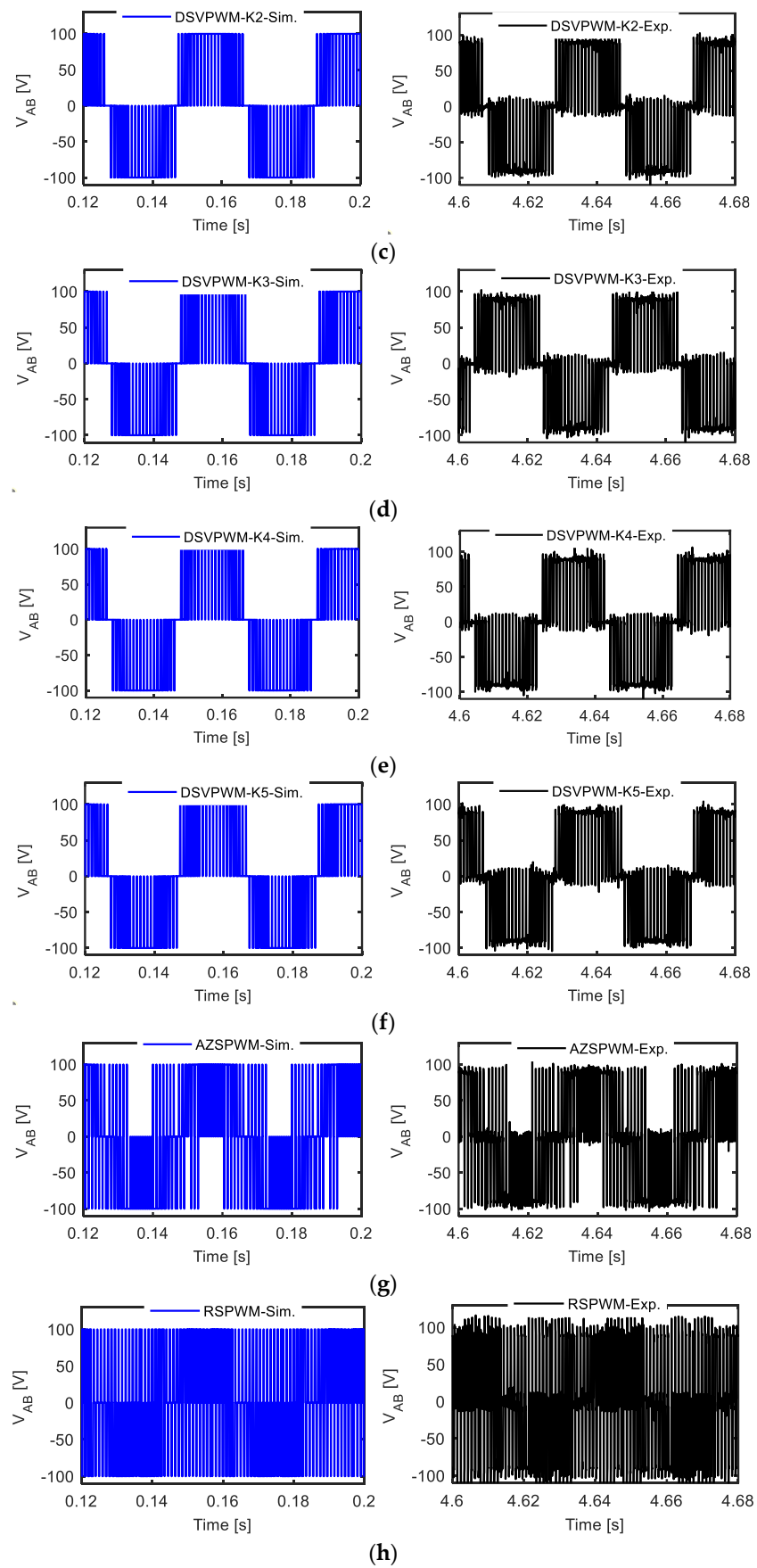


Figure 11. Cont.

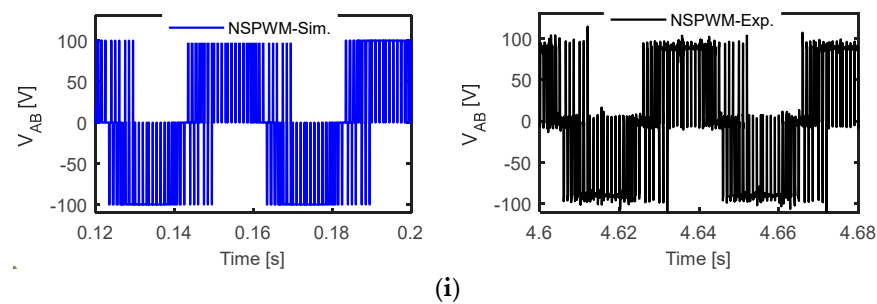


Figure 11. Measured (Exp.) and simulated (Sim.) results of the line voltage V_{AB} at 25 Hz and unity modulation index for (a) SVPWM, (b) DSVPWM-K1, (c) DSVPWM-K2, (d) DSVPWM-K3, (e) DSVPWM-K4, (f) DSVPWM-K5, (g) AZSPWM, (h) RSPWM, and (i) NSPWM.

4.3. Output Current and THD Comparison

This section delves into the analysis of output phase currents and their THD. Figure 12 presents a detailed comparison of simulated and measured output phase currents for the nine SVPWM techniques, evaluated under consistent conditions: a unity modulation index, a 100 V DC-link voltage, and a 25 Hz output frequency. The results illustrate a remarkable agreement between the simulated and experimental data, validating the accuracy of the simulation model. Figure 12h highlights that the RSPWM technique demonstrates suboptimal phase current performance at a unity modulation index, resulting in a notably higher THD compared to the other techniques. This observation underscores the significant influence of the modulation index on the THD of phase currents. To further investigate this dependency, Figure 13 explores the THD of the output phase currents across various modulation indices for the nine SVPWM techniques. At a unity modulation index, as depicted in Figure 13a, RSPWM exhibits the highest THD, while DSVPWM-K3 achieves the lowest THD. When the modulation index is reduced to 0.75, shown in Figure 13b, RSPWM's THD decreases but remains the highest among the techniques. In contrast, DSVPWM-K1 and DSVPWM-K2 demonstrate the lowest THD at this modulation index. At a modulation index of 0.5, illustrated in Figure 13c, NSPWM exhibits the highest THD, whereas DSVPWM-K3 maintains the lowest. Similarly, at a modulation index of 0.25, depicted in Figure 13d, RSPWM continues to have the highest THD, with DSVPWM-K3 again showing the lowest. Figure 14 further consolidates these findings by presenting THD values across different modulation indices for various SVPWM techniques. Both Figures 13 and 14 emphasize that the THD of the output phase current is highly sensitive to the modulation index value. This sensitivity highlights the critical role of selecting an appropriate modulation index to optimize THD performance and enhance the overall efficiency of SVPWM techniques.

4.4. Inverter Loss Comparison

This section evaluates and compares the total inverter losses, which include both switching and conduction losses, across various SVPWM techniques at different modulation indices and a 25 Hz output frequency. Figure 15 provides a comprehensive analysis of these losses, highlighting the performance of the nine SVPWM techniques. Figure 15a specifically presents the inverter losses at a unity modulation index. It is evident that the RSPWM technique exhibits the lowest total inverter losses among the techniques. However, this advantage comes with a trade-off, as RSPWM also displays significantly higher harmonic distortion in the output phase currents, as noted in Figure 13a. Consequently, despite its lower inverter losses, RSPWM is not deemed the optimal control method at a unity modulation index due to its higher THD.

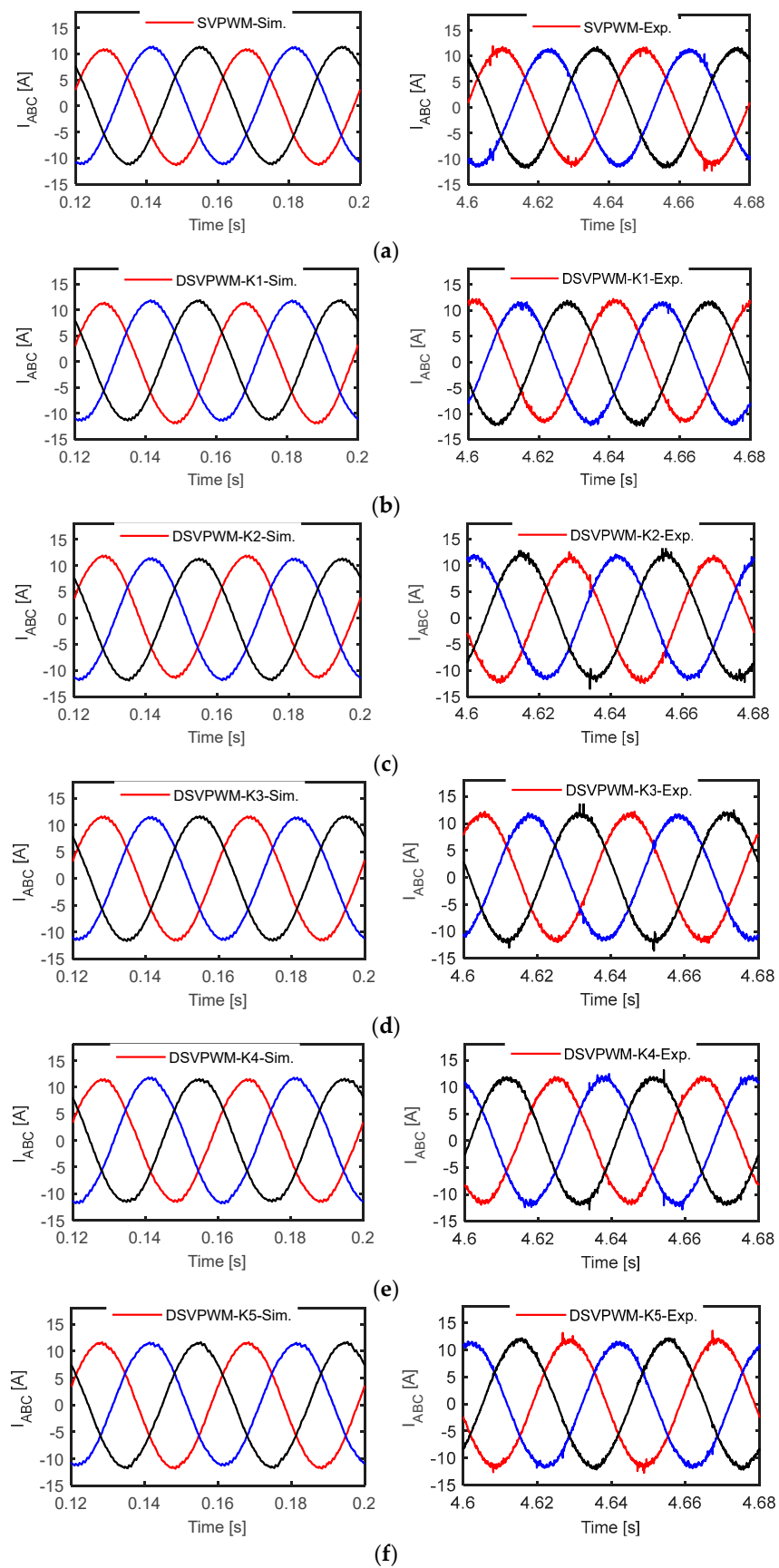


Figure 12. Cont.

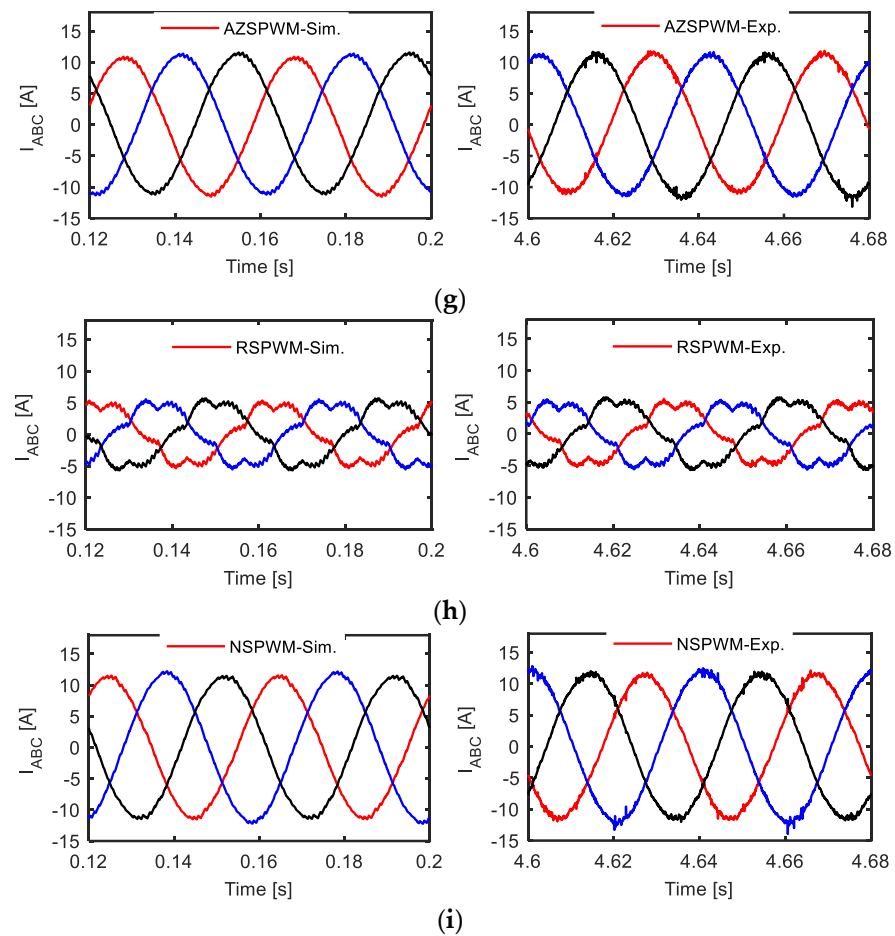


Figure 12. Measured (Exp.) and simulated (Sim.) results of the three-phase currents I_{ABC} at 25 Hz and unity modulation index for (a) SVPWM, (b) DSVPM-K1, (c) DSVPM-K2, (d) DSVPM-K3, (e) DSVPM-K4, (f) DSVPM-K5, (g) AZSPWM, (h) RSPWM, and (i) NSPWM.

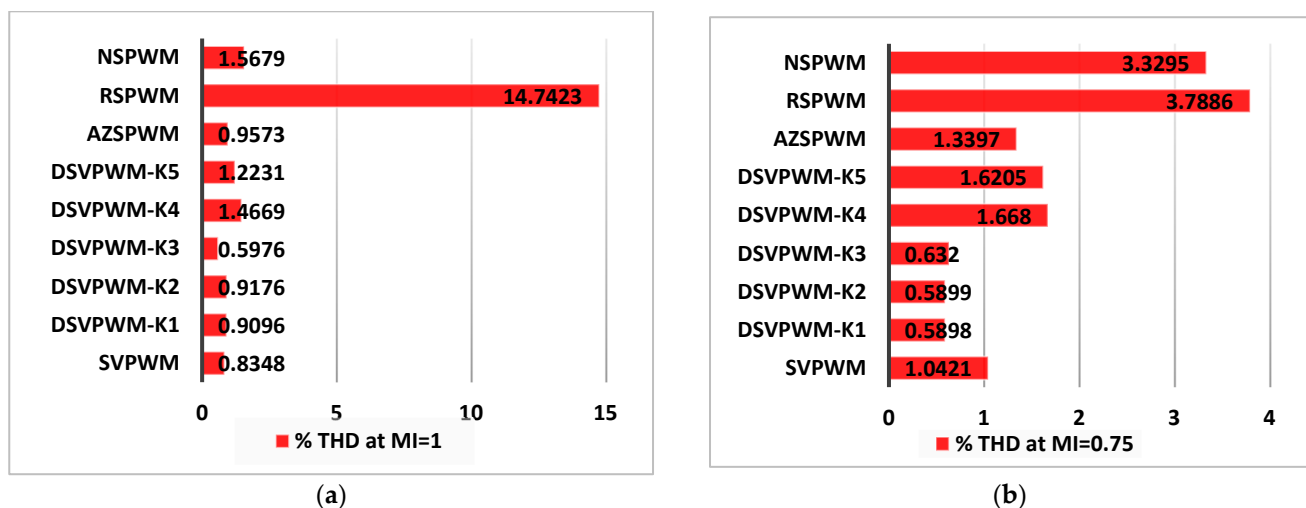


Figure 13. Cont.

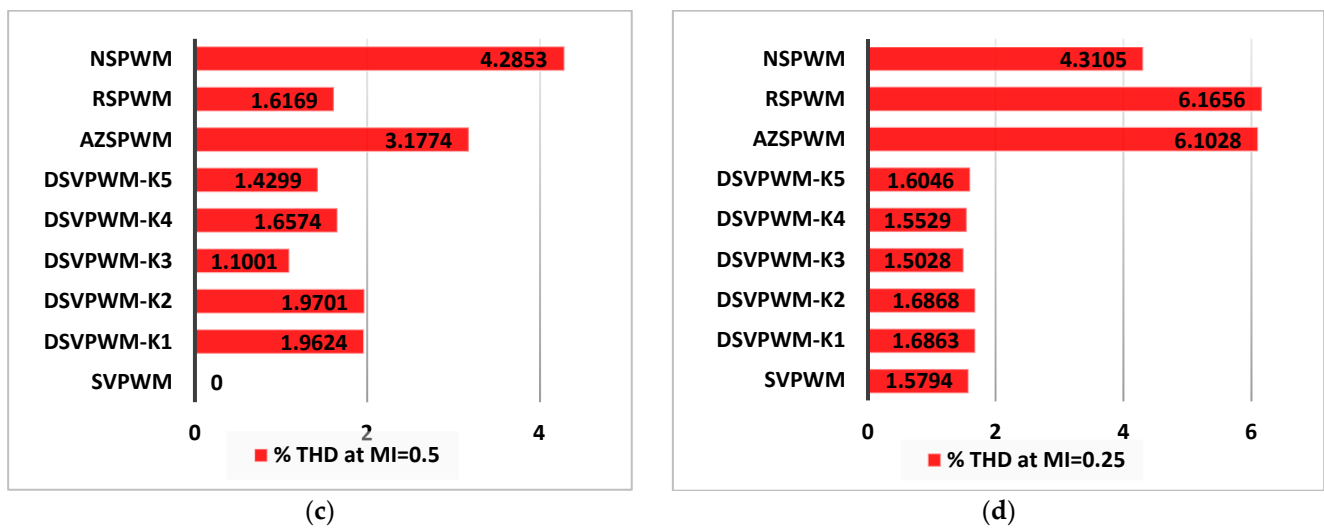


Figure 13. The mean value of the % THD of the three-phase currents at a 25 Hz output frequency and a modulation index (MI) of (a) 1, (b) 0.75, (c) 0.5, and (d) 0.25.

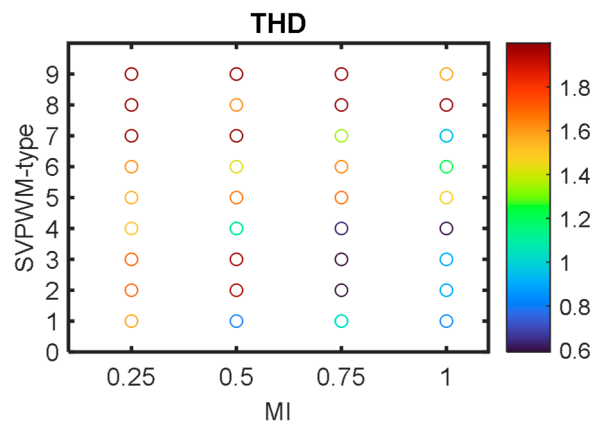


Figure 14. The mean value of the % THD of the three-phase currents at a 25 Hz output frequency at different modulation index (MI) values and different SVPWMs methods.

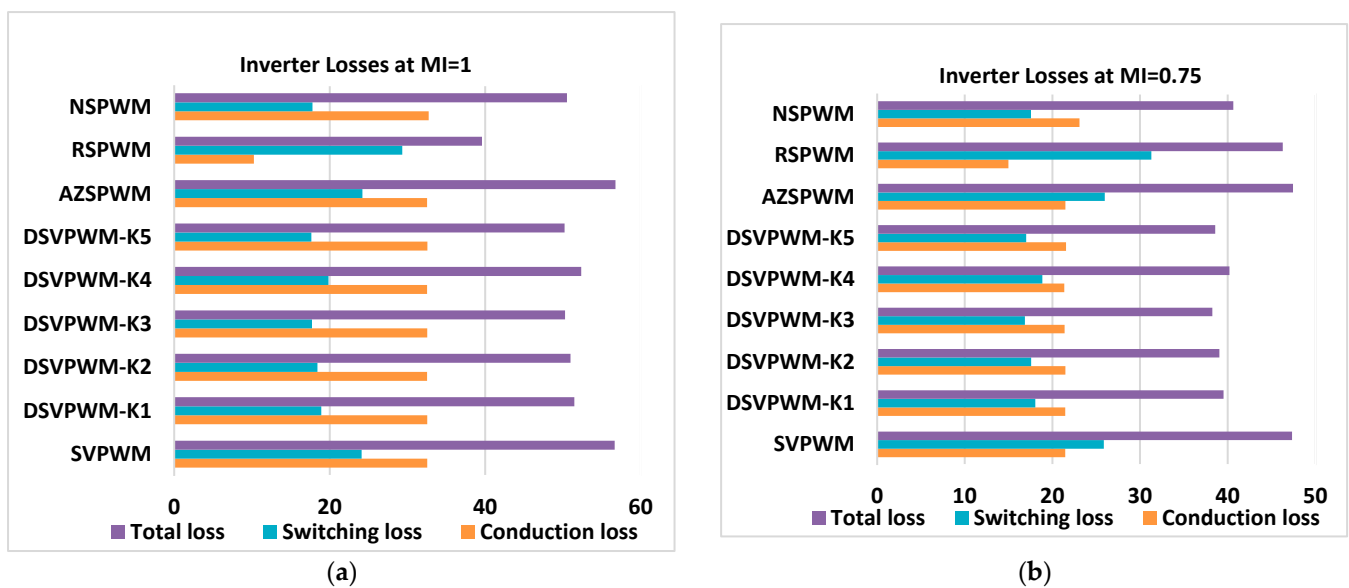


Figure 15. Cont.

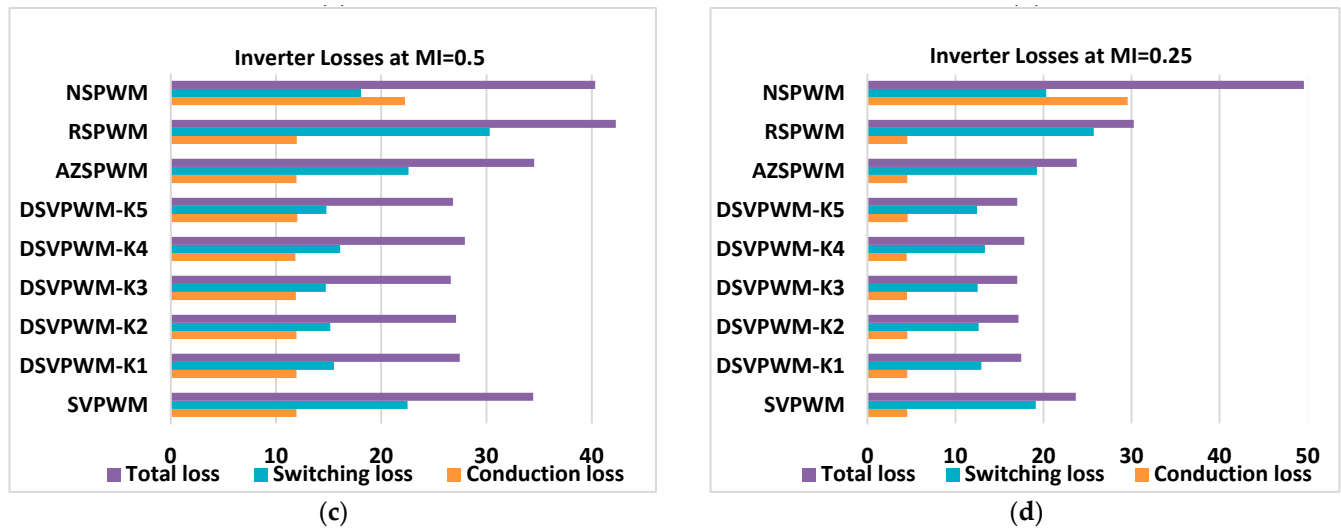


Figure 15. Inverter losses at a 25 Hz output frequency and a modulation index (MI) of (a) 1, (b) 0.75, (c) 0.5, and (d) 0.25.

Further analysis across different modulation indices is provided in Figure 15b–d, in conjunction with Figure 13b–d. These figures collectively indicate that DSVPM-K3 emerges as the optimal technique in terms of minimizing both inverter losses and THD across modulation indices of 1, 0.75, 0.50, and 0.25. However, it is important to note that DSVPM-K3 is ranked third for CMV reduction, as shown in Figure 9. Figure 16 extends this comparison by illustrating the inverter losses for a three-phase inverter across various modulation indices and SVPWM techniques. The data reveal that DSVPM-K3 and DSVPM-K5 consistently deliver the lowest inverter losses across all modulation indices, reinforcing their overall efficiency in comparison to other techniques.

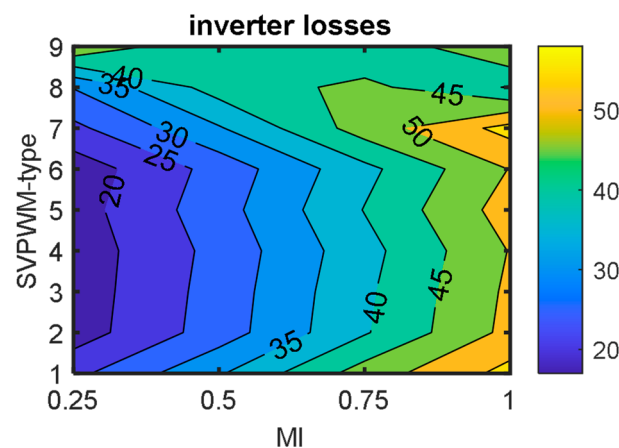


Figure 16. Inverter losses at a 25 Hz output frequency at different modulation index (MI) values and different SVPWMs methods.

5. Conclusions

This paper compared nine SVPWM techniques designed to reduce CMV, inverter losses, and harmonic currents. The comparison was carried out using both MATLAB R2023a simulation and experiment validation under identical conditions, including a sampling frequency of 20 kHz and various modulation indices of 1, 0.75, 0.5, and 0.25. In this comparison, an excellent agreement between the simulation and experimental data was found. The conclusions drawn from this comparison are as follows:

- RSPWM demonstrates the lowest CMV, with a zero peak-to-peak value across different modulation indices. However, RSPWM is only suitable for lower modulation indices

(0.25 and 0.5) due to its higher harmonics in the phase currents at higher modulation index values.

- AZSPWM offers optimal performance at high modulation indices (1 and 0.75). It achieves a CMV reduction of 66.66% compared to continuous SVPWM and offers significantly lower THD in the output phase current compared to RSPWM at a high modulation index. RSPWM matches AZSPWM in CMV performance and offers lower inverter losses at high modulation indices. However, NSPWM has nearly double the THD value in the output phase current compared to continuous SVPWM.
- DSVPMW-K1, K2, K3, K4, and K5 offer a 33.33% reduction in CMV compared to continuous SVPWM. These discontinuous SVPWM techniques have shown lower inverter losses compared to SVPWM. Among them, DSVPMW-K3 provides a good compromise by achieving lower inverter losses, a reduced THD of the output phase current, and lower CMV across various modulation indices.

Author Contributions: Conceptualization, K.B.T.; methodology, K.B.T.; software, K.B.T.; validation, K.B.T.; investigation, K.B.T.; writing—original draft preparation, K.B.T. and A.S.M.; writing—review and editing, A.S.M. and P.S.; visualization, A.S.M. and P.S. All authors have read and agreed to the published version of the manuscript.

Funding: The authors acknowledge the Flanders Make SBO project EBearDam at Ghent University, Belgium, and Khalifa University, United Arab Emirates, under Award No. KAU-KU-2021-01 for financial support during this work.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: Authors Kotb B. Tawfiq and Peter Sergeant were employed by the FlandersMake@UGent—Corelab EEDT-MP. The remaining author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest. The FlandersMake@UGent—Corelab EEDT-MP had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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