Rectifier Optimization for Low-Power RF Energy Harvesting Tags

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***Abstract*—An optimization technique is proposed for the design of highly efficient radio frequency (RF) rectifiers at low power levels. Therefore, a ”Thru-Reflect-Line” calibration kit is designed and used for the de-embedding of the SMS7630-005LF series pair Schottky diodes. Based on these measurements an accurate equivalent circuit is proposed, including all parasitic losses that are introduced from the package and the interconnects in the actual application. This equivalent model is used to design a compact and low-cost rectifier for operation in the 2.45 GHz band. This rectifier employs a lumped component L-type matching network and achieves a power conversion efficiency of 13% and 35% at -20 dBm and -10 dBm, respectively. The proposed rectifier can be seamlessly integrated in active radio frequency identification (RFID) tags to extend their lifetime and improve their performance.**

I. Introduction

In the past decade, the rise of radio frequency identification (RFID) shows increasing interest in far-field wireless power transfer [1]. RFID tags rely on the radio frequency (RF) signal from a reader for both power and communication. More advanced RF energy harvesting (EH) that scavenges power from ambient or intentional RF signals, can enable the development of self-sufficient active RFID systems in the near future. Therefore, more compact and low-cost RF rectifiers are needed to efficiently convert low RF input powers into DC power. Schottky diodes remain the predominant non-linear element for this conversion, although their performance is limited at low input powers, due to the junction potential (V_j), and also at high input powers, due to the breakdown voltage (V_b). It is challenging to accurately model and optimize these RF rectifiers in combination with lumped component matching networks because of the non-linear behaviour of the Schottky diodes. In [2], it is mentioned that a real diode requires a combination of parasitic capacitors and inductors to accurately model the package of the semiconductor device. In this paper, the SMS7630-005LF series pair Schottky diodes is characterized in a novel way by including all the parasitic losses that are introduced by the package and the interconnects.

II. Proposed Rectifier Design

A. Design Methodology

In order to simulate, optimize and design a compact and highly efficient rectifier, an accurate simulation model of the equivalent circuit of the Schottky diode is required. The Shockley diode model, often used for characterizing Schottky diodes, already includes parasitic losses due to the junction capacitance (C_j) and series resistance (R_s) [3]. These parameters are therefore often provided by the manufacturer, but are not sufficient to create an accurate model of the complete Schottky diode. Extra parasitic losses can be introduced by the package and should be accurately modelled. In addition, there can be deviations on the parameters, drastically influencing the electromagnetic characteristics of the Schottky diode.

One solution is measuring the S-parameters of the Schottky diode under different bias voltages. To this end, a well-designed ”Thru-Reflect-Line” (TRL) calibration kit is needed to de-embed of the connector and transmission line [4]. Based on these measurement results, the parasitic losses due to packaging can be incorporated in the equivalent circuit.

B. De-embedding and Equivalent Circuit

A TRL kit with a characteristic impedance of 50 Ω is designed and manufactured on low-cost FR4 substrate, IS400, with a dielectric constant ϵ_r of 3.9 and a loss tangent $tan(\delta)$ of 0.022. A two-layer design is used with a substrate height of 1.55 mm and a metal thickness of 35 µm. For the 50 Ω transmission line, a grounded coplanar waveguide is designed having a width of 2.66 mm and a gap of 0.8 mm, resulting in an $\epsilon_{r,eff}$ of 2.747 and a characteristic impedance of 50.06 Ω. The Thru, Reflect and Line have a length of 40 mm, 20 mm and 58.5 mm, respectively. The 18.5 mm length difference corresponds to a phase difference of 90° at 2.45 GHz and a propagation delay of 102.3 ps.

To accurately measure the non-linear behaviour of the diode, a bias tee is connected between the Vector Network Analyzer and the Schottky diode. Next, multiple small-signal measurements are performed at different bias voltages. These measurement results are shown on the Smith diagram in Fig. 1. The applied bias voltages are chosen such that the non-linear behaviour can be accurately incorporated in the equivalent circuit. From the results in Fig. 1 it is observed that the diode starts to conduct from around 140 mV and becomes more inductive when the bias voltage is further increased.

Based on the measured data in Fig. 1, the equivalent circuit of the SMS7630-005LF can be constructed, as is depicted in Fig. 2. To account for additional diode parasitics, a series inductor and shunt capacitor are added to each Schottky diode in the model. In addition, each pin of the SOT-23 package is modelled as a short transmission line with an extra series inductor, series resistance and shunt capacitor to model the parasitic losses introduced by the interconnect. The optimized values of these components are shown in Fig. 2. Moreover, it was necessary to decrease the series resistance R_s from 20 Ω to 10 Ω to get an optimal agreement with the measured data.

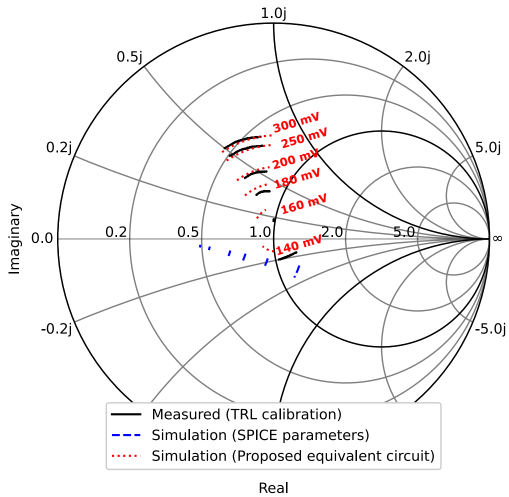

Fig. 1: Smith diagram with S_{11} from 2 to 3 GHz for the SMS7630-005LF.

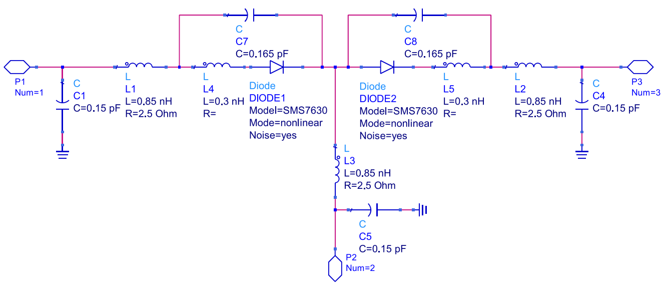

Fig. 2: Proposed equivalent circuit for the SMS7630-005LF series pair Schottky diodes.

C. Proposed Rectifier Design

The proposed rectifier design consists of a voltage doubler with the SMS7630-005LF series pair Schottky diodes in a SOT-23 package and an L-type lumped component matching network to keep the design low-cost and compact [5]. The matching network consists of two RF inductors from the Murata LQG15HS_02 series in a 0402 package. The two RF capacitors in the voltage doubler are from the Murata GQM series in a 0603 package. Both series have a Keysight PathWave Advanced Design System (ADS) library available, which is included in the simulation model.

The complete PCB layout, depicted in Fig. 3(b), was fully simulated with ADS and co-designed with the equivalent circuit of the Schottky diodes and all the discrete components, in order to obtain optimal and very accurate simulation results. The power conversion efficiency (PCE) of the rectifier is specifically optimized for very low RF input powers, ranging from -30 dBm to -10 dBm.

The simulation and measurement results of the output voltage and PCE at the center frequency of 2.45 GHz for an optimal load resistance of 4.7 kΩ are shown in Fig. 4. The achieved PCE for very low input powers, ranging from -30 dBm to -10 dBm, is exceptionally high for this proposed rectifier design with a lumped component matching network

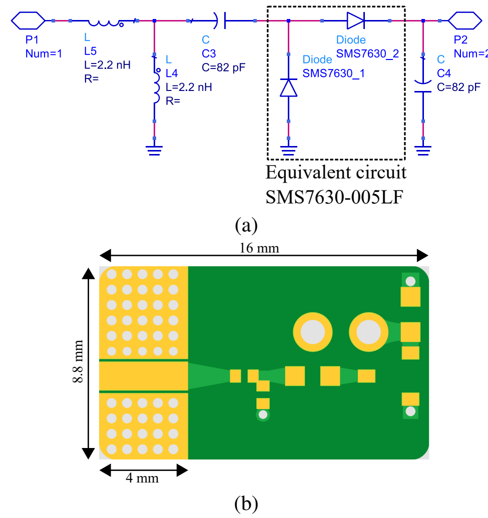

Fig. 3: (a) Schematic of the proposed voltage doubler topology and (b) layout of the proposed rectifier design.

and fabricated on low-cost FR4 substrate. A minimal increase in PCE and output voltage can be noticed in the measurement results and can be explained by the fabrication tolerances on the discrete components. Overall, the simulation results correspond very well with the measurement results.

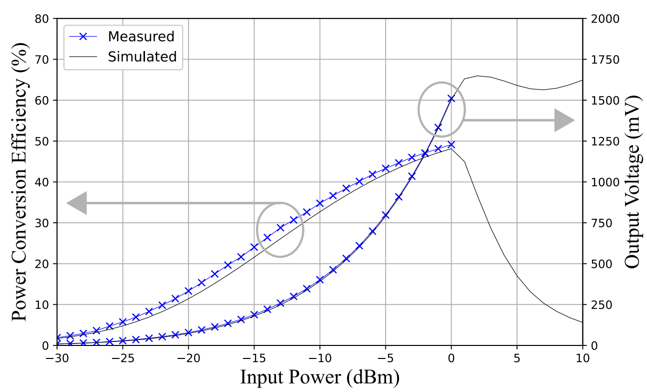

Fig. 4: Simulated and measured efficiency (%) and output voltage (mV) as a function of input power (dBm) at 2.45 GHz.

ACKNOWLEDGEMENT

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