Source/Drain Epitaxy For Nanosheet-based CFET Devices

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This work reports the progress in source/drain (S/D) epitaxy development for nanosheet-based monolithic complementary field effect transistors (mCFET). S/D processes which were set-up for bulk finFET devices can be easily transferred to mCFET devices. Owing to the complicated integration and small dimensions of the highly scaled structures however, more attention is required for the pre-epi cleaning of the exposed channel interfaces and for the additional defectivity that arises from the merging of individual epitaxial growth fronts. Low-temperature epi processes can be structurally integrated in mCFET devices, to further reduce the transistor access resistance components and comply with thermal budget limitations.

Introduction

The complementary field-effect transistor (CFET) is an attractive device architecture for beyond 1 nm CMOS technology nodes where n- and p-MOS nanosheet devices are placed on top of each other and hereby allowing for a further density scaling (1-6). Various CFET implementations are considered including monolithic or sequential approaches and each of them has its own strengths/challenges. The sequential approach is based on the processing of individual n- and p-MOS transistors vertically stacked by wafer-to-wafer bonding while in the monolithic case (mCFET) all transistors are built on the same wafer. Even for mCFET, different integration schemes exist depending on whether the contact to the bottom device is made from the frontside (so-called Metal-Diffusion-first approach (MD-first)) (4,5) or from the backside (6,7).

The choice of the integration scheme has obviously important consequences for the details of the nanosheet stack and related epi processes (8,9) but also for the epi source/drain (S/D) epitaxy processes that can be used for the bottom and top devices. For MD-first integration (see schematic in Fig. 1), the presence of the metal contact to the bottom S/D (B-S/D) constraints the thermal budget of the top S/D (T-S/D) and introduces a risk of metal exposure during epi processing, in case the isolating oxide layer (ISO) is marginal. When using a BS contacting method on the other hand, both B-SD and T-S/D are present before contact metallization which reduces the thermal budget and contamination concerns. In the following, we will further concentrate on the p- and n- S/D epitaxy aspects.

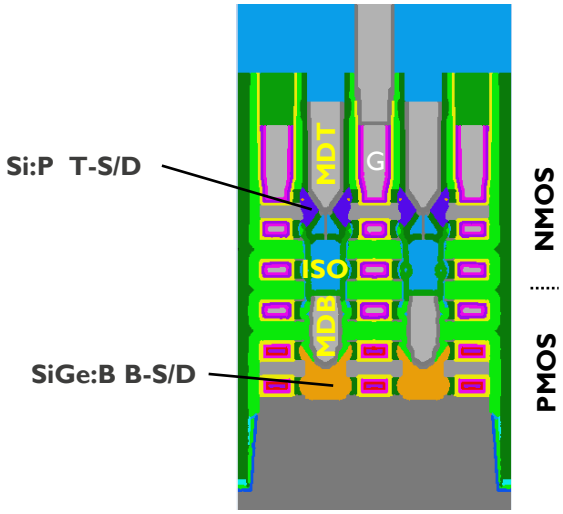

Figure 1. Schematic X-section of a mCFET stack assuming MD-first integration. A 1×1 stack is shown which has only 1 Si nanosheet for n-MOS and p-MOS respectively. The S/D of the p-MOS at the bottom is separated by an isolating layer (ISO) from the S/D of the n-MOS top device while the channels are isolated by a middle dielectric isolation.

Experimental

The S/D layers were epitaxially grown by RP-CVD in a 300 mm production compatible epi cluster (ASM Intrepid® ES™). For assessments on blanket wafers, the native oxide was removed *in situ* by a thermal treatment at a sufficiently high temperature (>1000°C). For the pre-cleaning of the nano-sheets before epi growth, we rely on a combination of wet and low-temperature in situ Previum™ cleans (10). Pre-epi bake was omitted to avoid dummy gate crystallization. For both types of S/D layers (p- and n-doped), two sets of process conditions have been assessed. For the high temperature (HT) co-flow S/D processes, conventional precursor gases enabling selective epitaxial growth, are used (11,12) while for the LT processes, with T ≤ 525ºC, higher order precursors are typically used in cyclic-deposition-etch (CDE) mode (13,14). For the highly P-doped layers, a wet oxidizing treatment was given to the wafers after processing to prevent further PH_x outgassing of the wafers.

A broad range of characterization techniques were used to assess the properties of the S/D layers. Before implementing the different layers in the patterned CFET device structures, blanket layer characterization was done using Atomic Force Microscopy (AFM), Secondary Ion Mass Spectroscopy (SIMS), High-Resolution X-ray Diffraction (HRXRD), cross-section Transmission Electron Microscopy (X-TEM). Sheet resistance and active carrier concentrations were measured by micro-four-point probe (m4pp) and micro-Hall Effect (MHE), respectively (15) while contact resistivity is assessed by using the Circular Transmission Line Method (CTLM) (16). After integration of the layers in the CFET device wafers, Top-View Scanning Electron Microscopy (TV-SEM), In-line X-TEM and Energy-Dispersive X-ray Spectroscopy (EDS) were typically used to characterize S/D layer properties.

Results and Discussion

P-type S/D epitaxy

Figure 2 shows X-TEM examples for the integration of a co-flow SiGe:B layer ([Ge]~ 60%), which was previously used for bulk finFET devices (12), into nanosheet and mCFET structures with 48 nm and 60 nm contacted poly pitch (CPP), respectively (gate dimension Lg ~ 18-20 nm). The SiGe:B growth happened from the different Si sheets and from the Si bulk. Twin defects can be observed due to the merging of neighboring and opposing sheets.

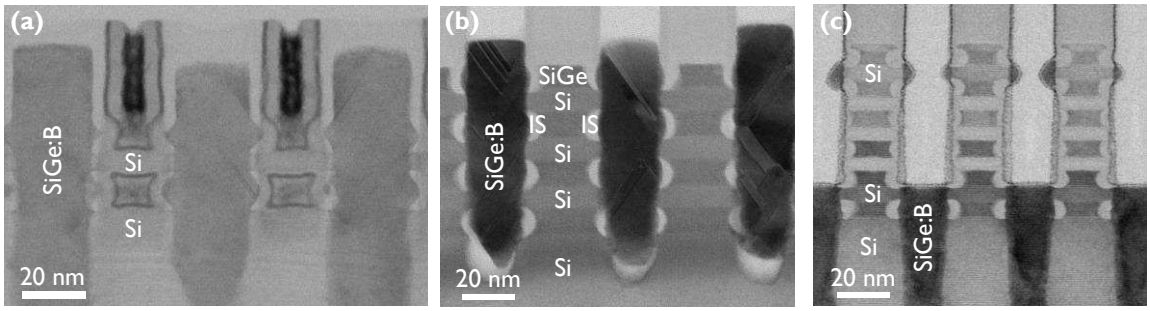

Figure 2. X-TEMs of (a) SiGe:B S/D growth ([Ge] ~ 60%) in a 48 nm CPP nanosheet stack with 1 Si sheet after metal gate replacement, (b) with 3 Si sheets after epitaxy, and (c) in a 60 nm CPP 1×1 CFET stack. SiN dielectric is used as inner-spacer (IS) material (5).

Compared to bulk FinFETs, the density of defects is clearly increased. For the bottom S/D in 1×1 CFET structures with single nanosheets (Fig. 2(c)), the majority of the SiGe:B was grown from the Si bulk which then merged with the growth fronts from the single sheets. Some parasitic SiGe:B epi can be observed on the top-Si sheets, which was removed later in the process flow.

Figure 3(a) compares specific Ti/SiGe:B contact resistivity (ρ_c) levels obtained using CTLM structures for the co-flow SiGe:B processes used in Fig. 2 and LT SiGe:B (17,18). Results are plotted as a function of the material resistivity (ρ) for fair comparisons. While conventional co-flow processes give a ρ_c down to ~ 4×10^{-9} Ω.cm^2 for a $[B]_{act}$ up to ~7×10^{20} cm^{-3}, the values are clearly above those obtained with LT-SiGe:B. A minimal ρ_c of ~ 2×10^{-9} Ω.cm^2 is demonstrated with $[B]_{act} = 2.5\times10^{21}$ cm^{-3} for LT-$Si_{0.5}Ge_{0.5}$:B. By reducing the epi temperatures below 400ºC and by optimizing the Ge concentration as well as the precursor choice, the active doping levels can even be further increased beyond the values quoted above (19). Fig. 3(b) and (c) show X-TEM examples of highly active LT-SiGe:B layers which are integrated into a 48 nm CPP nanosheet stack with 1 Si sheet and a 60 nm CPP 1×1 CFET stack, respectively. These figures demonstrate that these epitaxial growth schemes with high active doping concentrations are selective against oxide and nitride surfaces and that they can be integrated into NS and CFET device structures.

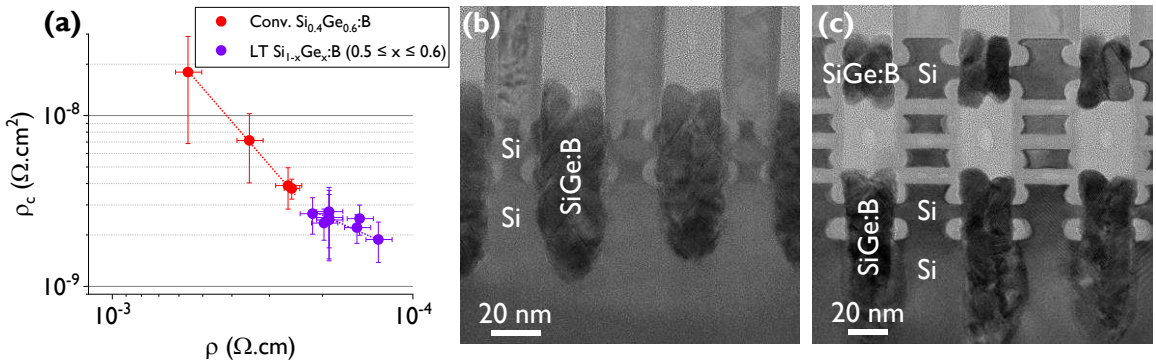

Figure 3. (a) Contact resistivities obtained on CTLM structures comparing conventional SiGe:B processes with LT-SiGe:B processes ([Ge] ~ 50-62%) which have $[B]_{act}$ up to ~ $2.5\times10^{21}cm^{-3}$ (17,18). (b) X-TEMs of LT-SiGe:B SD growth (19) for (b) 48 nm CPP nanosheet stack with 1 Si sheet and (c) 60 nm CPP 1×1 CFET stack.

N-type S/D epitaxy

Figure 4 summarizes some results for n-type S/D epitaxy. Fig. 4(a) shows the specific contact resistivities obtained for Ti/Si:P contacts as a function of the active P-concentration ($[P]_{act}$) determined from micro-Hall measurements (17,18). For the HT-Si:P process shown by the red squares, the doping activation after epitaxy is relatively poor (10%-15%) and post epitaxy spike anneals (T_p~ 950ºC-1000ºC) are needed to increase the active concentration and decrease the contact resistivity (11). The spike anneal globally improves the access resistance and diffuses some of the dopants towards the Si nanosheets. When moving to LT-Si:P processes with temperatures below 500ºC (indicated by the filled green triangles) (20-22), $[P]_{act}$ can be increased up to ~ 1×10^{21} cm^{-3} and the contact resistivity reduces to ~ 2×10^{-9} $\Omega.cm^2$. The advantage is clearly the higher activation levels which are achieved compared to HT-Si:P without the need for an additional activation anneal, making the thermal budget compatible with MD-first integration.

Fig. 4(b) shows a typical X-TEM example of the integration of HT-Si:P S/D in a 60 nm CPP 1×1 CFET structure. The bottom (co-flow) SiGe:B S/D is protected with a thin isolation oxide layer leading to a selective HT-Si:P growth. The growth occurs from opposing Si sheets and leads to an enhanced defectivity at places where the epi is merging and where the epi is laterally growing over the inner spacers. A higher defectivity is observed compared to bulk FinFETs, and more attention is required for the removal of dielectrics and cleaning of the nanosheet Si surfaces before Si:P growth. Still, even with the above limitations, a first successful demonstration of individually frontside contacted mCFET CMOS devices has been reported recently (5).

Fig. 4(c-d) shows typical X-TEM images and illustrate the successful integration of a CDE based LT-Si:P layer in a CFET device fabrication scheme. For this layer, the growth and etching were done at 525ºC and the resistivity was estimated at ρ ~ 0.3 mΩ.cm, corresponding to half the value obtained for HT-Si:P (ρ ~ 0.62 mΩ.cm). The growth was nicely selective and the structural properties were comparable to the HT-Si:P case. For this process we still rely on classical HCl/GeH_4 based etching (23-25). One attention point is however the considerable etch rates for both α-Si (i.e. used in the dummy gates), as well

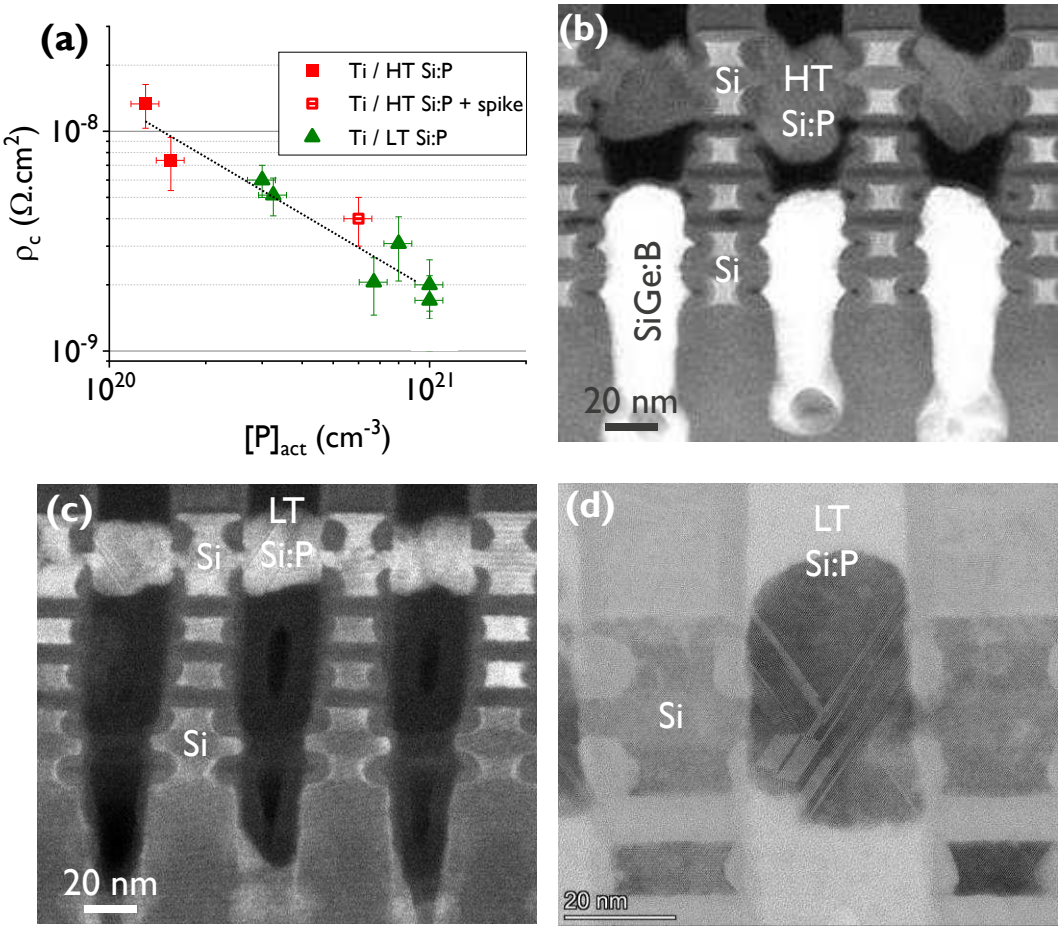

Figure 4. (a) specific contact resistivities obtained for Ti/Si:P contacts as a function of the active P-concentration ([P]$_{act}$) determined from micro-Hall measurements (17,18). (b-d) X-TEMs of Si:P growth in 60 nm CPP 1×1 CFET structures, (b) HT-Si:P, and (c-d) LT-Si:P (T_g = 525ºC).

and SiGe (i.e. used in the NS stack and B-S/D). If these materials are not well encapsulated by the surrounding dielectrics, they risk being etched during the etch cycles of the CDE process. In Fig. 4(c) we can for instance observe an attack of the underlying B-S/D indicating that the used ISO layer was too thin to prevent SiGe:B etching.

Conclusions

This work reports the progress in source/drain (S/D) epitaxy development for nanosheet-based monolithic complementary field effect transistors (mCFET). The S/D processes for bulk finFET devices have been successfully transferred to mCFET devices. Compared to bulk finFET S/Ds, a higher defectivity is observed arising from the merging of individual epitaxial growth fronts and the lateral growth over the surrounding dielectrics. Low-temperature epi processes were integrated successfully for the bottom and top S/D to further reduce the transistor access resistance components and comply with thermal budget limitations.

Acknowledgments

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