

Epitaxial Si/SiGe Multi-Stacks: From Stacked Nano-Sheet to Fork-Sheet and CFET Devices

R. Loo^{a,b}, A. Akula^a, Y. Shimura^a, C. Porret^a, E. Rosseel^a, T. Dursap^a, A. Y. Hikavy^{a,*},
M. Beggiato^a, J. Bogdanowicz^a, A. Merkulov^a, M. Ayyad^a, H. Han^a, O. Richard^a,
A. Impagnatiello^a, D. Wang^c, K. Yamamoto^c, T. Sipőcz^d, Á. Kerekes^d, H. Mertens^a,
N. Horiguchi^a, and R. Langer^a

^a Imec, Kapeldreef 75, 3001 Leuven, Belgium

^b Ghent University, Department of Solid-State Sciences, Krijgslaan 281, building S1,
9000 Ghent, Belgium

^c Faculty of Engineering Sciences, Kyushu University, 6-1 Kasuga-koen, Kasuga,
Fukuoka, Japan

^d Semilab Semiconductor Physics Laboratory Co. Ltd., Prielle Kornélia u. 2. H-1117
Budapest, Hungary

* Currently at Soitec, 922 Parc technologique des Fontaines, Chem. des Franques, 38190
Bernin, France

After a short description of the evolution of metal-oxide-semiconductor (MOS) device architectures and the corresponding requirements on epitaxial growth processes, the manuscript describes the material properties of complicated Si/SiGe multi-layer stacks used for complementary field effect transistor (CFET) devices. They contain two different Ge concentrations and have been grown using conventional process gases. A relatively high growth temperature is used to obtain acceptable Si and SiGe growth rates. Still island growth has been suppressed for Ge concentrations up to 40%. Excellent structural and optical material properties of the Si/SiGe multi-layer stack will be reported, with up to 3 + 3 Si channels in the top and bottom part of the stack, respectively. The absence/presence of lattice defects has been verified by room temperature photoluminescence measurements. Photoluminescence measurements at low temperatures are used to study band-to-band luminescence from individual sub-layers and to illustrate the optical material quality of the CFET stack.

Introduction

The scaling evolution from stacked nano-sheet devices to fork-sheet devices and complementary field effect transistor (CFET) architectures went together with increased complexities of the epitaxial growth schemes (Fig. 1). This is valid for both the Si/SiGe multi-layers, which define the thickness of the nano-sheet channels as well as the vertical distance between individual nano-sheets, and for the epitaxially grown source/drain (SD) layers which require a continuous increase in active doping concentration and a reduction in thermal budget without compromising material quality.

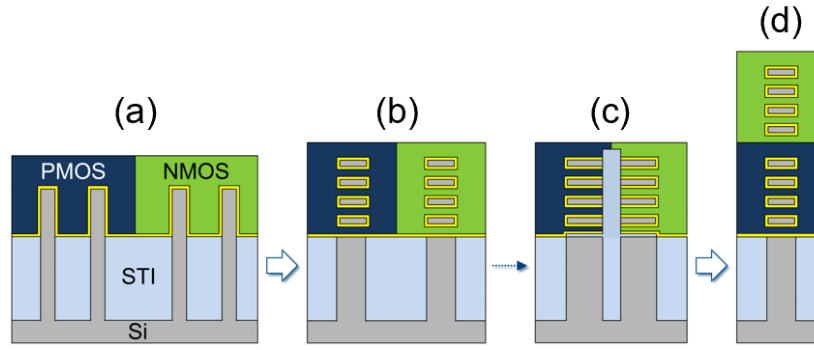


Figure 1. Evolution of MOS device architecture. a) Triple-gate finFETs are being replaced by b) gate-all-around (GAA) vertically stacked lateral nano-sheet FETs, which could potentially evolve into c) the so-called fork-sheet configuration wherein neighboring devices are separated by a dielectric wall. Beyond that, d) stacking of N/PMOS devices on top of each other in a CFET structure is currently being explored as an attractive concept for ultimate CMOS scaling.

Fork-sheet transistors are lateral nano-sheet devices with a forked gate structure (Fig. 1c) (1,2). The physical separation of n- and p-devices by a dielectric wall enables device scaling and, consequently, sheet width maximization within the limited footprint of low-track-height standard cells. Bottom dielectric isolation has been proposed to circumvent the junction isolation trade-off between punch-through suppression on the one hand and junction leakage and capacitance on the other hand (3). A typical fabrication scheme includes the challenging epitaxial growth of fully strained Si/Si_{1-y}Ge_y/multi-{Si_{1-x}Ge_x/Si} epi stacks (y>x) where the bottom Ge-rich Si_{1-y}Ge_y layer is later replaced by a SiN/SiCO isolation (4,5).

In the CFET architecture, N- and P-MOS devices are placed on top of each other, thus completely removing the area consumption by the N-P spacing. This allows for further maximizing the effective channel width and, hence, the drive current (6-12). The architecture can be fabricated following either a monolithic or a sequential approach. In the first option, N- and P-MOS transistors are built on the same wafer, while the sequential fabrication flow is based on wafer-to-wafer bonding techniques. The strengths and challenges of both approaches are discussed in (9). In the monolithic approach, device fabrication starts with the epitaxial growth of an even more complicated Si/SiGe multi-stack with two different Ge concentrations (Fig. 2) (9,12,13), and where Ge-rich Si_{1-y}Ge_y layers are later replaced by isolating dielectrics forming a so-called middle dielectric isolation (MDI) (9,12). Owing to the very small dimensions (e.g., sub-10 nm nano-sheet channel width), high etching selectivity of the Si_{1-y}Ge_y layers towards both Si_{1-x}Ge_x and Si, and excellent process controls are mandatory. This sets stringent requirements on the epitaxial layer stacks (thicknesses and composition control, sharpness of interfaces, and absence of strain relaxation) (4,5,13,14) as well as on the Si_{1-y}Ge_y etch process (high selectivity and limited consumption of Si_{1-x}Ge_x and Si) (14-17).

High performance metal / SD junctions are key to alleviate scaling-related contact issues in these devices (18). Selective epitaxial growth (SEG) processes yielding heavy active doping are therefore required, in addition to introducing innovative contact materials

and designs (19-21). The resulting electrical performance is, however, restricted by doping solubility limits and loading effects (impact of substrate patterning) inherent to scaling. Those must be circumvented to enable the upcoming generations of components. Moreover, novel device architectures add stringent constraints regarding pre-epi cleaning strategies, thermal budgets, and stability. Changes in how devices are connected are also being introduced into the roadmap. To address both wiring and power delivery bottlenecks, part of the interconnects are being moved to the wafer backside (21). This backside processing starts with an extreme wafer thinning, for which a thin SiGe etch stop layer is being considered to compensate for within-wafer non-uniformities of the Si substrate removal process (22-24).

The current work describes the material requirements for the different layers used in monolithic CFET device flows and the progress made on the associated epitaxial growth. The epitaxial growth processes used to deposit Si/Si_{1-x}Ge_x multi-layers for GAA devices (Fig. 1b) is well understood and has been reported in (25,26). Previous learnings from imec about the selective epitaxial growth of extremely highly doped SD layers as well as the growth against the vertical sidewalls of the nanosheets have been reported in e.g. (19,20,27,28). More recent results will be discussed in (29,30).

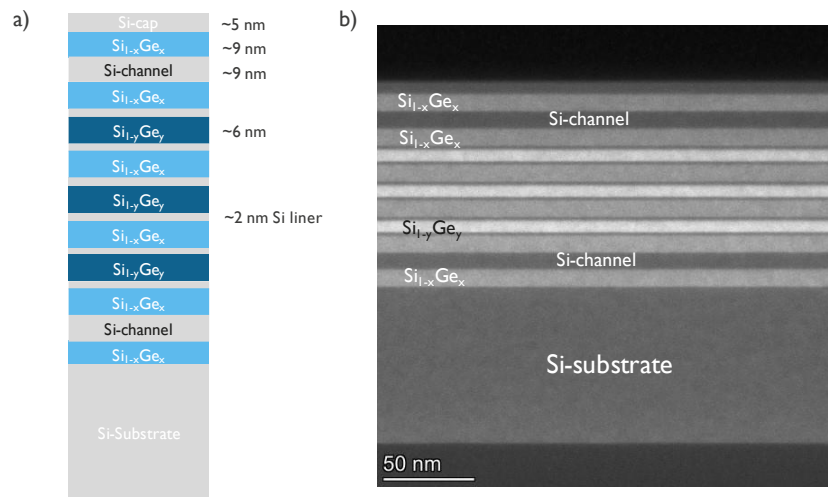


Figure 2. a) Schematic cross-section and b) cross sectional HAADF STEM image of a Si/SiGe multi-stack used for CFET devices with one channel for both the p-type and the n-type devices.

Experimental

The epitaxial layers were grown in a production compatible ASM Intrepid™ RP-CVD cluster tool. Before layer deposition, the 300 mm Si(001) wafer surface received a conventional wet-chemical clean. Depending on the incoming wafer, the native oxide was either removed in-situ by a thermal treatment at a sufficiently high temperature (> 1000°C) or by a wet HF clean followed by an in-situ anneal at 800 – 900°C. Careful optimization of the temperature profile within the epi-reactor allows to avoid the formation of slip lines during the pre-epi bake and to deposit epitaxial layers with a uniform thickness over the wafer (relative standard deviation < 1.3%). Epitaxial growth was carried out at reduced

pressure using H_2 as carrier gas and conventional precursor gases (SiH_4 , SiH_2Cl_2 , and GeH_4 (5% diluted in H_2)). The epitaxial layer stack consists of a complicated Si/SiGe multi-stack with two different Ge concentrations (Fig. 2). The $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers with $y > x$ are separated by thin Si layers. After fin patterning, the $Si_{1-y}Ge_y$ layers are replaced by SiN/SiCO (9,12). The presence of the Si liners prevents vertical etching of $Si_{1-x}Ge_x$ during $Si_{1-y}Ge_y$ removal (14). The abruptness of the compositional change at Si/SiGe interfaces is limited by Ge segregation occurring during Si layer growth on the SiGe surface. The most abrupt interfaces have been obtained when using a chlorinated chemistry (31,32).

A broad range of material characterization techniques have been used to study the epitaxial material properties. For a review of the metrology challenges encountered for GAA structures (including CFET) the reader is referred to the references (33) and (34). The interface abruptness between two sublayers of the epi-stack has been characterized by e.g. high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) (35) and soft X-ray reflectometry (36). Room temperature photoluminescence (PL) measurements have been performed using a production compatible En-Vision-3000 system from Semilab (37,38). This inspection system allows for automatic 200/300 mm wafer tests and targets quick, non-contact and non-destructive detection of nm scale PL active buried defects. The Micro-PL measurement, for characterizing optical properties of materials on a micron scale, is based on a high intensity illumination at 532 nm. The detection is carried out at either band-to-band PL, with a peak intensity at 1100 nm (1.127 eV), or at 1400 nm long pass filter PL, 1400-1600 nm (0.89-0.78 eV). Macro-PL applies 808 nm illumination for full wafer mapping. Temperature- (9-300 K) and power-dependent PL measurements, were used to study band-to-band luminescence. A continuous wave laser beam with an excitation wavelength of 532 nm and a spot diameter of $\sim 2 \mu m$ creates excitons. Because of the valence band offsets, most excitons are trapped by the SiGe layers and the luminescence from the different layers is collected by a 50x object lens, dispersed by a Horiba LabRAMHR-PL system, and detected by an extended InGaAs array sensor cooled at 180 K.

Results and Discussion

Structural material properties of the CFET stack

The epitaxial growth temperature has been chosen to be low enough to obtain two dimensional $Si_{1-y}Ge_y$ growth, without three dimensional islands, for single layers as well as for the complete CFET stack with Ge concentrations up to 40% (Fig. 2b). The smooth surface of the resulting CFET stacks is confirmed by both Scanning Electron Microscope (SEM) and surface haze measurements. No larger defects are observed across the wafer surface. Except for the area near the wafer edge, misfit dislocations are avoided by choosing suitable process conditions and taking limitations in layer compositions and individual thicknesses into account. The crystalline defect density, as measured for the layers shown in Fig. 2b, lies indeed below the detection limit of Electron Channeling Contrast Imaging (ECCI), which was in the given case $\sim 1 \times 10^5$ defects/cm². Near the wafer edge, misfit dislocations are nevertheless present, because the wafer edge reduces the critical thickness for layer relaxation (26). The absence of defects in the inner part of the wafer surface and the presence of misfits near the wafer edge is confirmed by room tempe-

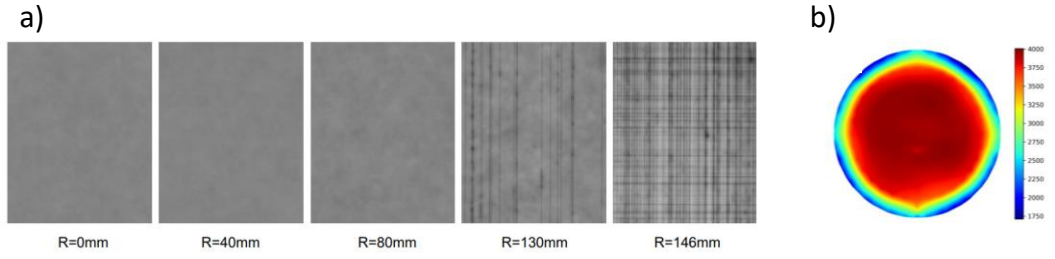


Figure 3. a) 1400 nm long pass filter PL measured on an epitaxial CFET stack from center to edge over the wafer. The field of view is $140 \times 175 \mu\text{m}^2$ and R is the radial distance from the wafer center. b) PL intensity map.

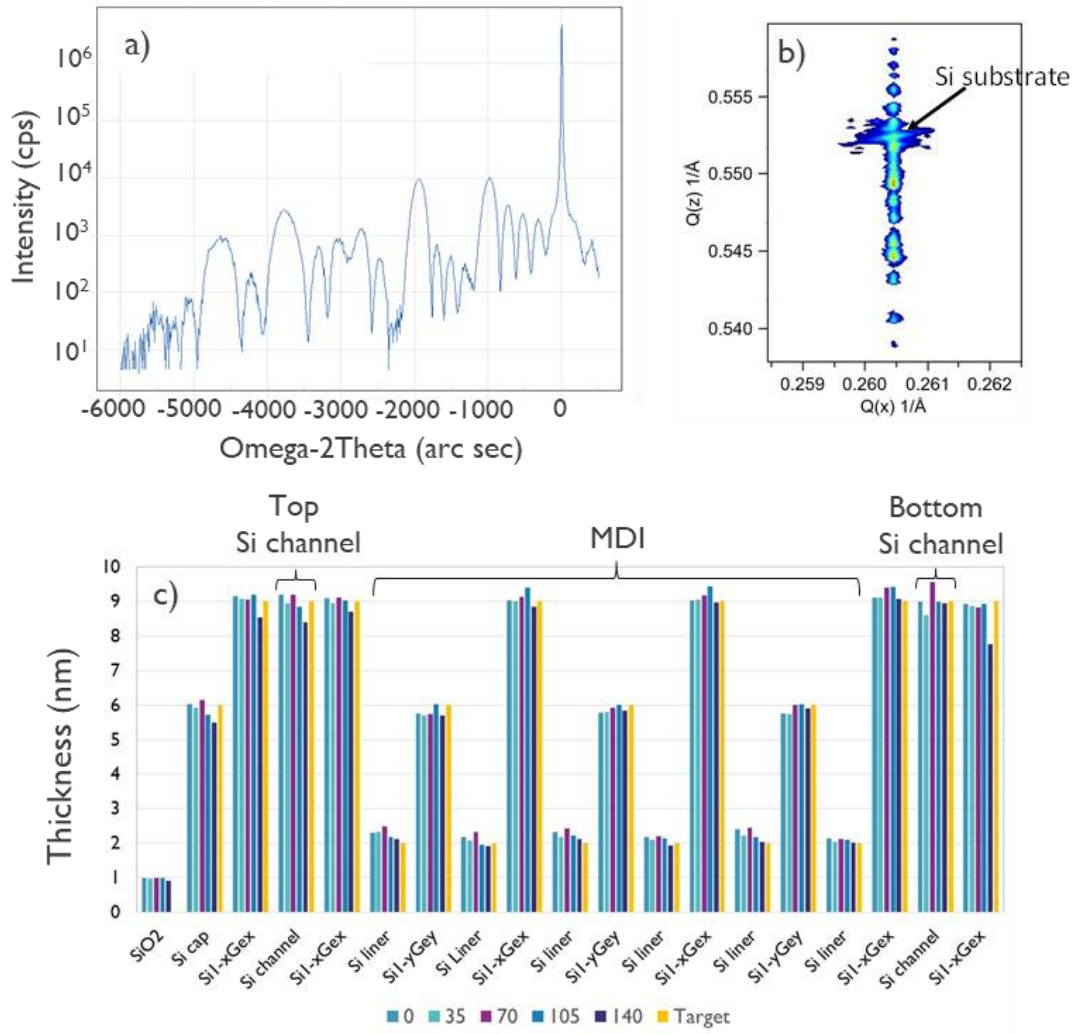


Figure 4. a) XRD ω - 2θ scan acquired around the Si 004 Bragg reflection for the CFET stack shown in Fig. 2b, grown on top of a Si:P ground plane doped layer, b) XRD RSM acquired for the same stack around the Si 113 Bragg reflection, and c) thicknesses of the individual layers as extracted from XRR and for different positions over the wafer, where the distance from the wafer center is given in mm.

perature PL measurements and reflected in the full wafer color map of the Macro-PL intensity (Fig. 3). A reduction of the growth temperature, together with the use of higher order precursors (14,25) might enable to suppress the formation of misfit dislocations at the wafer edge. However, avoiding reactions in the gas phase needs careful attention as it results in the formation of amorphous defects on the wafer surface which, in turn, also can act as nucleation sources for misfit dislocations, despite the lower processing temperature (39). Similar layers stacks but without the presence of misfit dislocations at the wafer edge will be reported by Rengo *et al* (40).

The material quality is further confirmed by X-Ray Diffraction (XRD) (Fig. 4a), X-Ray Reflectivity (XRR), and XRD Reciprocal Space Maps (RSM) (Fig. 4b). The latter confirms the absence of strain relaxation. The peaks constituting the omega-2theta (ω -2 θ) diffraction spectrum reflect the high material quality. The individual peaks are well resolved, and the spectrum has a low background signal. Fig. 4c shows an example of the within wafer uniformity of individual layer thicknesses as obtained after optimization of the process settings.

The Ge concentrations in the $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{Ge}_y$ layers might be adapted in function of the characteristics of the selective etching routines. Keeping the individual layer thicknesses unchanged, critical Ge concentrations exist, above which layer relaxation of the Si/SiGe multi-stack cannot be avoided. As an example, Fig. 5 compares the XRD ω -2 θ scans and plan-view (PV) SEM images of multi-stacks where the $\text{Si}_{1-x}\text{Ge}_x$ layers contain either 18% Ge (top) or 24% Ge (bottom) while the $\text{Si}_{1-y}\text{Ge}_y$ layers have in both cases the same nominal Ge concentration of 38%. The stack with the lower Ge concentration is fully strained and the XRD spectrum is well defined with well resolved peaks and a low background signal. The PV-SEM images show a smooth surface without suggesting the presence of misfit dislocations at the underlying Si/ $\text{Si}_{1-x}\text{Ge}_x$ and/or Si/ $\text{Si}_{1-y}\text{Ge}_y$ interfaces. For the stack with the higher Ge concentration, misfit dislocations are detected at different positions of the wafer surface. The corresponding XRD spectrum is less well defined with a higher background and the peaks are less well resolved.

Also, the presence of a Si:P ground plane doped layer, eventually considered for bottom isolation, increases the risk for a degraded material quality, especially when the Si:P ground plane doped layer is formed by ion implantation. In addition, there is a risk for P segregation into the Si/SiGe multi-stack, which also affects final device properties. Both issues can be avoided by using an optimized combination of ex-situ wet-chemical and in-situ thermal pre-epi cleaning routines, as confirmed by Extremely Low Impact Energy Secondary Ion Mass Spectrometry (EXLIE-SIMS) (41) shown in Fig. 6.

The optimized epitaxial growth of the Si/ $\text{Si}_{1-x}\text{Ge}_x$ / $\text{Si}_{1-y}\text{Ge}_y$ multi-stack can be extended to multiple channels (Fig. 7). Again, no larger defects are observed across the wafer surface and the epitaxial layer remains free of misfit dislocations, except for the area near the wafer edge. The XRD signature is close to the predicted spectrum. The different peaks are well resolved, and the low background illustrates the high material quality. The differences between the spectrum shown in Fig. 7b with respect to the one shown in Fig. 4a, are the result of the additional layers in the stack.

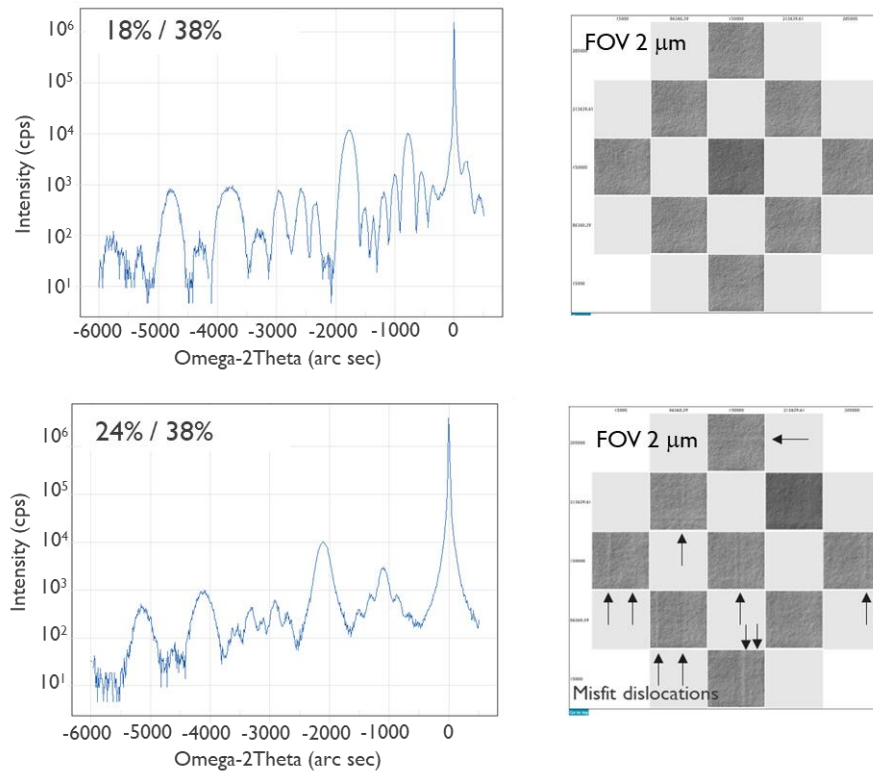


Figure 5. Left: XRD ω -2 θ scans acquired around the Si 004 Bragg reflection for CFET stacks with different Ge concentrations in the $\text{Si}_{1-x}\text{Ge}_x$ layers and grown on top of Si:P ground plane doped layers. Right: plan view SEM inspections taken on multiple locations of the wafer surface. $\text{Si}_{1-x}\text{Ge}_x$ layers contain 18% Ge (top) and 24% Ge (bottom). In both cases the $\text{Si}_{1-y}\text{Ge}_y$ layers contain 38% Ge.

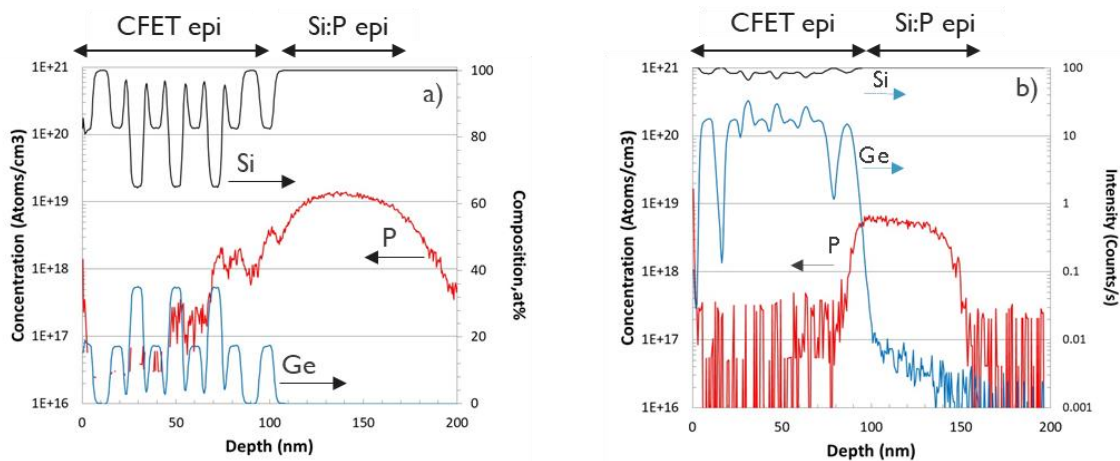


Figure 6. P, Si, and Ge profiles as measured by EXLIE-SIMS for epitaxial CFET stacks grown on Si:P. a) Non-optimized pre-epi treatment before growing the CFET stack and b) optimized pre-epi treatment for which the P segregation from the bottom Si:P layer into the CFET multi-stack is clearly suppressed. In b), the measurement conditions were optimal for P, but not for Si and Ge.

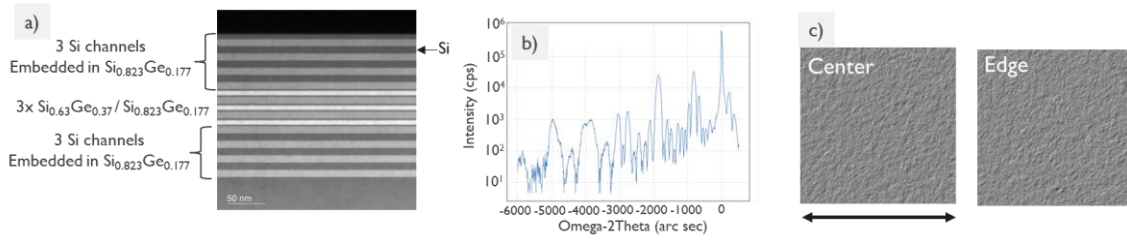


Figure 7. Si/SiGe multi-stack for CFET devices containing 3 + 3 channels in both the top and the bottom part. a) Cross-sectional HAADF STEM, b) XRD ω -2 θ scans acquired around the Si 004 Bragg reflection, and c) plan view SEM inspections taken at the center and edge of the wafer.

Interface sharpness

The presence of thin Si liners in between the $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{Ge}_y$ layers aims to prevent vertical etching of $\text{Si}_{1-x}\text{Ge}_x$ during the lateral $\text{Si}_{1-y}\text{Ge}_y$ removal (14). Still, the required high etching selectivity of the $\text{Si}_{1-y}\text{Ge}_y$ layers towards both $\text{Si}_{1-x}\text{Ge}_x$ and Si, and also of $\text{Si}_{1-x}\text{Ge}_x$ towards Si later in the processing flow, sets requirements on the sharpness of the interfaces between different layers. EXLIE-SIMS (41), Energy-Dispersive X-ray spectroscopy (EDX), integrated STEM contrast analysis (35), and soft X-ray reflectometry (36) confirm the sharp gradients in Ge concentration at the different interfaces. A typical example of Ge and Si profiles as measured by EXLIE-SIMS is shown in Fig. 8a, which also confirms the layer-to-layer reproducibility in composition. All interfaces are extremely sharp. The depth resolution of the EXLIE-SIMS is therefore not sufficient to extract interface steepness.

The interface abruptness has nevertheless been extracted from horizontally integrated HAADF-STEM contrast images (Fig. 8b). The HAADF-STEM contrast is approximately proportional to the square of the atomic number, which allows to extract the Ge depth profiles (Fig. 8c). integrated contrast has been fitted with the Sigmoid function which is expressed as:

$$f(x) = \frac{C}{1 + e^{\frac{\pm(z_0 - x)}{\tau}}} + b \quad [1]$$

where C and b are constants and z_0 denotes the position of the interface. The value of 4τ is used as the interface thickness (42). Note that the integrated contrast profiles shown in Fig. 8c have been obtained by integrating over an area of the TEM specimen. The extracted 4τ values include contributions from interfacial roughness and are therefore larger than the values obtained when extracting the contrast profile from a vertical line scan.

The interfaces from the Si-channel (bottom side) towards $\text{Si}_{1-x}\text{Ge}_x$ (top side) are, as expected, slightly sharper than the interfaces from $\text{Si}_{1-x}\text{Ge}_x$ (bottom side) towards the Si-channel (top side) (Fig. 8c, top and bottom figures). For the latter one, the abruptness of the compositional change is limited by Ge segregation, occurring during Si layer growth on the $\text{Si}_{1-x}\text{Ge}_x$ surface. The Si-liners placed in-between $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{Ge}_y$ layers, are too thin to enable extraction of interfacial thicknesses between the $\text{Si}_{1-y}\text{Ge}_y$ and Si layers, as Si-top and bottom interfaces are overlapping (Fig. 8c, middle part). The presence of the

Si-liners does allow a successful selective $\text{Si}_{1-y}\text{Ge}_y$ removal without damaging $\text{Si}_{1-x}\text{Ge}_x$ as reported in (9) and (12), which illustrates the interfacial sharpness in a different way.

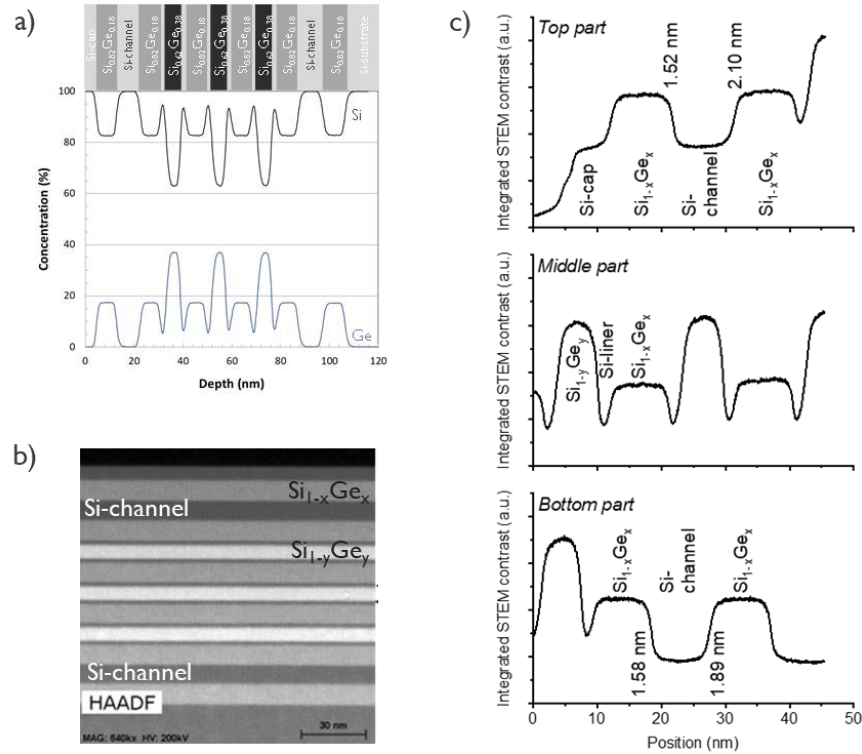


Figure 8. Si/SiGe multi-stack as used for CFET devices with one channel for both the p-type and the n-type devices. a) Ge and Si EXLIE-SIMS profiles, b) cross-sectional HAADF STEM, and c) horizontally integrated contrast profiles extracted from high resolution HAADF STEM images. The numbers mentioned at the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ and $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ interfaces are the interface thicknesses obtained after fitting the contrast profiles with the Sigmoid function.

Low temperature photoluminescence

The low temperature PL spectra contain four well defined luminescence peaks (Fig. 9a). By temperature- and excitation-power-dependent measurements, combined with a comparison with the PL spectra obtained on reference samples which contain only one group of SiGe layers (either the low-Ge $\text{Si}_{1-x}\text{Ge}_x$ or the Ge-rich $\text{Si}_{1-y}\text{Ge}_y$), the peaks could be assigned to the no-phonon (NP) transitions and their TO-phonon replicas arising from the $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{Ge}_y$ layers with the two different Ge concentrations (43,44). The largest fraction of the laser light is absorbed in the Si substrate where consequently the majority of the excitons are created. At the lowest measurement temperature, these excitons are trapped by the SiGe layer which is next to the substrate. This explains the higher intensity of the low-Ge $\text{Si}_{1-x}\text{Ge}_x$ luminescence. With increasing laser intensity, the NP peaks shift to a higher energy as the luminescence changes from localized excitons (LE's) to bound excitons (BE's), and free excitons (FE's) (not shown). Increasing the measurement temperature results in a thermal quenching of the low-Ge $\text{Si}_{1-x}\text{Ge}_x$ luminescence and a negative thermal quenching of the Ge-rich $\text{Si}_{1-y}\text{Ge}_y$ luminescence (Fig. 9b). Excitons can

leave the low-Ge $\text{Si}_{1-x}\text{Ge}_x$ layer(s) and are trapped by the Ge-rich $\text{Si}_{1-y}\text{Ge}_y$ layers which have a larger valence band offset, with respect to Si. The fact that excitons can escape from low-Ge $\text{Si}_{1-x}\text{Ge}_x$ layer(s) and move to Ge-rich $\text{Si}_{1-y}\text{Ge}_y$ layers without being trapped by non-radiation recombination centers illustrates the high material quality of the epitaxial stack and the absence of defects. Above ~ 120 K, there is no luminescence signal at energies above 0.9 eV (no luminescence arising from the low-Ge $\text{Si}_{1-x}\text{Ge}_x$ layers) and the PL intensity at 0.8 – 0.9 eV shows normal thermal quenching.

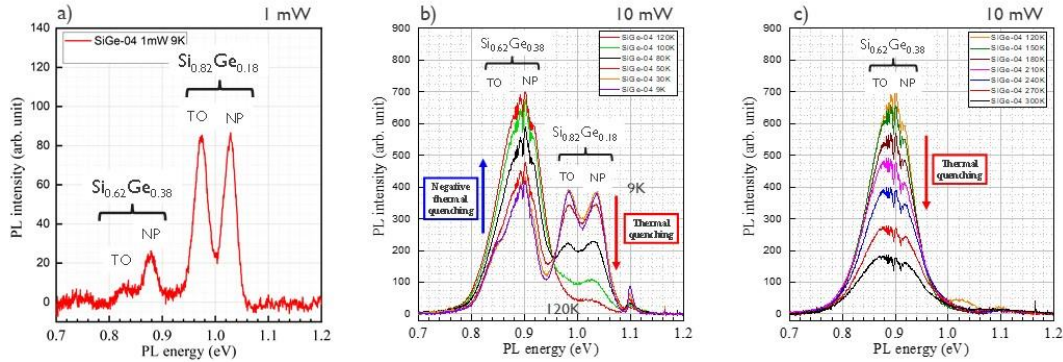


Figure 9. PL intensity as function of PL energy as measured on a complete CFET stack. a) Spectrum measured at 9 K and an excitation power intensity of 1 mW. b) and c) Temperature dependent PL spectra measured at an excitation power intensity of 10 mW and in temperature regimes of 9 – 120 K and 120 – 300 K, respectively.

Conclusions

The material properties of Si/SiGe multi-layer stacks used for CFET devices have been presented. The epitaxial layers contain two different Ge concentrations and have been grown using conventional process gases. Despite the relative high growth temperature, island growth can be suppressed for Ge concentrations up to 40%. Excellent material properties have been reported. A carefully optimized pre-epi surface preparation routine prevents both degradation of the material quality as well as phosphorus segregation when depositing the CFET stack on top of a Si:P ground plane doped layer. The optimized epitaxial growth process allows the deposition of the Si/SiGe CFET stack with multiple channels as demonstrated for 3 + 3 channels at the top and bottom part of the layer stack. Room temperature PL measurements allow for a fast and reliable verification of the absence/presence of lattice defects including full wafer mapping. Complementary low temperature PL measurements have been used to study the optical material properties of individual sublayers and to further demonstrate the material quality of the CFET stack.

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