Monolithic 650 V dual-gate p-GaN bidirectional switch

G. Baratella, U. Chatterjee, O. Syshchyk, M. Borga, E. Fabris, T. Cosnier, B. Bakeroot, S. Decoutere

***Abstract*—This paper is about the study and characterization of a monolithically integrated dual-gate bidirectional switch realized in a CMOS-compatible GaN pilot line. The switch is based on a p-GaN gate enhancement-mode (E-mode) high-electron-mobility transistor (HEMT) rated for 650 V, and provides a symmetrical electrical operation in positive and negative bias conditions while achieving comparable performance to the traditional HEMT and, with respect of the implementation of conventional bidirectional switches, the overall ON-resistance is sensibly lower.**

Several layout variations are discussed both through the electrical measurements and Technology CAD (TCAD) simulations, together with comparisons with the reference HEMT, providing valuable insights into the design optimization of dual-gate bidirectional switches.

***Index Terms*—Bidirectional switch, gallium nitride (GaN), high electron mobility transistor (HEMT)**

I. Introduction

WIDE bandgap semiconductors, such as gallium nitride (GaN), have emerged as promising candidates for power electronics applications, due to their superior properties compared to conventional silicon [1], [2], [3]. Among the various GaN-based device structures, enhancement-mode p-GaN gate high-electron-mobility transistors (E-mode p-GaN gate HEMTs) offer several advantages, such as normally-off operation, low gate leakage, and high switching speed [4].

Bidirectional switches (BDS), which allow to conduct current and block voltage in both polarities [5], [6], [7], [8], [9], [10], [11], [12], depending on the control signals applied to the gates as shown in Fig. 1, can be monolithically integrated using the E-mode p-GaN HEMT technology. They are the main component of a matrix converter, which is an efficient AC/AC converter that doesn't require a DC link, but they are also widely used in others power converters, motor drives, and battery management systems (BMS) [13], [14], [15], [16] and, in comparison with the traditional implementation of a BDS - realized by connecting two discrete unidirectional MOSFETs or IGBTs in anti-parallel or anti-series configuration - a monolithic dual-gate GaN BDS can be a valuable alternative due to its lower conduction losses, higher switching speed operation and reduced component count, which in turn helps to build a compact efficient system [17]. Furthermore, the possibility to fabricate this BDS in a GaN-IC process would allow the integration of multiple bidirectional switches and their driving circuits on the same die, yielding the development of fully integrated power converters and BMS. This would reduce the parasitics and the overall footprint, while increasing efficiency even further.

In this work, we present a dual-gate bidirectional switch design in a 650 V GaN technology, based on an E-mode p-GaN gate HEMT and realized with several layout variations, shown in Table 1. A Scanning electron microscopy (SEM) picture of the cross-section of device A is shown in Fig. 2, with a zoom-in SEM picture of the left p-GaN gate. We characterize such devices on-wafer and demonstrate their bidirectional operation under different gate bias conditions. TCAD simulations of the process flow and the physical behavior are also performed, and the results are correlated to real device measurements, to gain insights into the operation of the switches, and to provide guidelines for future device optimization.

In section II, the device structure and the process flow that has been used to fabricate the device are presented. The measurements set-ups for the bidirectional switches are described and compared to the standard characterization setups for the traditional HEMTs. Lastly, the Sentaurus [18] TCAD model is presented.

In section III, the results of the electrical characterization of the bidirectional switches are presented. First, the DC characterization in ON-state, with the I_{S2}-V_{S2S1} and I_{S2}-V_{G1S1} measurements, corresponding of the I_D-V_{DS} and I_D-V_{GS} measurements for the HEMTs, are shown. Afterwards, the OFF-state characteristics show the source 2 leakage until the breakdown of the device. Differently from HEMTs, where the breakdown is measured for positive V_{DS}, for the BDSs it is measured in both positive and negative biases, as the device must work in both directions. To conclude, the results in OFF-state are compared among the different layout variations, and TCAD simulations are used to gain insight into the breakdown mechanism.

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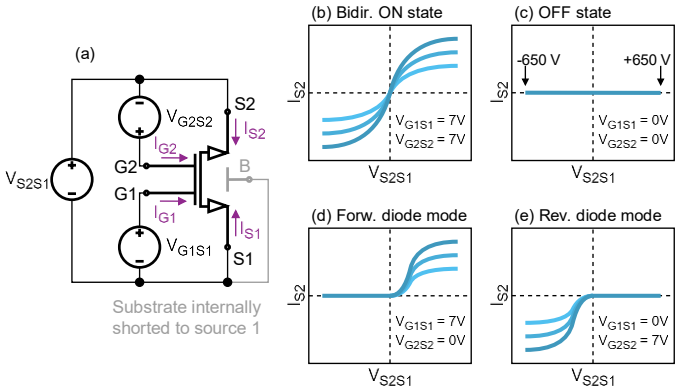

Fig. 1. (a) Bias scheme of a bidirectional switch and typical curves: (b) bidirectional ON state with both gates ON, (c) bidirectional OFF state with both gates OFF, (d) forward and (e) reverse diode mode with only one gate ON, respectively.

TABLE 1
BIDIRECTIONAL SWITCH DESIGN VARIATIONS

Device	L_G (µm)	L_{SG} (µm)	L_{GG} (µm)	L_{FP} (µm)
A	1.3	0.5	10	0.75/1/1/0
B	1.5	0.75	16	1.5/1.5/3/0
C	1.5	0.75	16	2/2/2/0
D	1.5	0.75	22	3/3/3/0
E	1.5	0.75	22	2/2/2/2

The LFP are referred to the gate field-plates in the following order: Metal0/Ohmic-Metal/Metal1/Metal2.

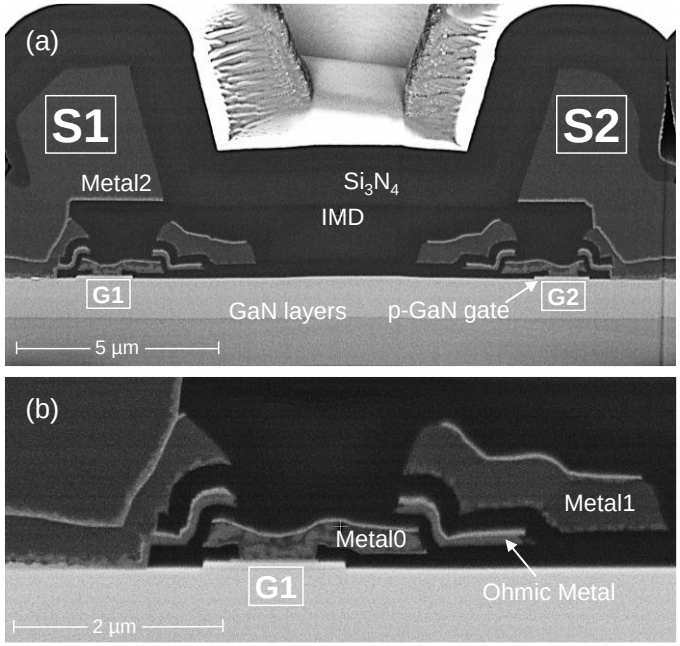

Fig. 2. (a) The SEM cross-section of device A and (b) a zoom on the gate 1.

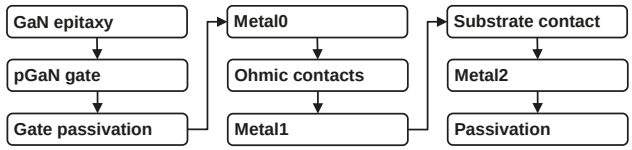

Fig. 3. Overview of the GaN process-flow.

II. DEVICE STRUCTURE AND TEST METHODOLOGY

The devices are made in imec's 650 V GaN technology, where the epitaxial layer is grown by metalorganic chemical vapor deposition (MOCVD) on a 200 mm SOI substrate with a Si(111) layer over a buried oxide layer [19], [20]. Patterning of the p-GaN stack is done to form the gates of the p-GaN bidirectional switch, after which a Metal0 is deposited on top of the p-GaN layers to allow low gate resistance and formation of the gate field-plate (FP). Afterwards, the openings in the SiO_2 layer, deposition and patterning of the ohmic-metal are performed to create the ohmic contacts for the sources and the first source-connected field-plates. Following, two interconnects levels are formed in Metal1 and Metal2, separated by SiO_2 layers, forming two source-connected field-plates. Finally, a Si_3N_4 passivation is deposited. An overview of the process flow is shown in Fig. 3.

The devices have two source contacts and two gate contacts, which must be polarized with a differential bias referenced to the corresponding source, and four field-plates that are inherited from the reference p-GaN HEMT. The field-plates are extended on both sides of the devices equally, and the source field-plates are connected to the corresponding source contacts in the third dimension, outside of the active area, to reduce the overlap between sources and gates and therefore the gate-to-source capacitance C_{GS}. The devices are fabricated with three variations in the gate-to-gate distance L_{GG} and five in the field-plate dimensions. Terminal source 1 is shorted to the substrate through the substrate contact. This design decision was made to cope with the characterization method of these prototypes, limiting the measurements to four terminals.

All devices are realized with ten fingers of 350 µm width, for a total gate width of 3.5 mm.

A. Characterization set-ups

The electrical characterization is performed on-wafer, using a Keysight B1505A Power Device Analyzer with one High-Voltage Source-Measuring Unit (HVSMU), one High-Current SMU (HCSMU) and two High-Power SMUs (HPSMUs).

Source 1 is connected to the Ground Unit (GNDU) of the B1505A, source 2 can be connected to either the HVSMU or the HCSMU by means of a Keysight N1258A Module Selector, whereas the two gates are connected to the two HPSMUs. The set-up is shown in Fig. 4(a).

The terminal gate 1 requires a voltage V_{G1S1} referred to source 1, whereas gate 2 requires a voltage V_{G2S2} referred to source 2. Gate 1 can be directly biased to the V_{G1S1} voltage required to turn it on, because the terminal source 1 is maintained at 0 V by the GNDU, similar as in a traditional HEMT. On the contrary, gate 2 requires a voltage V_{G2S2} referred to source 2 to form the 2DEG channel and, when source 2 is swept, also gate 2 must be swept synchronized with source 2 in order to maintain the correct V_{G2S2} potential that keeps gate 2 in ON (or OFF) state. The curves used to perform the I_{S2}-V_{S2S1} measurement, which is the equivalent of the I_D-V_{DS} for a traditional HEMT, are shown in Fig. 4(b).

To measure the threshold voltage of the device, the same set-up is used, with the curves shown in Fig. 4(c). Gate 1 is swept from -2 V to 7 V, while the other gate is at 7 V (ON-state). This is

done to avoid turning on the device into diode mode, which would introduce a voltage shift.

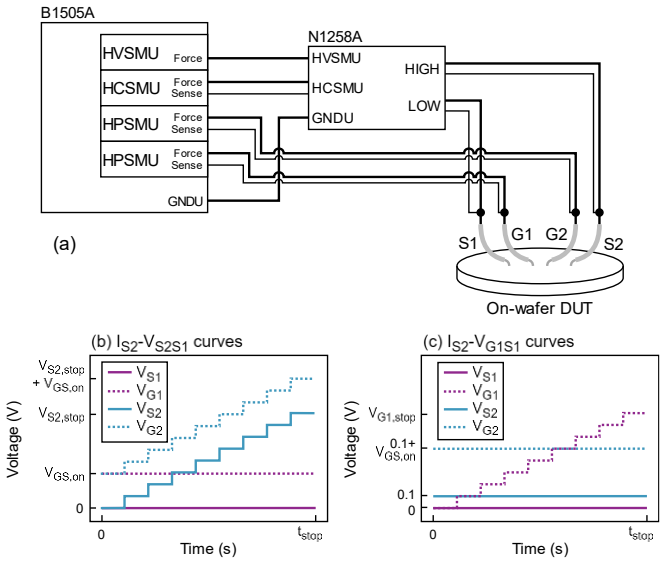

Fig. 4. (a) Test set-up for ON-state characterization with the Keysight B1505A Power Device Analyzer and the Keysight N1258A Module Selector, and the curves that are used for the ON-state characterization: (b) is the equivalent to the I_D-V_{DS} and (c) is the equivalent to the I_D-V_{GS} for traditional HEMTs and MOSFETs.

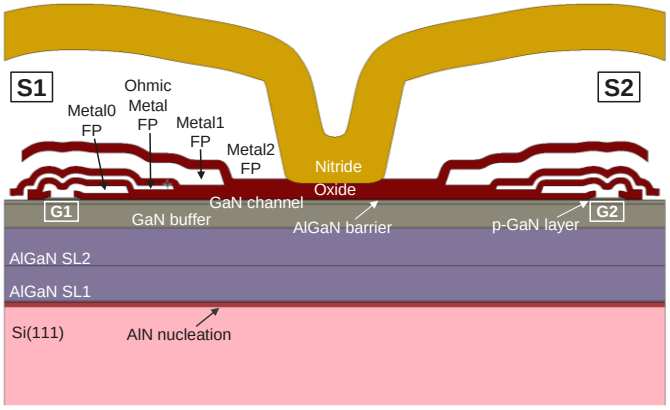

Fig. 5. The cross-section of the TCAD model of the dual-gate BDS developed in Synopsys TCAD, with the dimensions of device A.

In OFF-state, the same synchronized voltage sweep shown for the I_{S2}-V_{S2S1} measurement is required. Due to hardware limitations, both source 2 and gate 2 are connected to the HVSMU, in order to ensures that the correct voltage is applied to both terminals, but only the sum of the two currents can be measured. This is enough to measure the breakdown voltage of the device and the order of magnitude of the OFF-state leakage current.

Due to the high voltages in play, the high electric field can break the air, causing flashover between close-by pads and leading to a premature device failure. To prevent this, Fluorinert™ is applied on-wafer on top of the tested devices.

B. Dual-gate BDS TCAD model

A Technology CAD model of the dual-gate BDS is built in Synopsys TCAD, based on the model of the traditional HEMT [21]. The virtual device is obtained by reproducing the GaN-IC process flow in Sprocess, simulating the epitaxial stack, gate stack and backend formation, followed by a fine remeshing of the most critical areas for the subsequent device simulations. The gate leakage is calibrated against p-GaN gate HEMT I_G-V_{GS} characteristics. A combination of Schottky barrier tunneling and non-local tunneling through trap states in the AlGaN barrier is used. Simulations are performed in transient mode (using sweeping times equal to the measurements) to ensure proper simulation of the dynamics related to the trap states.

Here, the simulation results are used qualitatively to explain the phenomena seen in the experimental results. The simulated cross-section of device A is shown in Fig. 5. Note that only the upper part of the Si substrate is made visible.

III. Results and Discussion

A. ON-state characterization

The I_{S2}-V_{S2S1} results for device B are shown in Fig. 6 and Fig. 7. The voltage V_{S2S1} is swept from 0 V to ±10 V, to test the device in both positive and negative polarization, and, by applying $V_{G1S1,on}$ = $V_{G2S2,on}$ = 7 V to the gates, the device turns on in a bidirectional mode as can be seen in Fig. 6. The device exhibits a symmetrical behavior in the first and third quadrant, and has nearly identical forward and reverse ON-resistances, $R_{ON,F}$ = 19 Ωmm and $R_{ON,R}$ = 18 Ωmm, respectively.

For comparison, imec's reference HEMT with L_{GD} = 16 µm equal to the L_{GG} of the BDS, has a R_{ON} = 16 Ωmm at V_{GS} = 7 V, which implies an ON-resistance about 17% higher for the BDS. This can be seen in Fig. 6, where an I_D-V_{DS} for a HEMT with same dimension ($L_{GD,HEMT}$ = $L_{GG,BDS}$) is reported. This increase in ON-resistance is due to the increase of the total channel length due to the presence of the second gate.

When only one gate is switched on, the device operates in diode mode, as shown in Fig. 7(a) for V_{G1S1} = 7 V, V_{G2S2} = 0 V and Fig. 7(b) for V_{G1S1} = 0 V, V_{G2S2} = 7 V. In this condition, the current is allowed to flow in one direction only and it is blocked in the opposite direction. When in forward (i.e. for positive V_{S2S1} in Fig. 7(a) and negative V_{S2S1} in Fig. 7(b)), the R_{ON} is almost doubled for the diode mode (i.e., 34 Ωmm), and there is a voltage offset of about 3 V due to the V_{S2S1} needed to turn on the junction of the switched-OFF gate. Note that all the R_{ON} values are extracted at the point of maximum output conductance:

$$R_{ON} = g_{out,max}^{-1} \qquad g_{out} = \frac{dI_{S2}}{dV_{S2S1}} \tag{1}$$

for all the operation conditions, for consistency. In reverse bias (i.e. for negative V_{S2S1} in Fig. 7(a) and positive V_{S2S1} in Fig. 7(b)), it can be seen that a leakage of ~30 µA/mm between source 2 and gate 2 occurs when gate 2 is fully ON (V_{G2S2} = 7 V). The same would happen between source 1 and gate 1 when gate 1 is fully ON if source 1 current would be monitored. The leakage between S1 and S2, however, is below 1 nA/mm.

The I_{S2}-V_{G1S1} curve is shown in Fig. 8. The threshold voltage V_{TH} calculated with the second gate ON (V_{G2S2} = 7 V) is equal to 2 V, a result that is perfectly in line with the threshold voltage of the HEMT. The threshold voltage is calculated as the intersection of the slope of the I_{S2}-V_{G1S1} curve at $g_{m,max}$ with the x-axes. An I_{S2}-V_{G2S2} measurement with V_{G1S1} = 7 V also provides the same result (not shown).

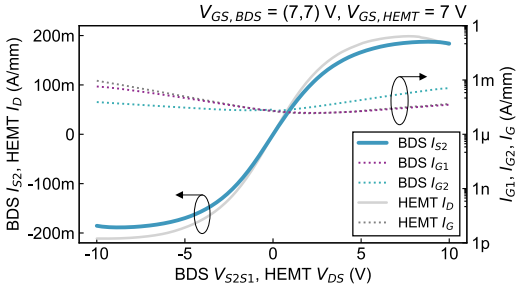

Fig. 6. I_{S2}-V_{S2S1} measurement for device B in bidirectional ON state. In grey the ID-VDS measurement for the corresponding lateral p-GaN HEMT with L_{GD} = L_{GG} = 16 µm.

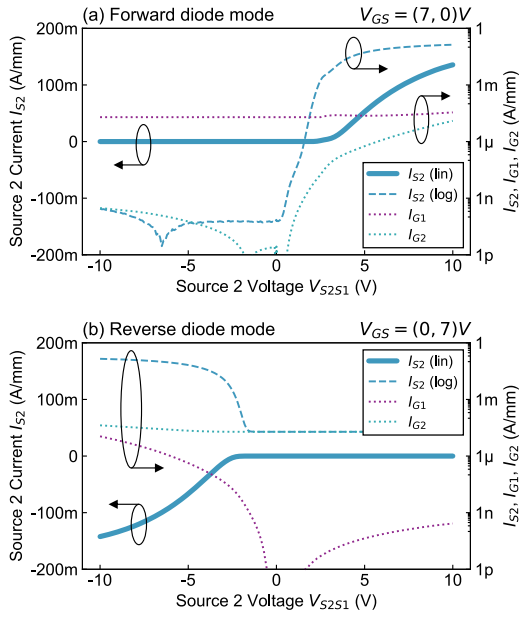

Fig. 7. I_{S2}-V_{S2S1} measurement for device B in (a) forward and (b) reverse diode mode. The I_{S2} current is shown in both linear (left axis-solid line) and log scale (right axis-dashed line).

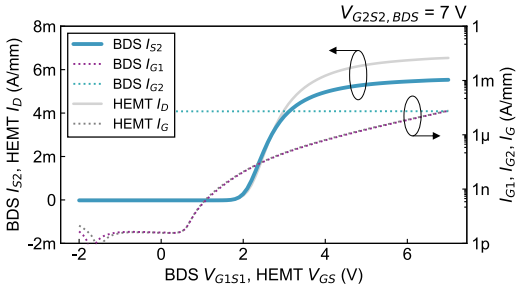

Fig. 8. I_{S2}-V_{G1S1} measurement for device B and the reference HEMT.

B. *Leakage current in OFF-state*

The leakage currents in OFF-state and the breakdown voltage V_{BD} for device E can be seen in Fig. 9, compared with the leakage current of an equivalent HEMT (only positive polarization is measured on the HEMT). From the measurement we can only study the sum of I_{S2} and I_{G2}. In positive polarization, a small leakage current is present and is in line with the HEMT. After ~650 V, the substrate current starts increasing (visible as source 1 current, since it is shorted to the substrate), up to the breakdown. The negative bias case can be studied by either exchanging source 1 with source 2 and gate 1 with gate 2 (note that as a consequence, the substrate is then at high-voltage) or by applying a negative voltage to source 2 and gate 2. The latter is preferred for a better comparison with the measurement set-up. In this case, a buffer current can be seen at source 1 in both Fig. 9 and Fig. 10, due to the turn-ON of the buffer junction caused by the reverse polarization of it. This normally never occurs in the standard p-GaN HEMT (where the high-voltage is always on the drain, and the substrate is always shorted to the source) because it is never biased in the III quadrant. The asymmetry visible on the gate 1 current is caused by the different bias direction, which, for negative V_{S2S1}, brings the source 1-gate 1 to a negative polarity (III quadrant operation). Again, the leakage current starts increasing significantly from ~ -650 V onwards.

In brief, the device shows correct voltage blocking capability up to the target voltage of ±650 V, with a constant leakage current < 10 nA/mm within the operating voltage, in both polarization conditions.

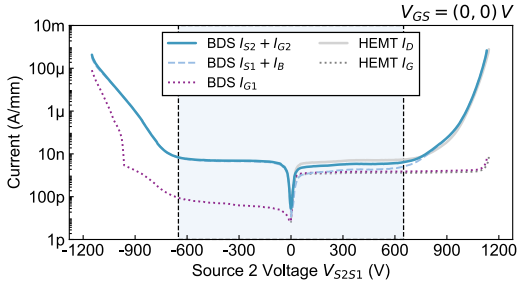

Fig. 9. I_{S2}-V_{S2S1} measurement for device E in OFF state. The last point in both directions is where the breakdown happens.

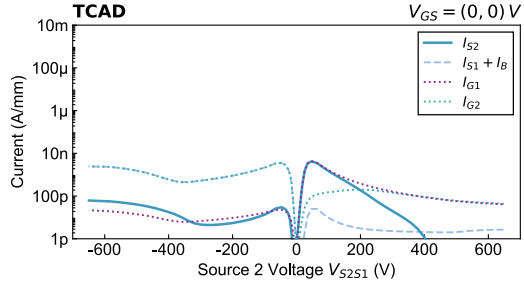

Fig. 10. I_{S2}-V_{S2S1} TCAD simulation of device variation E in OFF state. The simulation is performed up to ±650 V.

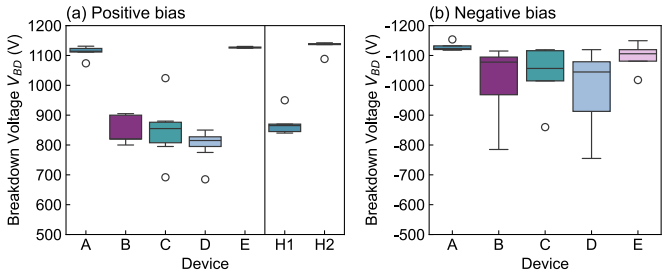

Fig. 11. Breakdown voltage for the unique design variations in (a) positive and (b) negative bias. Device H1 is a HEMT with the same dimensions as BDS D, and H2 is a HEMT with the same dimensions as BDS E.

C. *Design variation analysis for OFF-state optimization*

The breakdown voltage is measured on at least 5 devices of each design variation and the result is shown in Fig. 11(a) for

the positive polarization and Fig. 11(b) for the negative polarization. Also the breakdown of two lateral pGaN HEMTs are reported for comparison: HEMT H1 has the same dimensions as BDS D, without Metal2 field-plate and L_{GFP} = 3/3/3 µm, and HEMT H2 has the same dimensions as BDS E, which includes also the Metal2 field-plate and has L_{GFP} = 2/2/2/2 µm.

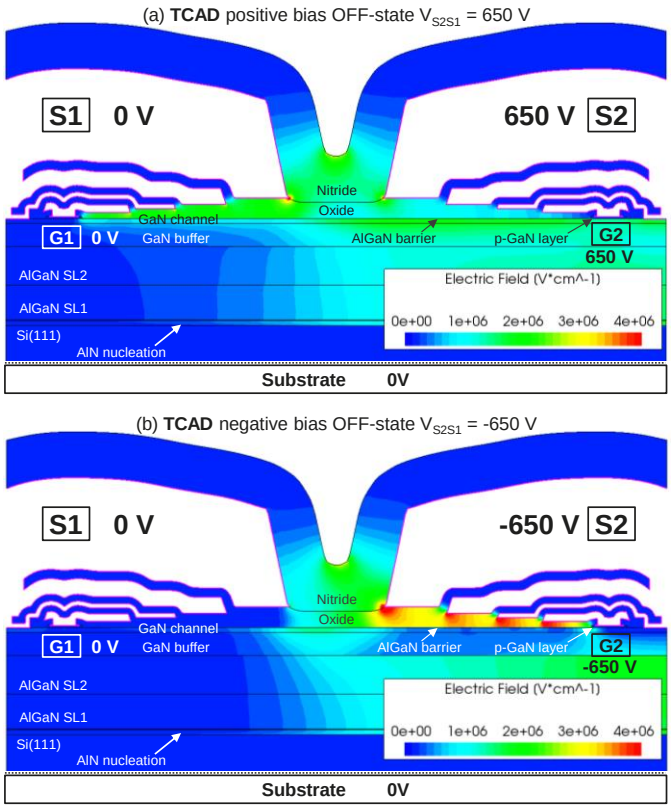

Fig. 12. Electric field in the TCAD simulation cross-section of the dual-gate BDS (design variation E), both pictures in OFF state: (a) positive polarization at V_{S2S1} = 650 V and (b) negative polarization at -650 V.

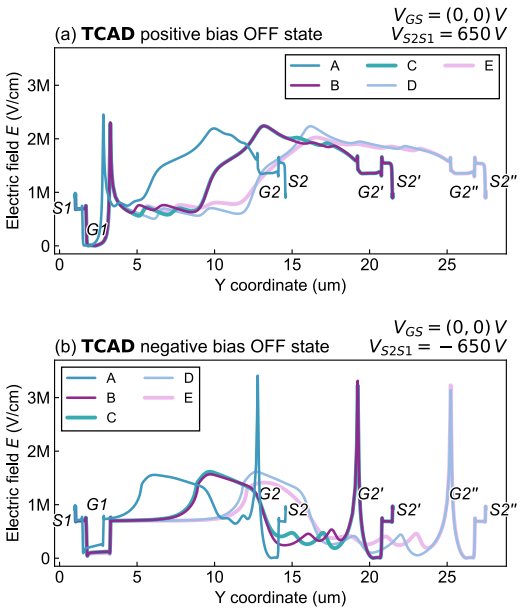

Fig. 13. Cutline of the electric field at the 2DEG level in the TCAD simulation of the dual-gate BDS in OFF state, for (a) positive polarization at V_{S2S1} = 650 V and (b) negative polarization at -650 V for the different design variations.

The breakdown occurs above ±650 V for every design variation. The vertical buffer breakdown is approximately 1.1 kV, a remarkably high value given the fact that the epitaxial stack used in this study is grown on GaN-on-SOI substrates. Hence, the breakdown voltages as reported in Fig. 11 at 1.1 kV, are actually determined by the epitaxial stack. This opens up perspectives for future BDS design variations with even higher breakdown voltages, e.g. on engineered substrates [22]. V_{BD} does not show a strong dependency on L_{GG}, whereas it can be seen that long FPs do have a negative impact on the V_{BD}. Because dual-gate BDSs need to have a symmetrical structure to sustain an applied voltage in both directions, also the field-plates must be designed equally on the two sides, whereas on a HEMT they can have a dedicated optimization for the low potential (source) and high potential (drain) sides. Longer field-plates help to distribute the electric field on the low potential side in the BDS, lowering the electric field peaks. Yet on the high potential side the effect of the field-plates is reduced due the reverse bias condition in the epitaxial stack, causing the electric field to increase, possibly above the critical electric field for GaN.

This can be seen by performing a TCAD simulation of the switch in OFF-state for several variations of L_{GG} and field-plates: in Fig. 12(a) the electric field is shown in the cross-section of the design variation E, and in Fig. 13(a) the cutline at the 2DEG quantum well level for all the design variations is shown. On the right side of the device, where the HV is applied, there is a relationship between the length of the field-plates and the height of the electric field peaks. Devices with larger channel length are normally designed with longer field-plates, to improve the distribution of the electric field, but this offsets the reduction in electric field peaks caused by the increase of the channel length. As a result, devices with longer L_{GG} and long field-plates have similar performance to the devices with shorter L_{GG} and shorter field-plates. For example, comparing devices D and E shows that the former, whose total field-plate length on the HV side is 9 µm, reaches a maximum electric field higher than the latter, whose total field-plate length is 8 µm, despite the same channel length. For the same reason, devices B and C have the same electric field peaks, as their total field-plate length is the same.

In negative bias (Fig. 11(b)) all devices perform similarly, and the breakdown voltage is mainly impacted by the buffer, although a larger spread is observed. These results can be explained by looking at the simulation results of the electric field in Fig. 12(b) and Fig. 13(b). Due to the asymmetry caused by the relative potential of the substrate, the electric field distribution is significantly different, especially in the surrounding of the source 2 (field-plate region, buffer, ...). On the source 1 side, the electric field is now lower than on the source 2 side in the case of positive polarization, due to the fact that the substrate potential is equal to the source 1 potential.

In summary, the optimization of the trade-off between the breakdown voltage and the ON-resistance must take into account the required symmetry of the field-plates and the asymmetry of the substrate potential in the two different bias regimes. From the presented experimental results, it can be seen

that devices with shorter L_{GG} can still meet the robustness requirement as long as the FPs are properly designed, thus reducing the ON-resistance. Conversely, by keeping a broader channel length and tuning the FPs, the breakdown voltage could be further increased.

CONCLUSION

We presented a monolithically integrated GaN bidirectional switch (BDS) fabricated by using the same CMOS-compatible GaN technology platform as for p-GaN gate HEMTs.

The BDS can be fabricated on a GaN-on-Silicon substrate, as well as integrated into a GaN-IC, which would enable the design of a monolithic power converter in GaN, with also the driver circuit on the same die.

The device exhibits bidirectional and diode operation modes, with a small penalty on the ON-resistance in comparison to an equivalent HEMT and reaches the target of 650 V OFF-state operation in both directions.

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