Extreme Silicon Thinning For Back Side Power Delivery Network: Si Thinning Stopping on Scaled SiGe Etch Stop Layer

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Abstract

This paper discusses the challenges relative to the silicon thinning which allows the back side power delivery integration (BSPDN). The back side silicon thinning stopping on a thin $Si_{0.75}Ge_{0.25}$ etch stop layer (ESL) has been investigated as it represents an alternative to the use of SOI wafers. Etch stop layers using 10 nm $Si_{0.75}Ge_{0.25}$ or 10 nm $Si_{0.75}Ge_{0.25}$ boron doped ($Si_{0.75}Ge_{0.25}$:B) have been studied for which different thinning process sequences were considered. All the considered thinning sequences are terminated with a diluted ammonia (NH_4OH) process which provides the selectivity towards the ESL. Considering a 10 nm $Si_{0.75}Ge_{0.25}$:B as an ESL considerably increases the selectivity of the last diluted NH_4OH silicon etching step. It nevertheless induces a risk of device poisoning caused by the diffusion of boron. Considering a 10 nm $Si_{0.75}Ge_{0.25}$ as an ESL has been then demonstrated using different thinning process sequences. Those alternative thinning sequences were optimized with respect to the silicon removal within wafer uniformity.

Introduction

The power delivery network and transistor interconnects are currently part of the back end of line. To free up more space for transistor interconnects, it was recently proposed to move the power supply to the chip backside [1]. This requires a wafer-to- wafer bonding followed by a wafer backside thinning stopping at the final epitaxial (EPI) silicon which acts as the channel material. The use of an epitaxial SiGe as an etch stop layer (ESL) is considered to preserve a uniform EPI silicon after the complete thinning as described in figure 1.

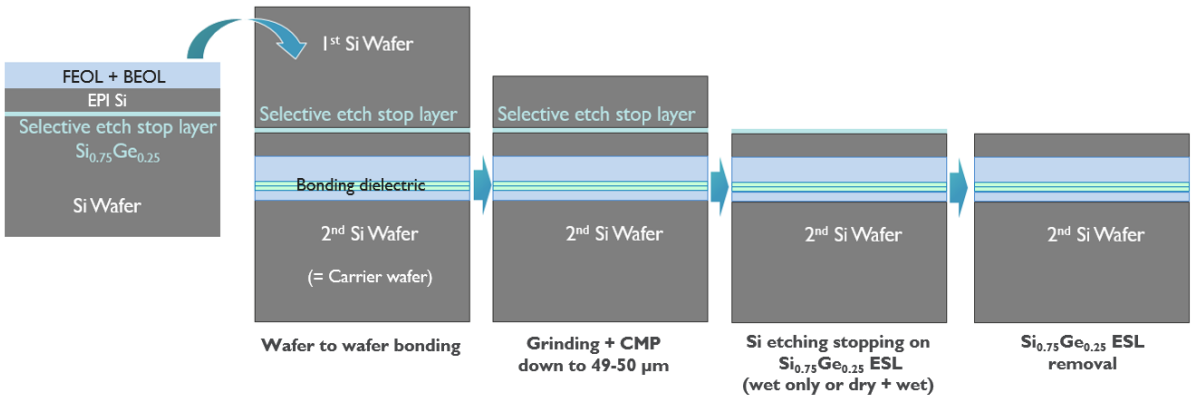

Figure1: Si thinning stopping on SiGe ESL for the BSPDN [3].

This epitaxial silicon layer serves as the channel and any defects will negatively impact the yield and the device performance. The number of crystal defects in the EPI silicon coming from the SiGe ESL needs to be kept as low as possible [2]. The Ge concentration and thickness are initially set at 25% and 50 nm as a compromise between the need of growing a defect free SiGe ESL and the silicon etch selectivity during the thinning [3]. In this study, we first describe an initial thinning process sequence

that uses a 50 nm $Si_{0.75}Ge_{0.25}$ ESL. This initial thinning sequence consists in a grinding, CMP (chemical and mechanical polishing), dry etch and a last alkaline wet silicon removal. We then address the challenge of reducing the SiGe ESL and its implications in term of total thickness variation control (TTV) during the thinning.

Alkaline silicon wet etch after grinding + CMP + dry etch stopping on 50 nm $Si_{0.75}Ge_{0.25}$ ESL

A wafer backside thinning sequence has already been described by Jourdain and al [3]. It consists in a sequence of a grinding followed by a chemical and a CMP stopping at 49 µm of remaining silicon. The remaining silicon thickness after grinding and CMP is set based on the TTV, damage, and induced stress under the silicon [4]. A dry etch continues the thinning down to a remaining silicon thickness of 10 µm [3; 5]. A final wet silicon removal consists in a two-step alkaline wet etching:

1/ A diluted Tetramethylammonium hydroxide (TMAH) 1_5 (1 volume of TMAH mixed with 5 volumes of de-ionized water) at 80 ºC stops at 3 µm remaining silicon. It provides an etch rate on silicon of about 1 µm/min.
2/ A diluted NH_4OH 1_60 (1 volume of NH_4OH mixed with 60 volumes of de-ionized water) at 70 ºC stops the silicon etch on the $Si_{0.75}Ge_{0.25}$ ESL. The silicon etch rate is about 0.22 µm/min for a $Si_{0.75}Ge_{0.25}$ loss of about 2.2 nm/min.

The final alkaline wet silicon removal starts first with the diluted TMAH to rapidly remove the silicon. Because of its high etch rate, the diluted TMAH does not directly stop on the $Si_{0.75}Ge_{0.25}$ ESL. When the thinning approaches the $Si_{0.75}Ge_{0.25}$ ESL (below 3 µm remaining silicon), the diluted NH_4OH is then used to stop on the ESL thanks to its intrinsic lower etch rate on the $Si_{0.75}Ge_{0.25}$.

Figure 2 shows the intrinsic lower etching rate on $Si_{0.75}Ge_{0.25}$ of the diluted NH_4OH over diluted TMAH. The wet etch experiments are performed on 300 mm wafers on which a $Si_{0.75}Ge_{0.25}$ EPI is grown on Si (100) using a SCREEN SU-3100 300 mm single wafer tool. For the same initial dilution and temperature, the diluted NH_4OH will show a lower $Si_{0.75}Ge_{0.25}$ etch rate. The $Si_{0.75}Ge_{0.25}$ wet etch rate difference between TMAH and NH_4OH for the same dilution suggests the role of the pH (= OH^- concentration) knowing that the TMAH is a strong base and NH_4OH a weak base.

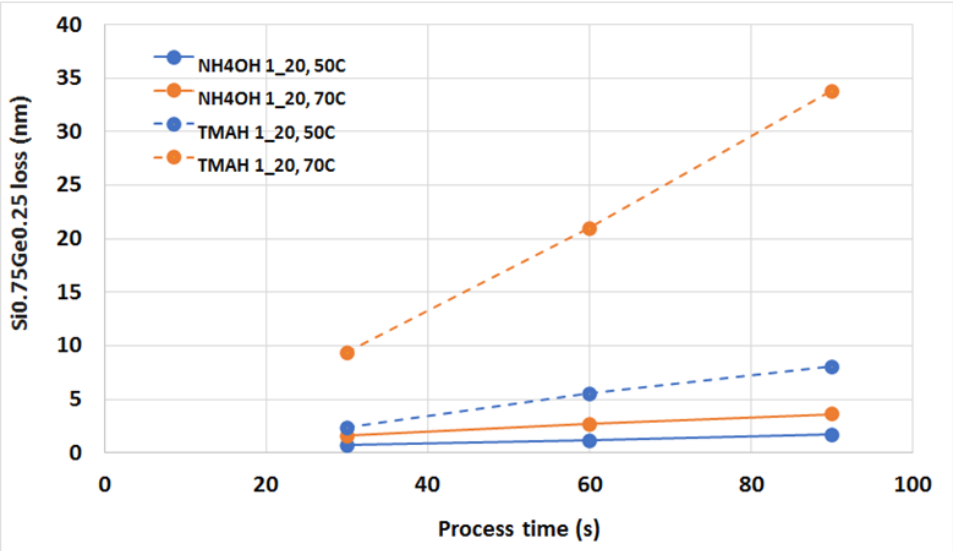

Figure 2: $Si_{0.75}Ge_{0.25}$ loss with diluted NH_4OH 1_20 vs diluted TMAH 1_20

The SiGe ESL layer is finally removed with a formulated chemistry having a high selectivity to silicon [6].

Need for a high selective alkaline silicon etch stopping on thin $Si_{0.75}Ge_{0.25}$ ESL: use of boron doped $Si_{0.75}Ge_{0.25}$ ($Si_{0.75}Ge_{0.25}$:B) as an ESL.

Defects in the epitaxial Si layer due to strain relaxation of the underlying SiGe layer should be avoided. The 50 nm $Si_{0.75}Ge_{0.25}$ might be in or close to the metastable region [7]. Especially at the edge of the wafer, the risk for strain relaxation is a concern [2]. To avoid strain relaxation during post-epi processing steps which require a certain thermal budget (typically for the shallow trench isolation anneal or for activation anneal), the germanium concentration and thickness should be kept as low as possible.
It is then proposed to consider an ESL as thin as 10 nm $Si_{0.75}Ge_{0.25}$. With a reduction of the $Si_{0.75}Ge_{0.25}$ ESL thickness, the TTV control during the various stages of the silicon thinning becomes critical. There is a need for a silicon etch process stopping on a SiGe ESL with a higher etch selectivity. Considering boron doped $Si_{0.75}Ge_{0.25}$ ($Si_{0.75}Ge_{0.25}$:B) as an ESL instead of $Si_{0.75}Ge_{0.25}$ initially appears a suitable option for increasing the selectivity of the alkaline etching with the diluted NH_4OH.

It is proposed to evaluate the selectivity towards the $Si_{0.75}Ge_{0.25}$:B over $Si_{0.75}Ge_{0.25}$ during the Si etching with the diluted NH_4OH chemistry. The experiments are performed on 300 mm wafers on which 10 nm EPI $Si_{0.75}Ge_{0.25}$ + 500 nm EPI Si-cap are grown on Si (100). 10 nm $Si_{0.75}Ge_{0.25}$ is compared with 10 nm $Si_{0.75}Ge_{0.25}$:B as an ESL. After the EPI growth, the following thermal budget is applied: 1000 ˚C under He for 1.5s (corresponding to an activation anneal) followed by a 500 ˚C steam anneal for 60 min ending with an anneal at 700 ˚C under N_2 for 20 min (corresponding to the STI anneal). The silicon wet etch process uses a 1_70 diluted NH_4OH at 70 ˚C on a SCREEN SU-3100 300 mm single wafer tool. The wafer mass loss is recorded for given increments of diluted NH_4OH process time as shown in figure 3. The wafer mass loss evolution will be characterized by 3 phases:

1/ Si etching: the wafer mass loss increases as function of the diluted NH_4OH process time since the 500 nm EPI is being etched.
2/ Etching through the $Si_{0.75}Ge_{0.25}$ ESL: the wafer mass loss is reduced when all the 500 nm EPI has been removed as the etching rate of $Si_{0.75}Ge_{0.25}$ ESL is a factor ~100 lower.
3/ Etching through the silicon substrate: the wafer mass loss restarts at the moment all the $Si_{0.75}Ge_{0.25}$ ESL has been removed.

Tracing the evolution of the wafer mass shows how long it takes for the diluted NH_4OH to fully remove the $Si_{0.75}Ge_{0.25}$ ESL.

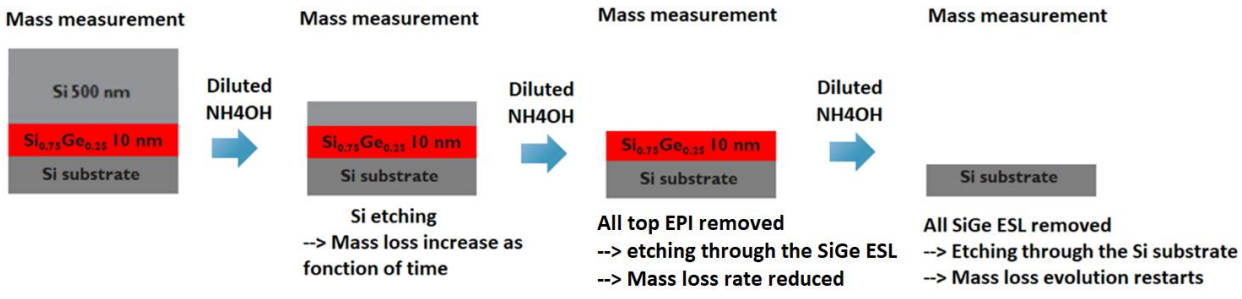

Figure 3: Wafer mass loss evolution with diluted NH_4OH principle on the EPI stacks Si 500 nm_$Si_{0.75}Ge_{0.25}$ 10 nm

It is shown in figure 4 that it takes around 260 s (160 s = start of $Si_{0.75}Ge_{0.25}$ removal and 420 s = start of the silicon substrate removal). One the other hand, the 10 nm of $Si_{0.75}Ge_{0.25}$: B remains not fully removed even for an over etch time of 850 s (160 s = start of $Si_{0.75}Ge_{0.25}$: B removal and 1000

s = end of the experiment). The higher selectivity when using $Si_{0.75}Ge_{0.25}$: B over $Si_{0.75}Ge_{0.25}$ as an ESL is then confirmed

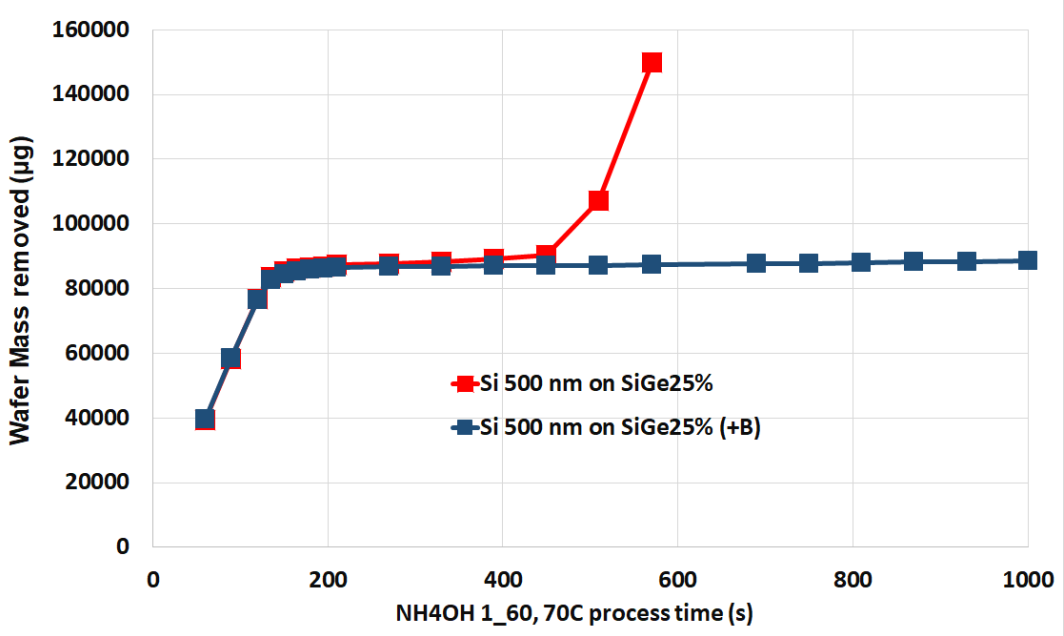

Figure 4 : Wafer mass loss evolution with diluted NH4OH for different EPI stacks : 500 nm Si-cap / 10 nm_$Si_{0.75}Ge_{0.25}$ / Si-substrate vs 500 nm Si-cap / 10 nm $Si_{0.75}Ge_{0.25}$: B / Si-substrate.

We further confirm via TEM the aspect of the $Si_{0.75}Ge_{0.25}$: B ESL for 2 given diluted NH_4OH process times as shown in figure 5: 210 s which corresponds to the beginning of the over etch period and 1000 s which corresponds to the end of the experiment. The apparent roughness of the $Si_{0.75}Ge_{0.25}$:B after the etching with the diluted NH_4OH chemistry suggests a preferential etching through the epitaxial defects. The presence of EPI defect suggests a possible role of the post EPI anneal that might cause clustering of boron atoms.

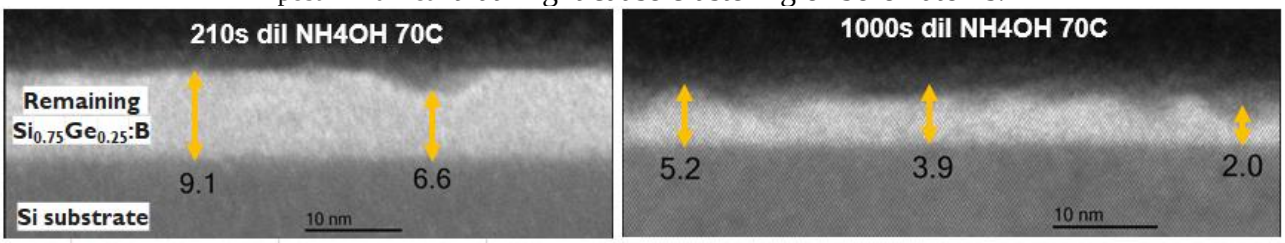

Figure 5: Remaining $Si_{0.75}Ge_{0.25}$: B thickness after 210 s and 1000 s diluted NH_4OH process time

The boron diffusion is a parameter to be taken into account when considering the $Si_{0.75}Ge_{0.25}$:B as an ESL. The boron is susceptible to diffuse through the silicon EPI channel during the device fabrication process and then compromise the channel properties if it diffuses too deep. The diffusion depth will depend on the total thermal budget. That behavior has been verified on an EPI stack made of 20 nm $Si_{0.75}Ge_{0.25}$:B + 150 nm Si-cap grown directly on Si (100). The following thermal budget is applied: 1000 ˚C under He for 1.5s (corresponding to an activation anneal) followed by a 500 ˚C steam anneal for 60 min ending with an anneal at 700 ˚C under N_2 for 20 min (corresponding to the STI anneal). Figure 6 shows a boron diffusion of 30 nm into both the silicon cap EPI and the silicon substrate.

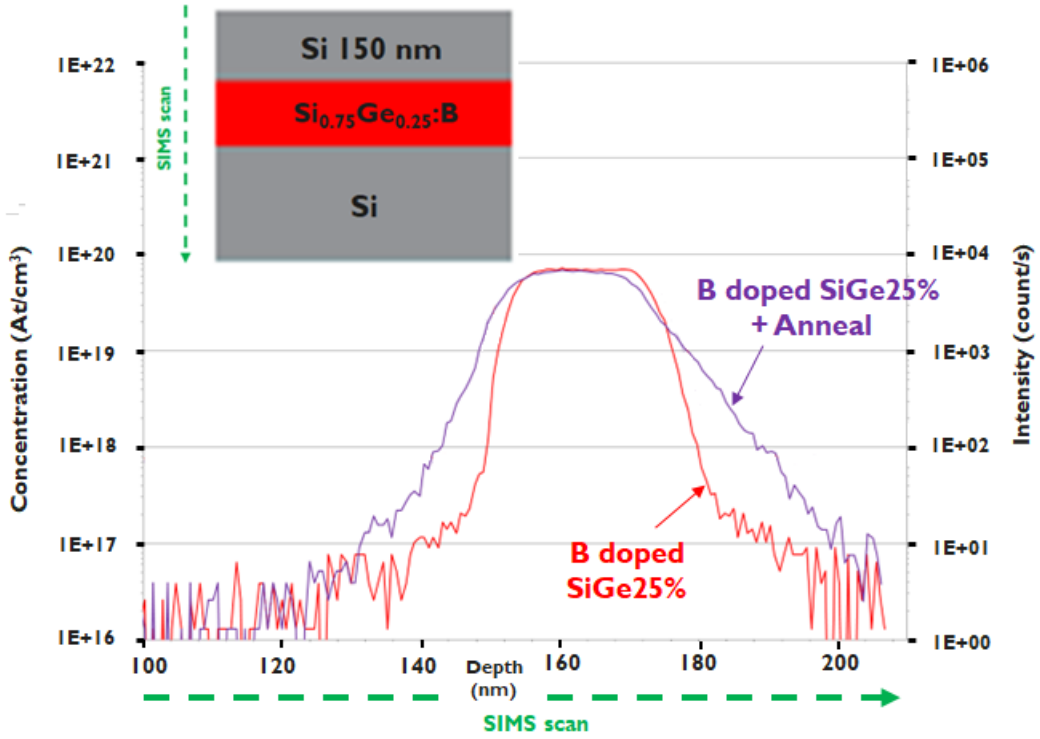

Figure 6: Boron diffusion into the Si after the anneal on a 10 nm $Si_{0.75}Ge_{0.25}$:B + 150 nm Si EPI stack

Figure 7 illustrates the boron diffusion distance with respect to the dimension of the EPI silicon channel. In the case where the EPI channel is several hundred of manometers (figure 7, left side), the diffused boron can appear still far from touching the front etch of line part of the device. For the case where the EPI silicon channel (figure 7, right side), the diffused boron represents a serious risk of affecting the device region.

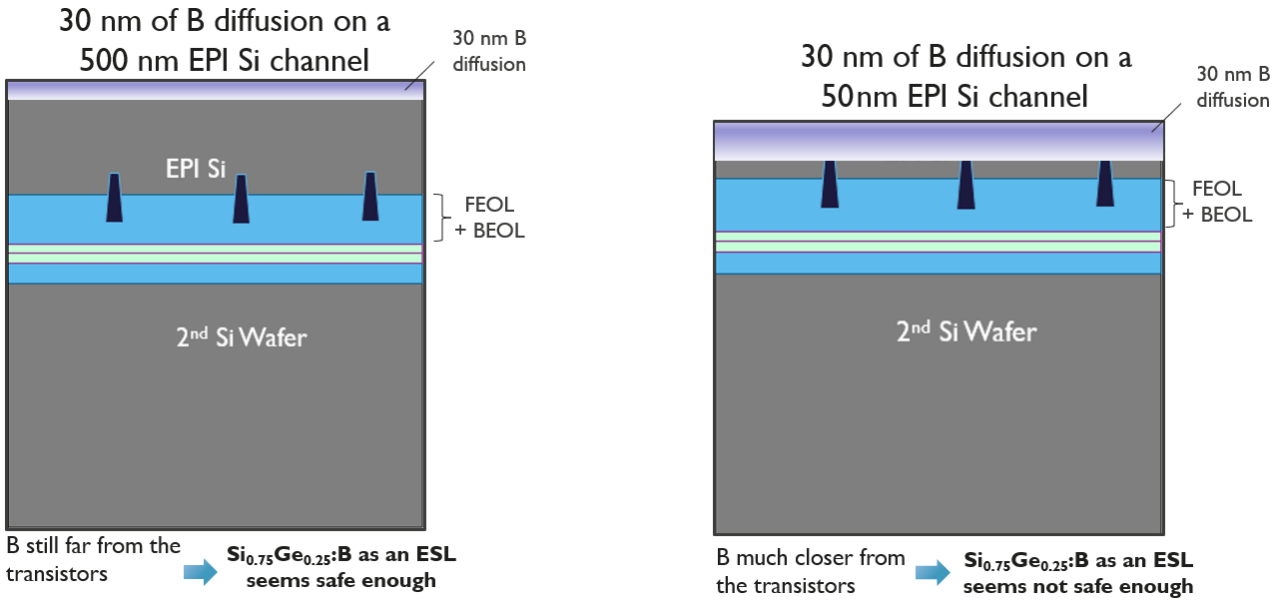

Figure 7: Boron diffusion on thin vs thick grown Si EPI channel

Selective alkaline silicon etch stopping on thin $Si_{0.75}Ge_{0.25}$ ESL: $Si_{0.75}Ge_{0.25}$: TTV (Total Thickness Variation) control over the entire thinning sequence.

The use of an undoped $Si_{0.75}Ge_{0.25}$ is ESL, requires a more precise TTV control through the entire thinning sequence. The grinding, CMP, and the subsequent wet etch steps need to be optimized at their best of their capabilities with respect to the TTV control.
The capability in stopping the Si thinning on 10 nm $Si_{0.75}Ge_{0.25}$ ESL has been evaluated. 300 mm Si (001) wafers are used on which 10 nm EPI $Si_{0.75}Ge_{0.25}$ + 500 nm EPI Si-cap has been grown. The wafers are then bonded on a carrier wafer and thinned down at the wafer back side.
Alternative thinning routes are proposed in which grinding, CMP, HF_HNO_3, diluted TMAH, and diluted NH_4OH are used to enable the silicon thinning stopping on a 10 nm $Si_{0.75}Ge_{0.25}$ ESL. The grinding and CMP experiments are performed on a DGP8761HC 300 mm tool grinder from DISCO (Grinding, CMP and post CMP cleaning modules are integrated in one tool). Wet etching in HF_HNO_3, diluted TMAH, and diluted NH_4OH is performed on a 300 mm single wafer tool SU-3200 from SCREEN. The diluted TMAH uses the MV scan feature (SCREEN) to better compensate for the incoming Si thickness profile.

Different silicon thinning sequences have been considered for which the grinding and CMP sequences aim to stop on 50, 10 or 3 µm of remaining Si, respectively (Fig. 8):

- Sequence 1: Grinding + CMP (→ 50 µm remaining Si) + HF_HNO_3 + diluted TMAH MV scan + diluted NH_4OH.
- Sequence 2: Grinding + CMP (→ 10 µm remaining Si) + diluted TMAH MV scan + diluted NH_4OH.
- Sequence 3: Grinding + CMP (→ 3 µm remaining Si) + diluted NH_4OH.

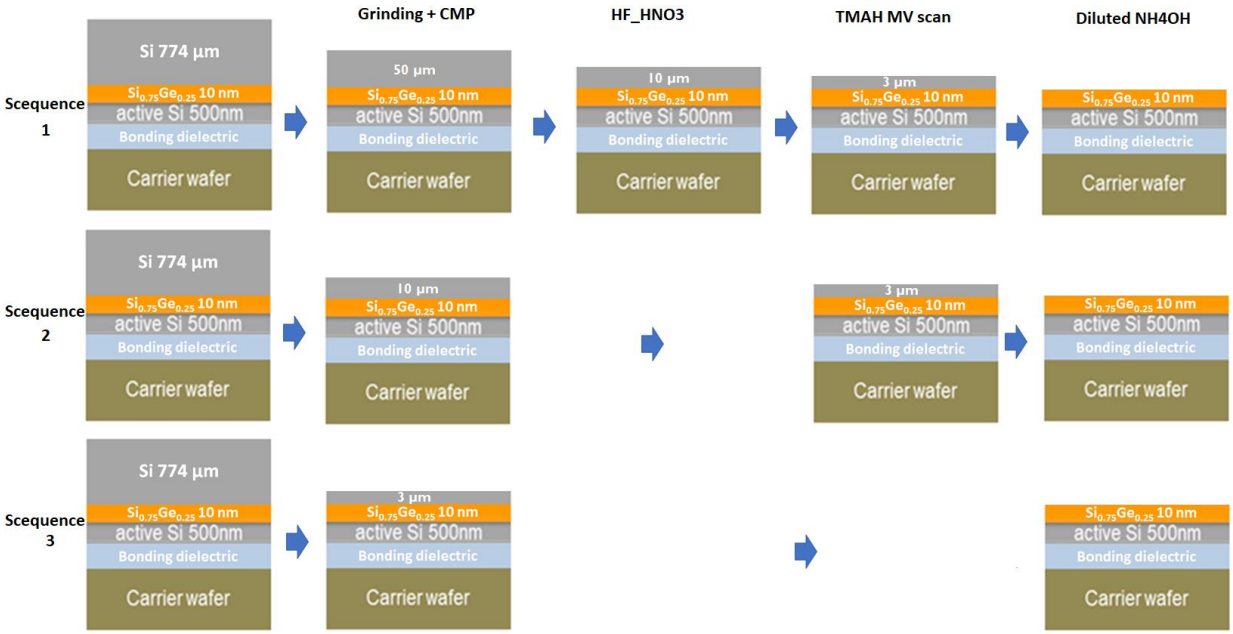

Figure 8: Different scenarios considered for the back side Si thinning stopping on 10 nm $Si_{0.75}Ge_{0.25}$ ESL.

For the 3 considered options, the final TTV before the last diluted NH4OH step (measured with a TTV interferometer from SUSS MicroTec) exhibits the same values at around 1-1.3 µm as shown in figure 9. The TTV before the last diluted NH_4OH step decides on the thinning process performance. It also allows to extrapolate the estimated $Si_{0.75}Ge_{0.25}$ ESL loss after the diluted NH_4OH step.

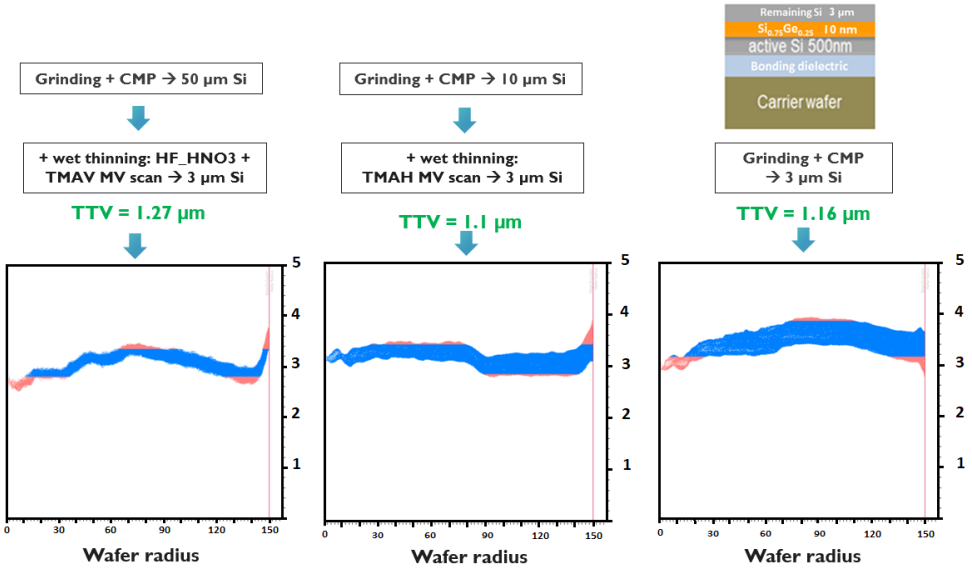

Figure 9: TTV measurements of the remaining Si after the different thinning sequences (1, 2, 3 from left to right) and before processing of the diluted NH_4OH step.

The last Si etching step in diluted NH_4OH is performed for all three thinning scenarios and the remaining Si $Si_{0.75}Ge_{0.25}$ ESL is characterized by XRR and TEM as shown in figure 10 and 11. For all three thinning scenarios, the capability to stop the last Si etching within the 10 nm $Si_{0.75}Ge_{0.25}$ ESL is demonstrated. In all cases, the thickness loss of the ESL lies below 5 nm, leading to remaining ESL thicknesses above 5 nm.

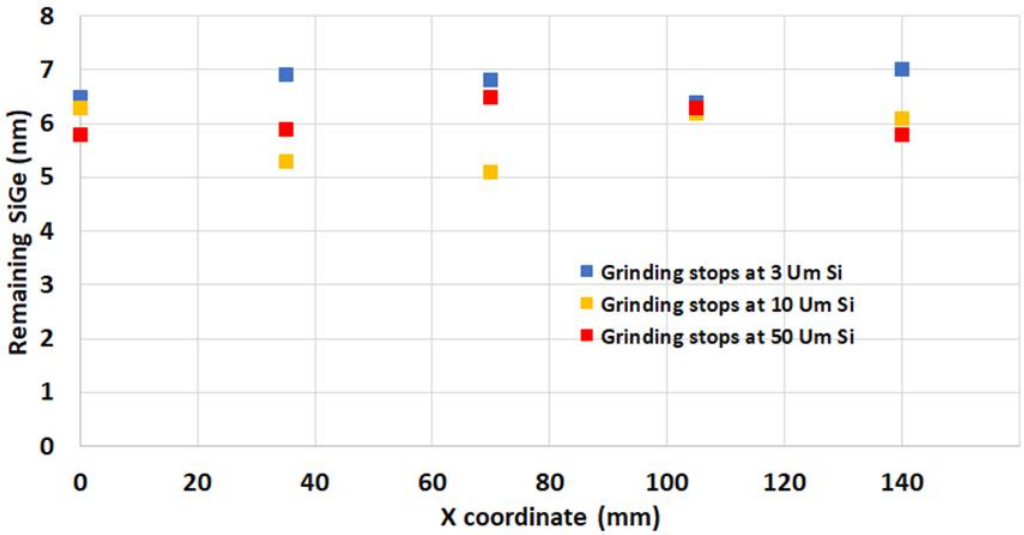

Figure 10: Remaining $Si_{0.75}Ge_{0.25}$ ESL thickness as extracted from XRR measurements after the last diluted NH_4OH step of the different Si thinning sequences and for different positions over the wafer. X coordinate shows the radial distance from the wafer center.

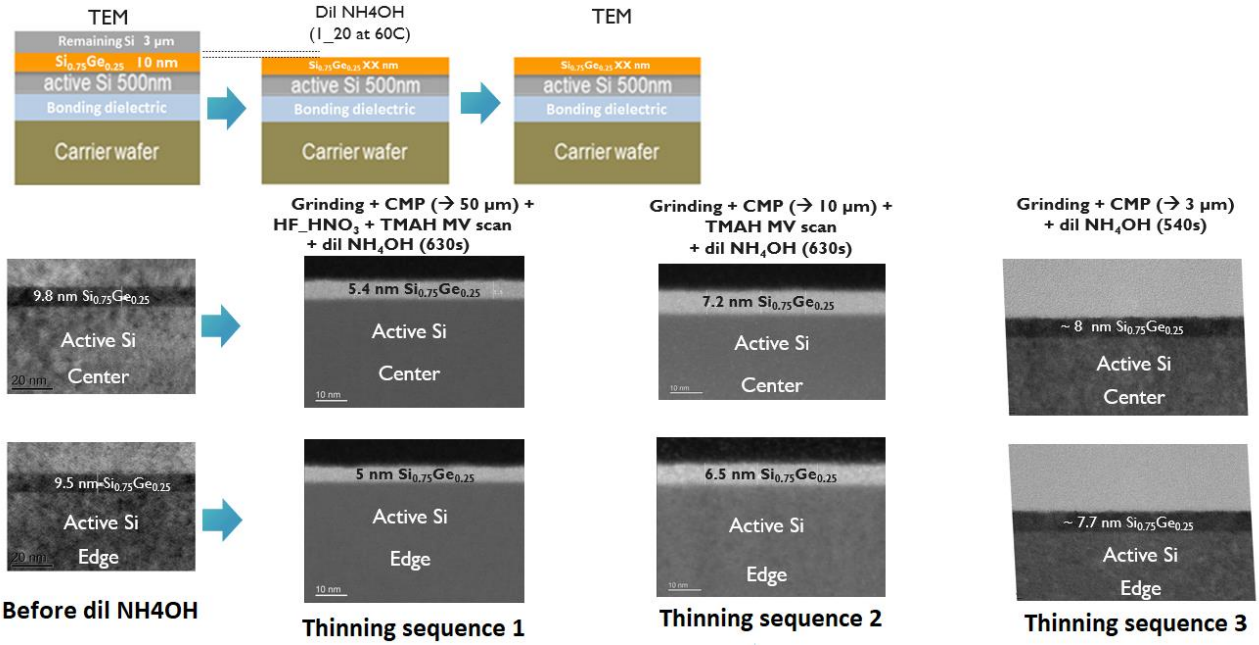

Figure 11: TEM images of the remaining $Si_{0.75}Ge_{0.25}$ ESL after the different thinning sequences after the last step of diluted NH_4OH

Conclusion

To allow the BSPDN integration, the back side silicon thinning stopping on a thin $Si_{0.75}Ge_{0.25}$ has been investigated. On one hand, 10 nm $Si_{0.75}Ge_{0.25}$: B as ESL has been considered. It confirmed a greater robustness towards the alkaline etching with diluted NH_4OH over the $Si_{0.75}Ge_{0.25}$. It nevertheless has the drawback to allow the boron diffusion into the Si channel. In addition, there is a severe risk for B precipitation during the post-epi processing steps which require a relatively high thermal budget. On the other hand, an undoped ESL of 10 nm $Si_{0.75}Ge_{0.25}$ has been studied. Because of the thin ESL and the lower etching selectivity between Si and undoped $Si_{0.75}Ge_{0.25}$ during the last Si wet-chemical etching step in NH_4OH, sustaining a low TTV during the entire thinning sequence is critical to enable the integration of this module in device flows. Different thinning variants were proposed. All of them show the capability to have a controlled and homogeneous etch stopping within the 10 nm $Si_{0.75}Ge_{0.25}$ etch stop layer.

References

[1] A. Veloso et al., Symposium on VLSI Technology Digest of Technical Papers, 2021
[2] R. Loo et al., ECS J. Solid State Sci. Technol. **10**, 014001, 2021
[3] A. Jourdain et al., IEEE 70th Electronic Components and Technology Conference (ECTC), pp. 42-48, 2020
[4] F. Inoue et al., IEEE 66th Electronic Components and Technology Conference (ECTC), pp.2095-2102, 2016
[5] A. Jourdain et al., IEEE 68th Electronic Components and Technology Conference (ECTC), pp. 1529-1536, 2018.
[6] K. Komori et al., Solid State Phenomena **282**, pp 107-112, 2018
[7] D.J. Paul et al., Semiconductor Science and Technology **19** (10), R75-R108, 2004